The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC810

Isolated 2x CAN Bus

Version 2.0

User Manual

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TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek / Germany
Phone: +49-(0)4101-4058-0 Fax: +49-(0)4101-4058-19
E-mail: info@tews.com www.tews.com

TPMC810-10R

Isolated 2x CAN bus, 2x DB9 front panel connector, P14 Back I/O

TPMC810-20R

Isolated 2x CAN bus, 2x DB9 front panel connector, P14 Back I/O with same pin assignment as TPMC816-10R

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	January 2003
1.1	Correction “Configuration EEPROM”	April 2003
1.2	Correction “Configuration EEPROM”	September 2003
1.3	Weight Added and Version	April 2004
1.4	Corrected PCI Base Address Number in Fig. 3-2	October 2005
1.5	New address TEWS LLC	September 2006
1.1.6	New notation for User Manual and Engineering Documentation	June 2009
1.1.7	- General Update - Added CAN Data Transmission Rate figures - Updated CAN Channel Interface figure in the DIP Switch Settings subchapter (generic ground symbol instead of earth ground symbol) - Added a note to the Pin Assignment chapter regarding isolated ground connection.	June 2019
2.0.0	User Manual Update for TPMC810 V2.0.	April 2022

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1 Product Description

The TPMC810 is a standard single-width 32 bit PMC with two independent CAN bus channels, isolated from the main system and from each other.

The TPMC810 provides two Philips/NXP SJA1000 CAN controllers (CAN specification 2.0B supported) and CAN High Speed transceivers are utilized for the CAN bus I/O interface. Data transmission rates from 60kb/s to 1 Mb/s are supported.

An on-board configuration option (DIP switch) is provided for each CAN bus channel to configure on-board termination and/or pass through mode for the CAN bus.

Each channel can generate an interrupt on INTA.

The TPMC810 provides front panel I/O via two DB9 male connectors and rear panel I/O via P14. A special order option providing the same rear I/O pin assignment as TPMC816 is available.

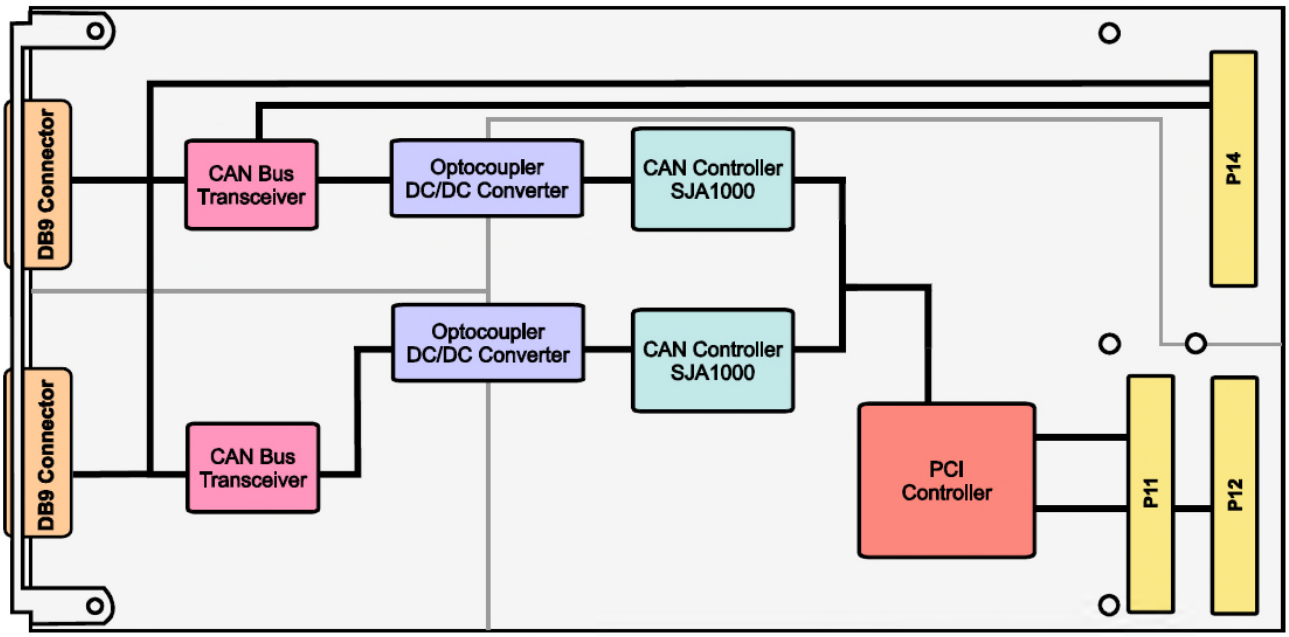

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI Rev. 3.0 compatible 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	TEWS PCI Interface FPGA	
CAN Controller	2 x SJA1000 @ 16MHz (Philips/NXP)	
CAN Transceiver	2 x TJA1050 (Philips/NXP)	
I/O Interface		
Number of CAN Bus Channels	2 (Isolated against each other)	
CAN Bus Interface	CAN High Speed (11898-2)	
CAN Data Transmission Rate	Minimum: 60kbaud (TJA1050 TXD Dominant Time-Out Feature) Maximum: 1Mbaud	
I/O Connector	2 x Male DB9 front panel connector PMC P14 I/O (64 pin Mezzanine Connector)	
Physical Data		
Power Requirements	207mA typical @ +5V DC	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +125°C
MTBF	527122h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	73.3g	

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This PMC module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with appropriate care.

3.2 Ground for Isolated I/O

I/O Connector's isolated ground signals must be connected to external ground.

4 Addressing

4.1 PCI Configuration space

PCI CFG Register Address	Write '0' to all unused (Reserved) bits								PCI writeable	Initial Values (Hex Values)
	31	24	23	16	15	8	7	0		
0x00	Device ID				Vendor ID				N	032A 1498
0x04	Status				Command				Y	0280 0000
0x08	Class Code						Revision ID		N	028000 00
0x0C	not supported		Header Type		not supported		not supported		Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers								Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers								Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0								Y	FFFFFE00
0x1C	not supported								Y	00000000
0x20	not supported								Y	00000000
0x24	not supported								Y	00000000
0x28	not supported								N	00000000
0x2C	Subsystem ID				Subsystem Vendor ID				N	000A 1498
0x30	not supported								Y	00000000
0x34	Reserved						Cap. Ptr.		N	000000 40
0x38	Reserved								N	00000000
0x3C	Max_Lat		Min_Gnt		Interrupt Pin		Interrupt Line		Y[7:0]	00 00 01 00
0x40-0xFF	Reserved									00000000

Table 4-1 : PCI Controller Header

4.2 PCI Address Space Overview

PCI BAR	PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	2 (0x18)	MEM	512	8	BIG	CAN Controller Address Space
1	3 (0x1C)	-	-	-	-	Not Used
2	4 (0x20)	-	-	-	-	Not Used
3	5 (0x24)	-	-	-	-	Not Used

Table 4-2 : PCI Address Space Overview

4.3 Serial EEPROM Memory

The serial EEPROM memory contains by default the TEWS PCI Interface FPGA configuration data for compatibility reasons. However, the entire configuration data are stored within and loaded from the internal flash of the PCI target chip.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x032A	0x1498	0x0280	0x0000	0x0280	0x0000	s.b.	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x0001	0x0000	0x0000
0x20	0x0000	0x0006	0x0000	0x0003	0x0FFF	0xFE00	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x1502	0x4120	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	0x0081	0x0000	0x0181	0x0000	0x0000
0x70	0x0000	0x0000	0x0030	0x0041	0x0078	0x0040	0x0224	0x96D0
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 4-3 : Configuration EEPROM

Subsystem-ID Value (Offset 0x0C): TPMC810-10 0x000A

TPMC810-20 0x0014

4.4 Local Configuration Register (LCR)

The PCI base address for the PCI Controller Configuration Registers is PCI Base Address 0 (PCI Memory Space, Offset 0x10 in the PCI Configuration Space) or PCI Base Address 1 (PCI I/O Space, Offset 0x14 in the PCI Configuration Space).

Do not change hardware dependent bit settings in the PCI Controller Configuration Registers.

Offset from PCI Base Address	Register	Value	Description
0x00	Local Address Space 0 Range	0x0FFF_FE00	CAN Controller Address Space
0x04	Local Address Space 1 Range	0x0000_0000	N/A
0x08	Local Address Space 2 Range	0x0000_0000	N/A
0x0C	Local Address Space 3 Range	0x0000_0000	N/A
0x10	Expansion ROM Range	0x0000_0000	
0x14	Local Address Space 0 Local Base Address (Remap)	0x0000_0001	
0x18	Local Address Space 0 Local Base Address (Remap)	0x0000_0000	
0x1C	Local Address Space 0 Local Base Address (Remap)	0x0000_0000	
0x20	Local Address Space 0 Local Base Address (Remap)	0x0000_0000	
0x24	Expansion ROM Local Base Address (Remap)	0x0000_0000	
0x28	Local Address Space 0 Bus Region Descriptor	0x1502_4120	
0x2C	Local Address Space 1 Bus Region Descriptor	0x0000_0000	
0x30	Local Address Space 2 Bus Region Descriptor	0x0000_0000	
0x34	Local Address Space 3 Bus Region Descriptor	0x0000_0000	
0x38	Local Exp. ROM Descriptor	0x0000_0000	
0x3C	Chip Select 0 Base Address	0x0000_0081	
0x40	Chip Select 1 Base Address	0x0000_0181	
0x44	Chip Select 2 Base Address	0x0000_0000	
0x48	Chip Select 3 Base Address	0x0000_0000	
0x4C	Interrupt Control/Status	0x0041	
0x4E	EEPROM Write Protect Boundary	0x0030	
0x50	Miscellaneous Control Register	0x0078_0040	
0x54	General Purpose I/O Control	0x0224_96D0	
0x70	Hidden1 Power Management data select	0x0000_0000	
0x74	Hidden 2 Power Management data scale	0x0000_0000	

Table 4-4 : PCI Controller Configuration Register Map

4.5 CAN Controller Register Address Space

4.5.1 Local Register Map

All local registers of the TPMC810 are accessible in the memory space of the PMC module.

The PCI base address for the Local Registers is PCI Base Address 2 (PCI Memory Space, Offset 0x18 in the PCI Configuration Space).

CAN CONTROLLER REGISTER SPACE		
Offset to PCI Base Address 2	**Register Name**	**Size (Bit)**
CAN Controller Channel 1		
0x000	CAN Controller CH1 Address 0	8
0x001	CAN Controller CH1 Address 1	8
0x002	CAN Controller CH1 Address 2	8
…	…	…
0x07F	CAN Controller CH1 Address 127	8
0x080 … 0x0FF	Reserved	-
CAN Controller Channel 2		
0x100	CAN Controller CH2 Address 0	8
0x101	CAN Controller CH2 Address 1	8
0x102	CAN Controller CH2 Address 2	8
…	…	…
0x17F	CAN Controller CH2 Address 127	8
0x180 … 0x1FF	Reserved	-

Table 4-5 : CAN Controller Register Space

4.5.2 SJA1000 CAN Controller Registers

The SJA1000 is controlled via a set of registers (control segment) and a RAM (message buffer).

The following table “Registers of the SJA1000” lists these registers grouped according to their usage in a system, the addresses are decimal values.

Note that some registers are available in PeliCAN Mode only and that the Control Register is available in BasicCAN Mode only. Furthermore some registers are read only or write only and some can be accessed during Reset Mode only.

For more information about the registers with respect to read and/or write access, bit definition and reset values, please consult the SJA1000 CAN Controller data sheet. See also chapter “Programming Hints” for some general register settings.

Type of Usage	Register Name		(Symbol)	Register Address (decimal)		Function
				PeliCAN Mode	BasicCAN Mode	
Elements for selecting different operation modes	Mode		(MOD)	0	—	Sleep-, Acceptance Filter-, Self Test-, Listen Only- and Reset Mode selection
	Control		(CR)	—	0	Reset Mode selection in BasicCAN Mode
	Command		(CMR)	—	1	Sleep Mode command in BasicCAN Mode
	Clock Divider		(CDR)	31	31	Set-up of clock signal at CLKOUT (pin 7) selection of PeliCAN Mode, Comparator Bypass Mode, TX1 (pin 14) Output Mode
Elements for setting up the CAN communication	Acceptance	Code, Mask	(ACR) (AMR)	16-19 20-23	4, 5	Selection of bit patterns for Acceptance Filtering
	Bus Timing	0 1	(BTR0) (BTR1)	6 7	6 7	Set-up of Bit Timing Parameters
	Output Control		(OCR)	8	8	Selection of Output Driver properties
Basic elements for the CAN communication	Command		(CMR)	1	1	Commands for Self Reception, Clear Data Overrun, Release Receive Buffer, Abort Transmission and Transmission Request
	Status		(SR)	2	2	Status of message buffers, status of CAN Core Block
	Interrupt		(IR)	3	3	CAN Interrupt flags
	Interrupt Enable		(IER)	4	—	Enable/disable of interrupt events in PeliCAN Mode
	Control		(CR)	—	0	Enable/disable of interrupt events in BasicCAN Mode

Table 4-6 : Registers of SJA1000

Type of Usage	Register Name	(Symbol)	Register Address (decimal)		Function
			PeliCAN Mode	BasicCAN Mode	
Elements for a comprehensive error detection and analyzing	Arbitration Lost Capture	(ALC)	11	—	Shows bit position, where arbitration was lost
	Error Code Capture	(ECC)	12	—	Shows last error type and location
	Error Warning Limit	(EWLR)	13	—	Selection of threshold for generating an Error Warning Interrupt
	RX Error Counter	(RXERR)	14	—	Reflects the current value of the Receive Error Counter
	TX Error Counter	(TXERR)	14, 15	—	Reflects the current value of the Transmit Error Counter
	Rx Message Counter	(RMC)	29	—	Number of messages in the Receive FIFO
	Rx Buffer Start Addr.	(RBSA)	30	—	Shows the current internal RAM address of the message available in the Receive Buffer
Message buffers	Transmit Buffer	(TXBUF)	16-28	10-19	
	Receive Buffer	(RXBUF)	16-28	20-29	

Table 4-7 : Registers of the SJA1000 (cont.)

4.6 Local Software Reset

A Local Software Reset signal may be used to reset the on board local logic.

The local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the Miscellaneous Control Register CNTRL (offset 0x50) in the PCI Controller Register Space.

CNTRL[30] PCI Adapter Software Reset:

Value of 1 issues a reset to the local logic. The local logic remains in this reset condition until the PCI Host clears the bit. The contents of the PCI Controller Configuration Registers are not reset.

5 Programming Hints

5.1 SJA1000 CAN Controller

5.1.1 SJA1000 CAN Controller

The SJA1000 clock input frequency is 16 MHz (for both SJA1000 controllers).

See chapter “SJA1000 CAN Controller Registers” for an overview of all registers in the different modes. Note that some registers are available in PeliCAN Mode only and that the Control Register is available in BasicCAN Mode only. Furthermore some registers are read only or write only and some can be accessed during Reset Mode only.

A transmit message has to be written to the transmit buffer. After a successful reception the microprocessor may read the received message from the receive buffer and then release it for further use.

5.1.2 Operating Modes

For register access, two different modes have to be distinguished:

- Reset Mode
- Operating Mode

The Reset Mode (see SJA1000 Control Register (CR; 0x0) for BasicCAN or Mode Register (MOD; 0x0) for PeliCAN, bit Reset Request) is entered automatically after a hardware-reset or when the controller enters the bus-off state (see Status Register, bit Bus Status).

The operating mode is activated by resetting of the reset request bit in the control register.

5.1.3 Hardware Related Configuration Registers

The SJA1000 Output Control Register and Clock Divider Register have to be programmed as follows (SJA1000 controller must be in Reset Mode):

Bit	Symbol	Description
7	OCTP1	11 : Push-Pull output stage
6	OCTN1	
5	OCPOL1	0 : Normal polarity
4	OCTP0	11 : Push-Pull output stage
3	OCTN0	
2	OCPOL0	0 : Normal polarity
1	OCMODE1	01 : Test output mode (bit reflection) 10 : Normal output mode
0	OCMODE0	

Table 5-1 : Output Control Register (OCR; 0x08)

Bit	Symbol	Description
7	CAN Mode	0 : BasicCAN Mode 1 : PeliCAN Mode
6	CBP	1 : Bypass input comparator, use RX0 only
5	RXINTEN	0 : Disable interrupts on TX1 output
4	-	0
3	clock off	1 : Disable clock output (not used)
2	CD.2	0
1	CD.1	0
0	CD.0	0

Table 5-2 : Clock Divider Register (CDR; 0x1F)

5.1.4 Integrated Data Buffer

The data to be transmitted on the CAN bus is loaded into the memory area of the SJA1000, called “Transmit Buffer”. The data received from the CAN bus is stored in the memory area of the SJA1000, called “Receive Buffer”. These buffers contain 2, 3 or 5 bytes for the identifier and frame information (dependent on mode and frame type) and up to 8 data bytes.

- BasicCAN Mode: The buffers are 10 bytes deep (see figure “Rx- and Tx-buffer in BasicCAN Mode”).
  - o 2 identifier bytes
  - o up to 8 data bytes
- PeliCAN Mode: The buffers are 13 bytes deep (see figure “Rx- and Tx-buffer in PeliCAN Mode”).
  - o 1 byte for frame information
  - o 2 or 4 identifier bytes (Standard Frame or Extended Frame)
  - o up to 8 data bytes

Address	Name	Composition and Remarks
Tx-buffer: 0x0A Rx-buffer: 0x14	Identifier Byte 1	8 Identifier bits
Tx-buffer: 0x0B Rx-buffer: 0x15	Identifier Byte 2	3 Identifier bits, 1 Remote Transmission Request bit, 4 bits for the Data Length Code, indicating the amount of data bytes
Tx-buffer: 0x0C-0x13 Rx-buffer: 0x16-0x1D	Data Byte 1 - 8	Up to 8 data bytes as indicated by the Data Length Code

Table 5-3 : Rx- and Tx-buffer in BasicCAN Mode

Address	Name	Composition and Remarks
0x10	Frame Information	1 bit indicating, if the message contains a Standard or Extended frame 1 Remote Transmission Request bit 4 bits for the Data Length Code, indicating the amount of data bytes
0x11, 0x12	Identifier Byte 1, 2	Standard Frame: 11 Identifier bits Extended Frame: 16 Identifier bits
0x13, 0x14	Identifier Byte 3, 4	Extended Frame only: 13 Identifier bits
Frame type Standard: 0x13 – 0x1A Extended: 0x15 – 0x1C	Data Byte 1 - 8	Up to 8 data bytes as indicated by the Data Length Code

Table 5-4 : Rx- and Tx-buffer in PeliCAN Mode

The whole Receive FIFO (64 bytes) can be accessed using CAN addresses 32 to 95.

A read access of the Tx-buffer can be done using CAN addresses 96 to 108.

For more information about the registers with respect to read and/or write access, bit definition and reset values, please consult the SJA1000 CAN Controller data sheet.

6 Configuration Hints

6.1 Transceiver Silent Mode

The CAN transceivers can be switched to Silent Mode, in this mode the transmitter is disabled. The S pins of the TJA1050 CAN transceivers are directly controlled by two GPIO outputs of the PCI Controller. The level on these GPIO lines can be changed by setting bit 5 for channel 1 or bit 26 for channel 2 in the General Purpose I/O Control Register (offset 0x54):

Value of GPIO Data	Function
0	Transceiver is in high-speed mode, which is the normal operating mode
1	Transceiver is in silent mode, transmitter is disabled

Table 6-1 : Transceiver Silent Mode Settings

Default value after power on is '0' (operating mode).

6.2 DIP Switch Settings

The following describes the DIP switch settings for one CAN channel. Possible line configuration options for each channel are:

- On board Line Termination: on / off
- P14 Bus Mode : connected / not connected and pass through/bus end

The on board termination option for a CAN channel node input (see P14 I/O pin assignment) is a 120 ohms split termination network.

For the pass through option, the I/O lines are passed through from the node input pins to the node output pins of the P14 I/O connector. Whereas in the bus end mode the I/O lines are NOT passed through and the node input pins must be used to connect the CAN bus lines. Note that on TPMC810-20R the pass through option is not applicable and only the bus end mode is available (see P14 Back I/O pin assignment).

Switches	Function	Setting	Description
S1,S2	Line Termination	ON	Line termination enabled
		OFF	Line termination disabled
S3,S4	P14 Connection	ON	Incoming CAN bus connection enabled
		OFF	Incoming CAN bus connection disabled
S5,S6	P14 Pass Through	ON	Outgoing CAN bus connection enabled
		OFF	Outgoing CAN bus connection disabled

Table 6-2 : DIP Switch Settings

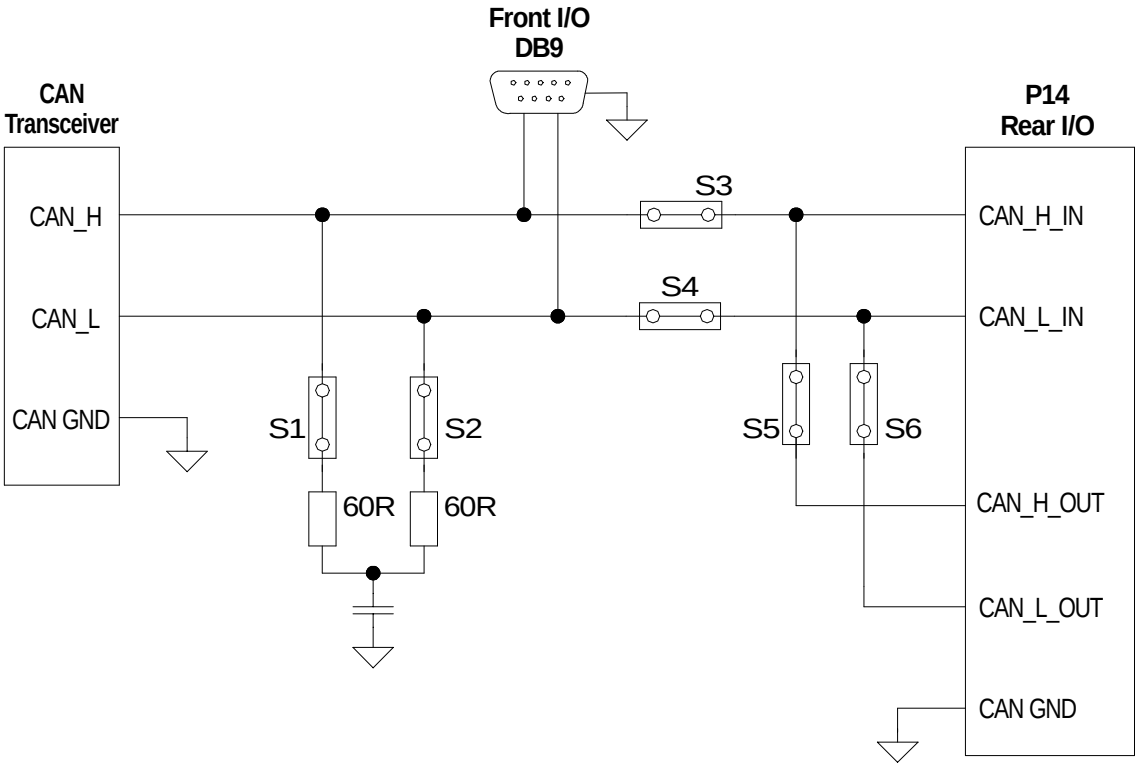

Figure 6-1 : CAN Channel Interface

7 Pin Assignment – I/O Connector

7.1 Front Panel I/O

Pin	Signal
1	NC
2	CAN1_L
3	CAN1_GND
4	NC
5	NC
6	CAN1_GND
7	CAN1_H
8	NC
9	NC

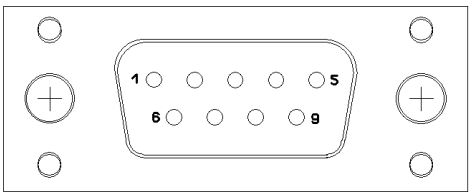

Table 7-1 : DB9 Male Connector X1 Channel 1

Pin	Signal
1	NC
2	CAN2_L
3	CAN2_GND
4	NC
5	NC
6	CAN2_GND
7	CAN2_H
8	NC
9	NC

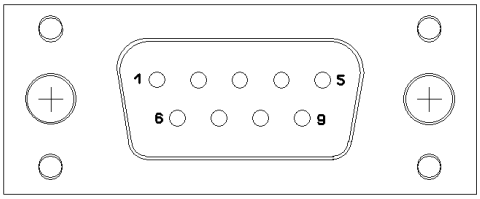

Table 7-2 : DB9 Male Connector X2 Channel 2

Note that the I/O circuits of both CAN ports are electrically isolated from the main system and also from each other.

The CAN ports may be used with isolated CAN networks as well as with non-isolated CAN networks.

In either case the CAN I/O ground signals are isolated from system ground and require a proper connection to the common ground of the CAN network they are connected too.

7.2 Back I/O P14 – TPMC810-10R

Pin	Signal
1	NC
2	CAN Channel 1 Ground
3	CAN Channel 1 Low Level (input for path-through option)
4	CAN Channel 1 High Level (input for path-through option)
5	CAN Channel 1 Ground
6	CAN Channel 1 Ground
7	CAN Channel 1 Low Level Out
8	CAN Channel 1 High Level Out
9	NC
10	NC
11	NC
12	NC
13	NC
14	NC
15	NC
16	CAN Channel 2 Ground
17	CAN Channel 2 Low Level (input for path-through option)
18	CAN Channel 2 High Level (input for path-through option)
19	CAN Channel 2 Ground
20	CAN Channel 2 Ground
21	CAN Channel 2 Low Level Out
22	CAN Channel 2 High Level Out
23	CAN Channel 2 Ground
24 ... 64	NC

Table 7-3 : Pin Assignment P14 Back I/O Connector – TPMC810-10R

7.3 Back I/O P14 – TPMC810-20R

Pin	Signal
1	NC
2	CAN Channel 1 Ground
3	CAN Channel 1 Low Level (input/output)
4	CAN Channel 1 High Level (input/output)
5	CAN Channel 1 Ground
6	NC
7	NC
8	NC
9	NC
10	NC
11	CAN Channel 2 Ground
12	CAN Channel 2 Low Level (input/output)
13	CAN Channel 2 High Level (input/output)
14	CAN Channel 2 Ground
15	NC
16 ... 64	NC

Table 7-4: Pin Assignment P14 Back I/O Connector – TPMC810-20R

Note that the I/O circuits of both CAN ports are electrically isolated from the main system and also from each other.

The CAN ports may be used with isolated CAN networks as well as with non-isolated CAN networks.

In either case the CAN I/O ground signals are isolated from system ground and require a proper connection to the common ground of the CAN network they are connected too.