The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC813

LON Interface

Version 1.0

User Manual

Issue 1.2

September 2006

D76813800

TEWS TECHNOLOGIES GmbH
Am Bahnhof 7
25469 Halstenbek, Germany
www.tews.com
Phone: +49-(0)4101-4058-0
Fax: +49-(0)4101-4058-19
e-mail: info@tews.com

TEWS TECHNOLOGIES LLC
9190 Double Diamond Parkway,
Suite 127, Reno, NV 89521, USA
www.tews.com
Phone: +1 (775) 850 5830
Fax: +1 (775) 201 0347
e-mail: usasales@tews.com

TPMC813-10

LON interface RS485

TPMC813-30

LON interface FTT-10A

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	January 2000
1.1	General Revision	May 2003
1.2	New address TEWS LLC	September 2006

Table of Contents

Table of Figures

1 Product Description

The TPMC813 is a standard single-width 32 bit PMC module providing a complete LON interface using the Neuron chip 3150. The communication is executed via a 4 Kbytes Dual Port RAM. A 32 Kbytes EPROM is used to store the protocol firmware of the Neuron chip 3150 and the application program.

Two kinds of on board physical interface are available: the TPMC813-10 supports standard RS485 and the TPMC813-30 provides the free topology twisted pair interface based on the ECHELON FTT-10A transceiver.

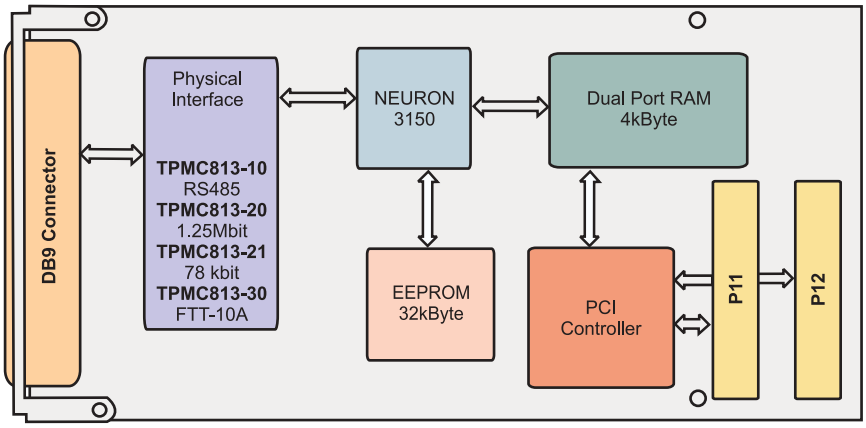

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI Rev. 2.1 compliant 33MHz / 32bit PCI 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	PCI9050-1 (PLX Technology)	
Firmware	MIP/DPR from ECHELON in EPROM, Run Time License included	
I/O Interface		
Interface Type	TPMC813-10: 1LON port, RS485 TPMC813-30: 1LON port, FTT-10A Transceiver	
I/O Connector	DB9 connector	
Physical Data		
Power Requirements	285mA typical @ +5V DC	
Temperature Range	Operating Storage	-40 °C to +85 °C -55°C to +125°C
MTBF	TPMC813-10: 363274 h TPMC813-30: 389994 h	
Humidity	5 – 95 % non-condensing	
Weight	75 g	

Figure 2-1 : Technical Specification

3 Local Space Addressing

3.1 PCI9050 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9050 local spaces.

PCI9050 Local Space	PCI9050 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	0 (0x10)	MEM	128	32	LITTLE	Local Configuration Registers
1	1(0x14)	I/O	128	32	LITTLE	Local Configuration Registers
2	2 (0x18)	MEM	4096	8	BIG (lower lane)	Local Address Space 0
3	3 (0x1C)	MEM	16	8	BIG (lower lane)	Local Address Space 1
4	4 (0x20)	-	-	-	-	Local Address Space 2
5	5 (0x24)	-	-	-	-	Local Address Space 3
6	6 (0x30)	-	-	-	-	Local Expansion ROM Space

Figure 3-1 : PCI9050 Local Space Configuration

3.2 Local Address Space 0

PCI Base Address: PCI9050 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space).

The Dual Port RAM memory is accessible through the Local Address Space 0 of the PMC module.

Offset / Register Offset	Register Name	Access Type	Register Width
0x0000-0x0FFF	4k Dual Port RAM	R/W	8 bit

Figure 3-2 : Local Memory Space 1

TPMC813 is designed for a byte read/write access. A word or long word access will fail.

3.2.1 Dual Port RAM

The TPMC813 has a 4k x 8 Dual Ported RAM. This RAM is used to exchange messages and commands between the host software and the MIP/DPR firmware, which is running on the TPMC813. The data structures are initialized by the MIP/DPR firmware as defined in the Microprocessor Interface Program (MIP) User's Guide of ECHELON.

3.3 Local Address Space 1

PCI Base Address: **PCI9050 PCI Base Address 2 (Offset 0x1C in PCI Configuration Space).**

Offset to PCI Base Address 2	Register Name	Access Type	Size (Bit)
0x0000	SEMMAPHORE FLAG 0	R/W	8
0x0001	SEMMAPHORE FLAG 1	R/W	8
0x0002	SEMMAPHORE FLAG 2	R/W	8
0x0003	SEMMAPHORE FLAG 3	R/W	8
0x0004	SEMMAPHORE FLAG 4	R/W	8
0x0005	SEMMAPHORE FLAG 5	R/W	8
0x0006	SEMMAPHORE FLAG 6	R/W	8
0x0007	SEMMAPHORE FLAG 7	R/W	8
0x0008	Local Interrupt Control Register (LICREG)	W	8
0x0009	Local Interrupt Status Register (LISREG)	R/W	8
0x000A	Local Reset Register (LRESREG)	W	8

Figure 3-3 : Local Address Space 1

TPMC813 is designed for a byte (8bit) read/write access. A word or long word access will fail.

3.3.1 Semaphore Flag Registers

The Semaphore Flag Registers are implemented in the Dual Ported RAM device of the TPMC813. The MIP/DPR firmware of the TPMC813 uses these semaphores to synchronize the access to the data structures in the Dual Ported RAM between the host software and the MIP/DPR firmware. For more information please refer to Microprocessor Interface Program (MIP) User's Guide of ECHELON.

The value of the semaphore flag is stored in bit 0 of the read data byte.

3.3.2 Local Interrupt Control Register (LICREG)

The Interrupt Control Register is used to control the interrupt generation.

Bit	Symbol	Description	Access	Reset Value
7:1		Not used and undefined during reads		
0		1 = interrupt enabled 0 = interrupt disabled MIP/DPR firmware can generate an interrupt to indicate the transfer of messages. The interrupt will occur at pin INTA# of the PCI bus.	W	0

Figure 3-4 : Interrupt Control Register (LICREG)

The LICREG is cleared to '0' after power-on or reset.

3.3.3 Local Interrupt Status Register (LISREG)

The Interrupt Status Register is used to decode the interrupt type.

Bit	Symbol	Description	Access	Reset Value
7:2		Not used and undefined during reads		
1		If Neuron chip causes a reset 1 = reset 0 = run Bit is cleared by writing '0x02' to the LISREG address 0x1009.	R/W	0
0		If Neuron chip causes an interrupt 1 = interrupt 0 = run Bit is cleared by writing '0x01' to the LISREG address 0x1009.	R/W	0

Figure 3-5 : Interrupt Status Register (LISREG)

The LISREG is cleared to '0' after power-on or reset.

3.3.4 Local Reset Register (LRESREG)

The Local Reset Register LRESREG can be used to initiate a reset of the local side of the TPMC813 under control of the host software.

Bit	Symbol	Description	Access	Reset Value
7:1		Not used and undefined during reads		
0		1 = active local reset 0 = run The local reset remains active until this bit is cleared by the host software.	W	

Figure 3-6 : Local Reset Register (LRESREG)

The LRESREG is cleared to '0' after power-on or reset. A local reset will restart the MIP/DPR firmware of the TPMC813.

4 PCI9050 Target Chip

4.1 PCI Configuration Registers (CFG)

4.1.1 PCI9050 Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	032D 1498
0x04	Status		Command		Y	0280 0000
0x08	Class Code			Revision ID	N	028000 XX
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers				Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers				Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0				Y	FFFFF000
0x1C	PCI Base Address 3 for Local Address Space 1				Y	FFFFFFF0
0x20	PCI Base Address 4 for Local Address Space 2				Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3				Y	00000000
0x28	PCI Cardbus Information Structure Pointer				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	000A 1498
0x30	PCI Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved			New Cap. Ptr.	N	000000 00
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00

Figure 4-1 : PCI9050 Header TPMC813-10

4.1.2 PCI Base Address Initialization

PCI Base Address Initialization is scope of the PCI host software.

PCI9050 PCI Base Address Initialization:

1. Write 0xFFFF_FFFF to the PCI9050 PCI Base Address Register.
2. Read back the PCI9050 PCI Base Address Register.
3. For PCI Base Address Registers 0:5, check bit 0 for PCI Address Space.

   Bit 0 = '0' requires PCI Memory Space mapping

   Bit 0 = '1' requires PCI I/O Space mapping

   For the PCI Expansion ROM Base Address Register, check bit 0 for usage.

   Bit 0 = ‘0’: Expansion ROM not used

   Bit 0 = ‘1’: Expansion ROM used
4. For PCI I/O Space mapping, starting at bit location 2, the first bit set determines the size of the required PCI I/O Space size.

   For PCI Memory Space mapping, starting at bit location 4, the first bit set to '1' determines the size of the required PCI Memory Space size.

   For PCI Expansion ROM mapping, starting at bit location 11, the first bit set to '1' determines the required PCI Expansion ROM size.

   For example, if bit 5 of a PCI Base Address Register is detected as the first bit set to ‘1’, the PCI9050 is requesting a 32 byte space (address bits 4:0 are not part of base address decoding).
5. Determine the base address and write the base address to the PCI9050 PCI Base Address Register. For PCI Memory Space mapping the mapped address region must comply with the definition of bits 3:1 of the PCI9050 PCI Base Address Register.

After programming the PCI9050 PCI Base Address Registers, the software must enable the PCI9050 for PCI I/O and/or PCI Memory Space access in the PCI9050 PCI Command Register (Offset 0x04). To enable PCI I/O Space access to the PCI9050, set bit 0 to '1'. To enable PCI Memory Space access to the PCI9050, set bit 1 to '1'.

For more information please refer to the PCI9050-1 data sheet which is part of the TMPC813-ED Engineering Documentation.

4.2 Local Configuration Register (LCR)

After reset, the PCI9050 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9050 Local Configuration Registers is:

PCI9050 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9050 PCI Configuration Register Space) or

PCI9050 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9050 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9050 Local Configuration Registers.

Offset from PCI Base Address	Register	Value
0x00	Local Address Space 0 Range	0x0FFF_F000
0x04	Local Address Space 1 Range	0x0FFF_FFF0
0x08	Local Address Space 2 Range	0x0000_0000
0x0C	Local Address Space 3 Range	0x0000_0000
0x10	Local Exp. ROM Range	0x0000_0000
0x14	Local Re-map Register Space 0	0x0000_0001
0x18	Local Re-map Register Space 1	0x0000_1001
0x1C	Local Re-map Register Space 2	0x0000_0000
0x20	Local Re-map Register Space 3	0x0000_0000
0x24	Local Re-map Register ROM	0x0000_0000
0x28	Local Address Space 0 Descriptor	0x2921_50C2
0x2C	Local Address Space 1 Descriptor	0x2921_50C2
0x30	Local Address Space 2 Descriptor	0x0000_0000
0x34	Local Address Space 3 Descriptor	0x0000_0000
0x38	Local Exp. ROM Descriptor	0x0000_0000
0x3C	Chip Select 0 Base Address	0x0000_0801
0x40	Chip Select 1 Base Address	0x0000_1009
0x44	Chip Select 2 Base Address	0x0000_0000
0x48	Chip Select 3 Base Address	0x0000_0000
0x4C	Interrupt Control/Status	0x0000_0043
0x50	Miscellaneous Control Register	0x0078_0000

Figure 4-2 : PCI9050 Local Configuration Register

4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9050 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x0F : PCI9050 PCI Configuration Register Values
- Address 0x10 to 0x64 : PCI9050 Local Configuration Register Values
- Address 0x65 to 0x7C : Not used
- Address 0x7E + 0x7F : TPMC variant

See the PCI9050 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x032D	0x1498	0x0280	0x0000	s.b.	0x1498	0x0000	0x0100
0x10	0x0FFF	0xF000	0x0FFF	0xFFF0	0x0000	0x0000	0x0000	0x0000
0x20	0x0000	0x0000	0x0000	0x0001	0x0000	0x1001	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x2921	0x50C2	0x2921	0x50C2
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0801
0x50	0x0000	0x1009	0x0000	0x0000	0x0000	0x0000	0x0000	0x0043
0x60	0x0078	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x70	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	s.b.

Figure 4-3 : Configuration EEPROM TPMC813-xx

Subsystem-ID Value (Offset 0x08):	TPMC813-10	0x000A
	TPMC813-30	0x001E
Subsystem-ID Value (Offset 0x7E):	TPMC813-10	0x000A
	TPMC813-30	0x001E

For more information please refer to the PCI9050-1 data sheet which is part of the TPMC813-ED Engineering Documentation.

4.4 Local Software Reset

The PCI9050 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9050 local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9050 local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of '1' resets the PCI9050 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9050 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9050 PCI and Local Configuration Registers are not reset. The PCI9050 PCI Interface is not reset.

4.5 Big / Little Endian

- PCI – Bus (Little Endian)

Byte 0	AD[7..0]
Byte 1	AD[15..8]
Byte 2	AD[23..16]
Byte 3	AD[31..24]

- Every Local Address Space (0...3) and the Expansion ROM Space can be programmed to operate in Big or Little Endian Mode.

Big Endian		**Little Endian**	
32 Bit		**32 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
Byte 2	D[15..8]	Byte 2	D[23..16]
Byte 3	D[7..0]	Byte 3	D[31..24]
16 Bit upper lane		**16 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
16 Bit lower lane			
Byte 0	D[15..8]		
Byte 1	D[7..0]		
8 Bit upper lane		**8 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
8 Bit lower lane			
Byte 0	D[7..0]		

Figure 4-4 : Local Bus Little/Big Endian

Standard use of the TPMC813:

Local Address Space 0	8 bit bus in Big Endian Mode
Local Address Space 1	8 bit bus in Big Endian Mode
Local Address Space 2	not used
Local Address Space 3	not used
Expansion ROM Space	not used

To change the Endian Mode use the Local Configuration Registers for the corresponding Space. Bit 24 of the according register sets the mode. A value of 1 indicates Big Endian and a value of 0 indicates Little Endian.

For further information please refer to the PCI9050 manual which is also part of the TPMC813-ED Engineering Documentation.

Use the PCI Base Address 0 + Offset or PCI Base Address 1 + Offset:

Short cut Offset	Name	
LAS0BRD	0x28	Local Address Space 0 Bus Region Description Register
LAS1BRD	0x2C	Local Address Space 0 Bus Region Description Register
LAS2BRD	0x30	Local Address Space 0 Bus Region Description Register
LAS3BRD	0x34	Local Address Space 0 Bus Region Description Register
EROMBRD	0x38	Expansion ROM Bus Region Description Register

You could also use the PCI - Base Address 1 I/O Mapped Configuration Registers.

4.5.1 PCI Interrupt Control/Status Register

The Neuron chip can generate an interrupt at pin INTA# of the PCI bus. The interrupt status can be read at the Interrupt Status Register INTCSR of the PCI Controller PCI9050-1.

Bit	Description	Access	Reset Value
31:8	unused	R	0
7	Software Interrupt	R/W	0
6	PCI Interrupt Enable	R/W	1
5	Local Interrupt 2 Status	R	0
4	Local Interrupt 2 Polarity	R/W	0
3	Local Interrupt 2 Enable	R/W	0
2	Local Interrupt 1Status	R	0
1	Local Interrupt 1 Polarity	R/W	1
0	Local Interrupt 1 Enable	R/W	1

Figure 4-5 : Interrupt Control/Status Register (INTCSR; 0x4C)

5 Installation

5.1 Jumper Configuration

The jumper block J1 configures the termination of the TPMC813-30.

Termination	1-3	2-4
Termination with 52.5 ohms for Singly Terminated Bus Topology	close	close
Termination with 105 ohms for Singly Terminated Bus Topology	open	close
Termination with 105 ohms for Doubly Terminated Bus Topology	close	open
No termination on board **(factory setting)**	**open**	**open**

The jumper block J2 configures the termination of the TPMC813-10.

Termination	1-2	3-4
Termination with a R / C network	close	close
No termination on board **(factory setting)**	**open**	**open**

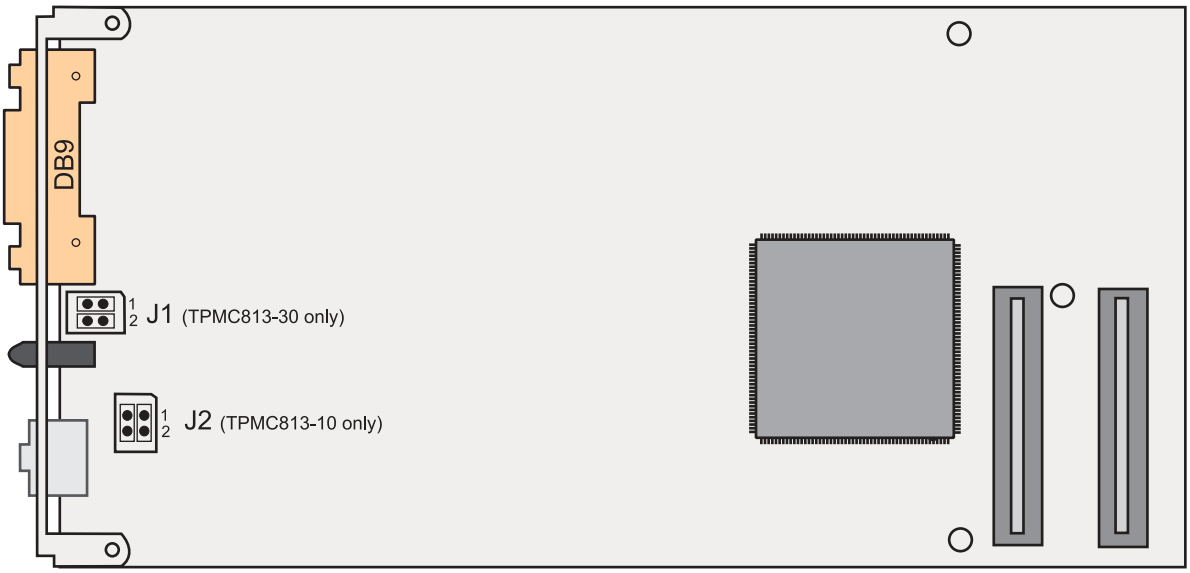

Figure 5-1 : Jumper Configuration

5.2 Service LED / Service Request Button

The firmware flashes the Service LED at a ½ Hz rate if the TPMC813 has not been configured with network address information. Pressing the Service Request Button causes the TPMC813 to transmit a network management message containing its 48 bit unique ID on the network.

Node State	Service LED
Without application and without configuration	On
Without configuration (but with an application)	Flashing
Configured, Hard Off-Line	Off
Configured	Off

Figure 5-2 : Service LED

6 Pin Assignment – I/O Connector

6.1 Front panel DB9 female Connector

Pin	Signal	Level
	TPMC813-10 / RS485	**TPMC813-30 / FTT-10A**
1	LON DATA +	LON NET A
2	LON DATA -	LON NET B
3	NC	NC
4	NC	NC
5	NC	NC
6	Case Ground	Case Ground
7	SERVICE#	SERVICE#
8	Ground	Ground
9	+5V, 1.1A maximum (fused)	+5V, 1.1A maximum (fused)

Figure 6-1 : DB9 female connector