The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC868

16 Channel

Asynchronous Serial Interface

Version 1.0

User Manual

Issue 1.0.7

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TPMC868-10R

16 channel asynchronous serial interface RS232, front panel I/O and back I/O

TPMC868-11R

16 channel asynchronous serial interface RS422, front panel I/O and back I/O

TPMC868-10R-ET

16 channel asynchronous serial interface RS232, front panel I/O and back I/O, extended temperature range

TPMC868-11R-ET

16 channel asynchronous serial interface RS422, front panel I/O and back I/O, extended temperature range

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	July 2000
1.1	Technical Specification Update (TPMC868-11) & General Revision	April 2003
1.2	Correction Module Number	July 2003
1.3	Baud Rate Programming Note Update	December 2003
1.4	Added Module Versions TPMC868-xx-ET	May 2004
1.5	New address TEWS LLC	September 2006
1.0.6	New Notation for User Manual and Engineering Documentation	July 2009
1.0.7	General Revision	August 2014

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1 Product Description

The TPMC868 is a standard single-width 32 bit PMC module and offers 16 channels of high performance serial interface.

Two modules options are available:

- The TPMC868-10R provides 16 RS232 channels with front panel I/O and P14 I/O supporting RxD, TxD, RTS, CTS and GND per channel.
- The TPMC868-11R provides 16 RS422 channels with front panel I/O and P14 I/O supporting RxD+/-, TxD+/- and GND per channel.

Each channel has a 64 byte transmit FIFO and a 64 byte receive FIFO to significantly reduce the overhead required to provide data to and get data from the transmitters and receivers. The FIFO trigger level is programmable.

The baud rate is individually programmable for up to 230 kbaud. All serial channels use ESD protected transceivers up to +/-15KV according to IEC 1000-4-2.

All TPMC868 modules are available in extended temperature range as TPMC868-xxR-ET versions.

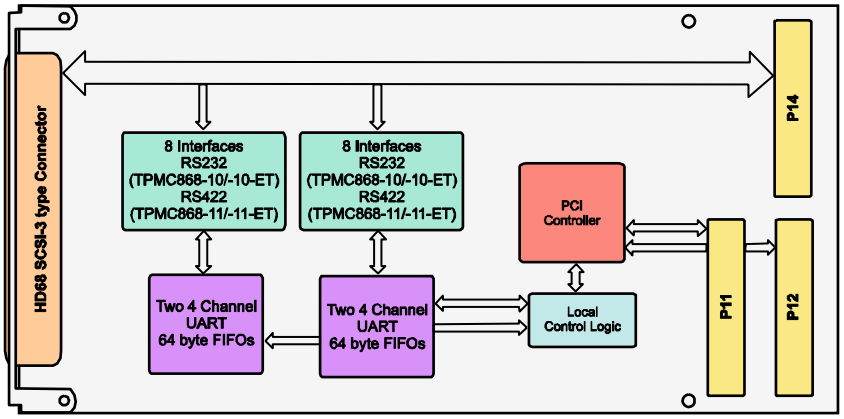

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI Rev. 2.1 compliant 33 MHz / 32 bit PCI 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	PCI9050-1 (PLX Technology)	
UART Type	16C654 Quad UART (4 x) (Exar)	
I/O Transceivers	TPMC868-10R: MAX3225E (or equivalent) (ESD protected) TPMC868-11R: MAX490E (or equivalent) (ESD protected)	
I/O Interface		
Interface Type	Asynchronous serial interface	
Number of Channels	16	
Physical Interface	TPMC868-10R: RS232 TPMC868-11R: RS422	
Serial Channel I/O Signals	TPMC868-10R: TXD, RXD, RTS#, CTS# TPMC868-11R: TXD+, TXD-, RXD+, RXD- (on board termination)	
I/O Connector	HD68 SCSI-3 type connector (e.g. AMP# 787082) PMC P14 I/O (64 pin Mezzanine Connector)	
Physical Data		
Power Requirements	TPMC868-10R: 16mA @+3.3V DC (max. without load) 350mA @+5V DC (max.) TPMC868-11R: 125mA @+3.3V DC (max.) 300mA @+5V DC (max. without load)	
Temperature Range	Operating Storage	0°C to +70 °C (TPMC868-10R/-11R) -40°C to +85°C (TPMC868-xxR-ET) -40°C to +85°C
MTBF	TPMC868-10R: 157653h TPMC868-11R: 166965h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	78 g	

Table 2-1 : Technical Specification

3 Local Space Addressing

3.1 PCI9050 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9050 local spaces.

PCI9050 Local Space	PCI9050 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	0 (0x10)	MEM	128	32	LITTLE	Local Configuration Registers
1	1 (0x14)	I/O	128	32	LITTLE	Local Configuration Registers
2	2 (0x18)	MEM	256	8	BIG	UART Register Space
3	3 (0x1C)	MEM	16	16	BIG	Interrupt Status Register Space

Table 3-1 : PCI9050 Local Space Configuration

3.2 UART Register Space

PCI Base Address: PCI9050 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space).

UART Register Space Region	PCI Address	Size (Bit)
Serial Channel 1 Register Set	PCI Base Address 2 + (0x0000 to 0x0007)	8
Serial Channel 2 Register Set	PCI Base Address 2 + (0x0008 to 0x000F)	8
Serial Channel 3 Register Set	PCI Base Address 2 + (0x0010 to 0x0017)	8
Serial Channel 4 Register Set	PCI Base Address 2 + (0x0018 to 0x001F)	8
Serial Channel 5 Register Set	PCI Base Address 2 + (0x0020 to 0x0027)	8
Serial Channel 6 Register Set	PCI Base Address 2 + (0x0028 to 0x002F)	8
Serial Channel 7 Register Set	PCI Base Address 2 + (0x0030 to 0x0037)	8
Serial Channel 8 Register Set	PCI Base Address 2 + (0x0038 to 0x003F)	8
Serial Channel 9 Register Set	PCI Base Address 2 + (0x0040 to 0x0047)	8
Serial Channel 10 Register Set	PCI Base Address 2 + (0x0048 to 0x004F)	8
Serial Channel 11 Register Set	PCI Base Address 2 + (0x0050 to 0x0057)	8
Serial Channel 12 Register Set	PCI Base Address 2 + (0x0058 to 0x005F)	8
Serial Channel 13 Register Set	PCI Base Address 2 + (0x0060 to 0x0067)	8
Serial Channel 14 Register Set	PCI Base Address 2 + (0x0068 to 0x006F)	8
Serial Channel 15 Register Set	PCI Base Address 2 + (0x0070 to 0x0077)	8
Serial Channel 16 Register Set	PCI Base Address 2 + (0x0078 to 0x007F)	8

UART Register Space Region	PCI Address	Size (Bit)
FIFO Ready Register CH1-CH4	PCI Base Address 2 + (0x0080)	8
FIFO Ready Register CH5-CH8	PCI Base Address 2 + (0x0084)	8
FIFO Ready Register CH9-CH12	PCI Base Address 2 + (0x0088)	8
FIFO Ready Register CH13-CH16	PCI Base Address 2 + (0x008C)	8

Table 3-2 : UART Register Space Overview

3.2.1 Serial Channel Register

The UART register space provides a register set of each of the 16 serial channels.

Register Set	Register Set Offset
SERIAL CHANNEL 1	0x0000
SERIAL CHANNEL 2	0x0008
SERIAL CHANNEL 3	0x0010
SERIAL CHANNEL 4	0x0018
SERIAL CHANNEL 5	0x0020
SERIAL CHANNEL 6	0x0028
SERIAL CHANNEL 7	0x0030
SERIAL CHANNEL 8	0x0038
SERIAL CHANNEL 9	0x0040
SERIAL CHANNEL 10	0x0048
SERIAL CHANNEL 11	0x0050
SERIAL CHANNEL 12	0x0058
SERIAL CHANNEL 13	0x0060
SERIAL CHANNEL 14	0x0068
SERIAL CHANNEL 15	0x0070
SERIAL CHANNEL 16	0x0078

Table 3-3 : Serial Channel Register Set Offset

Each Register Set provides the following 8 bit registers:

Register Symbol	Register Name
DLL	Baud Rate Divisor LSB
DLM	Baud Rate Divisor MSB
EFR	Enhanced Feature Register
FCR	FIFO Control Register
IER	Interrupt Enable Register
ISR	Interrupt Status Register
LCR	Line Control Register
LSR	Line Status Register
MCR	Modem Control Register
MSR	Modem Status Register
RHR	Receive Holding Register
SCPD	Scratchpad Register
THR	Transmit Holding Register
XON1	Xon-1 Word
XON2	Xon-2 Word
XOFF1	Xoff-1 Word
XOFF2	Xoff-2 Word

Table 3-4 : Serial Channel Register

The following table provides the register offsets within a register set, access types and access control:

Access Control	Register Offset								Access Type
	0x0	0x1	0x2	0x3	0x4	0x5	0x6	0x7	
LCR Bit 7 = 0	RHR		ISR	LCR		LSR	MSR	SCPD	READ
	THR	IER	FCR		MCR			SCPD	WRITE
LCR Bit 7 = 1 (but LCR ≠ 0xBF)	DLL	DLM							READ
	DLL	DLM							WRITE
LCR = 0xBF			EFR		Xon-1	Xon-1	Xoff-1	Xoff-1	READ
			EFR		Xon-2	Xon-2	Xoff-2	Xoff-2	WRITE

Table 3-5 : Serial Channel Register Offset and Access Control

The address for a serial channel *register x* **in a register set for** *channel y* **is:**

PCI Base Address 2 (PCI Base Address for the UART Register Space)

+ Register Set Offset for *channel y*

+ Register Offset for *register x*

Because some serial channel registers overlap in the UART device address space, further access control must be programmed to access those registers.

Some serial channel registers are write only or read only registers.

All serial channel registers are byte sized.

For a description of the serial channel registers please refer to the 16C654 UART (Exar) data sheet.

3.2.2 FIFO Ready Register

There are 4 UART FIFO Ready Registers. Each FIFO Ready Register provides status data for 4 serial channels.

Register	Description	PCI Address
FIFORDY1	FIFO Ready Register CH1-CH4	PCI Base Address 2 + (0x0080)
FIFORDY2	FIFO Ready Register CH5-CH8	PCI Base Address 2 + (0x0084)
FIFORDY3	FIFO Ready Register CH9-CH12	PCI Base Address 2 + (0x0088)
FIFORDY4	FIFO Ready Register CH13-CH16	PCI Base Address 2 + (0x008C)

Table 3-6 : FIFO Ready Register

The FIFO Ready Registers are byte wide read registers.

The FIFO Ready Registers provide real-time status of the serial channel transmit and receive FIFOs.

Each TX and RX channel has its own 64 byte FIFO. When any of the 8 TX/RX FIFOs becomes empty/full, the status bit associated with the TX/RX channel is set in the FIFO Ready Register.

Bit	Symbol	Description	Access	Reset Value
7	RXRDY4	Read as '1' : the receiver is ready and is filled to a level below the programmed trigger level. Read as '0' : the corresponding receive FIFO is filled to a level above the programmed trigger level or a time-out has occurred.	R	
6	RXRDY3			
5	RXRDY2			
4	RXRDY1			
3	TXRDY4	Read as '1' : one or more empty locations exist in the corresponding transmit FIFO. Read as '0' : the corresponding transmit FIFO is full. The channel will not accept any more transmit data.	R	
2	TXRDY3			
1	TXRDY2			
0	TXRDY1			

Table 3-7 : FIFORDY1 Register (CH1 - CH4)

Bit	Symbol	Description	Access	Reset Value
7	RXRDY8	Read as '1' : the receiver is ready and is filled to a level below the programmed trigger level. Read as '0' : the corresponding receive FIFO is filled to a level above the programmed trigger level or a time-out has occurred.	R	
6	RXRDY7			
5	RXRDY6			
4	RXRDY5			
3	TXRDY8	Read as '1' : one or more empty locations exist in the corresponding transmit FIFO. Read as '0' : the corresponding transmit FIFO is full. The channel will not accept any more transmit data.	R	
2	TXRDY7			
1	TXRDY6			
0	TXRDY5			

Table 3-8 : FIFORDY2 Register (CH5 - CH8)

Bit	Symbol	Description	Access	Reset Value
7	RXRDY12	Read as ‘1’ : the receiver is ready and is filled to a level below the programmed trigger level. Read as ‘0’ : the corresponding receive FIFO is filled to a level above the programmed trigger level or a time-out has occurred.	R	
6	RXRDY11			
5	RXRDY10			
4	RXRDY9			
3	TXRDY12	Read as ‘1’ : one or more empty locations exist in the corresponding transmit FIFO. Read as ‘0’ : the corresponding transmit FIFO is full. The channel will not accept any more transmit data.	R	
2	TXRDY11			
1	TXRDY10			
0	TXRDY9			

Table 3-9 : FIFORDY3 Register (CH9 - CH12)

	Symbol	Description	Access	Reset Value
7	RXRDY16	Read as ‘1’ : the receiver is ready and is filled to a level below the programmed trigger level. Read as ‘0’ : the corresponding receive FIFO is filled to a level above the programmed trigger level or a time-out has occurred.	R	
6	RXRDY15			
5	RXRDY14			
4	RXRDY13			
3	TXRDY16	Read as ‘1’ : one or more empty locations exist in the corresponding transmit FIFO. Read as ‘0’ : the corresponding transmit FIFO is full. The channel will not accept any more transmit data.	R	
2	TXRDY15			
1	TXRDY14			
0	TXRDY13			

Table 3-10: FIFORDY4 Register (CH13 - CH16)

3.3 Interrupt Status Register Space

PCI Base Address: PCI9050 PCI Base Address 3 (Offset 0x1C in PCI Configuration Space).

Interrupt Status Register Space	PCI Address	Size (Bit)
Interrupt Status Register	PCI Base Address 3+ 0x0000	16

Table 3-11: Interrupt Status Register Space

Bit	Symbol	Description	Access	Reset Value
15	INT_CH16	0 : No active interrupt request 1 : Active interrupt request	R	
14	INT_CH15			
13	INT_CH14			
12	INT_CH13			
11	INT_CH12			
10	INT_CH11			
9	INT_CH10			
8	INT_CH9			
7	INT_CH8			
6	INT_CH7			
5	INT_CH6			
4	INT_CH5			
3	INT_CH4			
2	INT_CH3			
1	INT_CH2			
0	INT_CH1			

Table 3-12: Interrupt Status Register

Each of the 16 serial channel interrupts is mapped to the Local Interrupt 1 of the PCI9050 (PCI Target Chip).

The PCI9050 (PCI Target Chip) maps the local interrupts to the PCI INTA interrupt line if PCI interrupts are enabled in the PCI9050 (PCI Target Chip) Interrupt Control Register.

If PCI interrupts are disabled in the PCI9050 (PCI Target Chip) Interrupt Control Register, the Interrupt Status Register can be used as a polling register for serial channel interrupts.

After Reset PCI interrupts are enabled in the PCI9050 (PCI Target Chip) Interrupt Control Register.

Each of the 16 serial channel interrupts can be enabled individually by the IER register in the UART register space.

After Reset all serial channel interrupts are disabled by the UART's IER register.

4 PCI9050 Target Chip

4.1 PCI Configuration Registers (PCR)

4.1.1 PCI9050 Header

PCI CFG Register Address	PCI9050 PCI Configuration Register				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	0364 1498
0x04	Status		Command		Y	0280 0000
0x08	Class Code			Revision ID	N	070200 00
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers				Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers				Y	FFFFFF81
0x18	PCI Base Address 2 for Local Address Space 0				Y	FFFFFF00
0x1C	PCI Base Address 3 for Local Address Space 1				Y	FFFFFFF0
0x20	PCI Base Address 4 for Local Address Space 2				Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3				Y	00000000
0x28	PCI Cardbus Information Structure Pointer				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	000A 1498 (-10R) 000B 1498 (-11R)
0x30	PCI Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved			New Cap. Ptr.	N	000000 00
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00

Table 4-1 : PCI9050 Header TPMC868

Device-ID : 0x0364 (TPMC868)

Vendor-ID : 0x1498 (TEWS TECHNOLOGIES)

4.1.2 PCI Base Address Initialization

PCI Base Address Initialization is scope of the PCI host software.

PCI9050 PCI Base Address Initialization:

- Write 0xFFFF_FFFF to the PCI9050 PCI Base Address Register.
- Read back the PCI9050 PCI Base Address Register.
- For PCI Base Address Registers 0:5, check bit 0 for PCI Address Space:

  Bit 0 = '0' requires PCI Memory Space mapping

  Bit 0 = '1' requires PCI I/O Space mapping

  For the PCI Expansion ROM Base Address Register, check bit 0 for usage:

  Bit 0 = ‘0’: Expansion ROM not used

  Bit 0 = ‘1’: Expansion ROM used

- Or PCI I/O Space mapping, starting at bit location 2, the first bit set determines the size of the required PCI I/O Space size.

  For PCI Memory Space mapping, starting at bit location 4, the first bit set to '1' determines the size of the required PCI Memory Space size.

  For PCI Expansion ROM mapping, starting at bit location 11, the first bit set to '1' determines the required PCI Expansion ROM size.

  For example, if bit 5 of a PCI Base Address Register is detected as the first bit set to ‘1’, the PCI9050 is requesting a 32 byte space (address bits 4:0 are not part of base address decoding).

- Determine the base address and write the base address to the PCI9050 PCI Base Address Register. For PCI Memory Space mapping the mapped address region must comply with the definition of bits 3:1 of the PCI9050 PCI Base Address Register.

  After programming the PCI9050 PCI Base Address Registers, the software must enable the PCI9050 for PCI I/O and/or PCI Memory Space access in the PCI9050 PCI Command Register (Offset 0x04). To enable PCI I/O Space access to the PCI9050, set bit 0 to '1'. To enable PCI Memory Space access to the PCI9050, set bit 1 to '1'.

4.2 Local Configuration Register (LCR)

After reset, the PCI9050 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9050 Local Configuration Registers is:

PCI9050 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9050 PCI Configuration Register Space), or

PCI9050 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9050 PCI Configuration Register Space)

Do not change hardware dependent bit settings in the PCI9050 Local Configuration Registers.

Offset from PCI Base Address	Register	Value
0x00	Local Address Space 0 Range	0x0FFF_FF00
0x04	Local Address Space 1 Range	0x0FFF_FFF0
0x08	Local Address Space 2 Range	0x0000_0000
0x0C	Local Address Space 3 Range	0x0000_0000
0x10	Local Exp. ROM Range	0x0000_0000
0x14	Local Re-map Register Space 0	0x0000_0001
0x18	Local Re-map Register Space 1	0x0000_0101
0x1C	Local Re-map Register Space 2	0x0000_0000
0x20	Local Re-map Register Space 3	0x0000_0000
0x24	Local Re-map Register ROM	0x0000_0000
0x28	Local Address Space 0 Descriptor	0x5501_40C0
0x2C	Local Address Space 1 Descriptor	0x5541_40C0
0x30	Local Address Space 2 Descriptor	0x0000_0000
0x34	Local Address Space 3 Descriptor	0x0000_0000
0x38	Local Exp. ROM Descriptor	0x0000_0000
0x3C	Chip Select 0 Base Address	0x0000_0081
0x40	Chip Select 1 Base Address	0x0000_0103
0x44	Chip Select 2 Base Address	0x0000_0000
0x48	Chip Select 3 Base Address	0x0000_0000
0x4C	Interrupt Control/Status	0x0000_0041
0x50	Miscellaneous Control Register	0x0078_04B2

Table 4-2 : PCI9050 Local Configuration Register

4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9050 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x0F : PCI9050 PCI Configuration Register Values
- Address 0x10 to 0x64 : PCI9050 Local Configuration Register Values
- Address 0x65 to 0x7C : Not used
- Address 0x7Eto 0x7F : TPMC variant

See the PCI9050 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x0364	0x1498	0x0702	0x0000	s.b.	0x1498	0x0000	0x0100
0x10	0x0FFF	0xFF00	0x0FFF	0xFFF0	0x0000	0x0000	0x0000	0x0000
0x20	0x0000	0x0000	0x0000	0x0001	0x0000	0x0101	0x0000	0x0000
0x30	0x0000	0x0000	0x0000	0x0000	0x5501	0x40C0	0x5541	0x40C0
0x40	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0081
0x50	0x0000	0x0103	0x0000	0x0000	0x0000	0x0000	0x0000	0x0041
0x60	0x0078	0x14B2	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x70	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	s.b.

Table 4-3 : Configuration EEPROM TPMC868-xxR

Subsystem-ID Value (Offset 0x08):	TPMC868-10R	0x000A
	TPMC868-11R	0x000B
Board Option Value (Offset 0x0E):	TPMC868-10R	0x000A
	TPMC868-11R	0x000B

4.4 PCI Interrupt Control/Status

PCI9050 PCI interrupts can be globally enabled / disabled by programming bit 6 of the PCI9050 Interrupt Control / Status Register (INTCSR) at offset 0x4C in the PCI9050 Local Configuration Register Space.

PCI Base Address for the PCI Memory mapped PCI9050 Local Configuration Register Space:
Offset 0x10 in the PCI9050 PCI Configuration Register Space.

INTCSR (Offset 0x4C) bit 6 = 0 disables PCI Interrupts, bit 6 = 1 enables PCI Interrupts.

4.5 Software Reset

The PCI9050 provides a Local Reset output (LRESET#) programmable in the PCI9050 Miscellaneous Control Register (CNTRL) at offset 0x50 in the PCI9050 Local Configuration Register Space.

PCI Base Address for the PCI Memory mapped PCI9050 Local Configuration Register Space: Offset 0x10 in the PCI9050 PCI Configuration Register Space.

CNTRL (Offset 0x50) bit 30 = 0 de-asserts the LRESET# output; bit 30 = 1 asserts the LRESET# output.

The PCI9050 LRESET# output is used to reset the on board local logic. The PCI9050 controller will also be partly reset by this bit. The contents of the PCI and local configuration registers will not be reset.

4.6 Local Space Byte Ordering

The byte ordering for the PCI9050 Local Spaces is programmable in the Local Space Descriptor Registers in the PCI9050 Local Configuration Register Space.

PCI Base Address for the PCI Memory mapped PCI9050 Local Configuration Register Space: Offset 0x10 in the PCI9050 PCI Configuration Register Space.

Offset for the Local Space 0 Descriptor Register: Offset 0x28

Offset for the Local Space 1 Descriptor Register: Offset 0x2C

In the Local Space Descriptor Registers bit 24 selects the local space byte ordering mode. A value of 1 indicates Big Endian; a value of 0 indicates Little Endian byte ordering.

5 Functional Description

For a detailed description of the UART functions please refer to the 16C654 data sheet (Exar).

6 Programming Hints

6.1 UART Baud Rate Programming

Each of the 16 serial channels of the TPMC868 provides a programmable Baud Rate Generator. The clock of the 16C654 UART can be divided by any divisor from 1 to 2^{16} – 1. The divisor can be programmed by the UART channel DLM (Divisor MSB) and DLL (Divisor LSB) registers. After reset bit 7 of the UART channels MCR register defaults to '0' and the divisor value is 0xFFFF.

The basic formula of baud rate programming is:

$$\frac{7.3728MHz}{16 * DIVISOR * (1 + 3 * MCR\_BIT7)}$$

Baud Rate MCR Bit 7 = 0	Baud Rate MCR Bit 7 = 1	Divisor	DLM Value	DLL Value
200	50	0x0900	0x09	0x00
300	75	0x0600	0x06	0x00
600	150	0x0300	0x03	0x00
1200	300	0x0180	0x01	0x80
2400	600	0x00C0	0x00	0xC0
4800	1200	0x0060	0x00	0x60
9600	2400	0x0030	0x00	0x30
19.2K	4800	0x0018	0x00	0x18
28.8K	7200	0x0010	0x00	0x10
38.4K	9600	0x000C	0x00	0x0C
76.8K	19.2K	0x0006	0x00	0x06
153.6K	38.4K	0x0003	0x00	0x03
230.4K	57.6K	0x0002	0x00	0x02
460.8K	115.2K	0x0001	0x00	0x01

Table 6-1 : UART Baud Rate Programming

Access to the DLM, DLL registers must be enabled in the LCR register.

These steps should be used to modify the DLM, DLL registers :

- **Write 0x80 to LCR register (enable access to DLM, DLL registers)**
- **Modify DLM, DLL registers**
- **Write normal operation byte value to LCR register**

The MCR (Modem Control Register) bits 5-7 must be enabled for modifying by setting EFR (Enhanced Feature Register) bit 4.

These steps should be used to modify MCR bit 7 :

- **Write 0xBF to LCR register (enable access to EFR register)**
- **Set EFR register bit 4 to '1' (enable modification of MCR bits 5-7)**
- **Write 0x00 to LCR register (enable access to MCR register)**
- **Modify MCR bit 7**
- **Write 0xBF to LCR register (enable access to EFR register)**
- **Set EFR register bit 4 to '0' (Latch MCR bit setting)**
- **Write normal operation byte value to LCR register**

7 Installation Hints

Connect channel I/O either to front I/O or P14 back I/O at a time. Do not connect an I/O channel to both front I/O connector and P14 back I/O connector at the same time.

There is no GND signal present on the P14 back I/O connector. Make sure that back I/O connected systems are using the same ground as the TPMC868 system.

The TPMC868-11R (RS422) provides on board termination resistors. Do not apply additional external termination resistors here.

Please note that on the TPMC868-10R and TPMC868-11R, the P14 back I/O connector is always populated and connected to on board logic. Do not use these modules on carrier boards where P14/J14 is reserved for other system signals but PMC I/O. Ask support for special board options with front I/O only in this case.

8 Pin Assignment I/O Connector

8.1 TPMC868-10R Front Panel I/O Connector

Pin	Signal	Description	Direction	Level
1	TXD[00]	Transmit Data Serial Channel 1	Output	RS232
2	RTS#[00]	Request To Send Serial Channel 1	Output	RS232
3	TXD[01]	Transmit Data Serial Channel 2	Output	RS232
4	RTS#[01]	Request To Send Serial Channel 2	Output	RS232
5	TXD[02]	Transmit Data Serial Channel 3	Output	RS232
6	RTS#[02]	Request To Send Serial Channel 3	Output	RS232
7	TXD[03]	Transmit Data Serial Channel 4	Output	RS232
8	RTS#[03]	Request To Send Serial Channel 4	Output	RS232
9	GND			
10	TXD[04]	Transmit Data Serial Channel 5	Output	RS232
11	RTS#[04]	Request To Send Serial Channel 5	Output	RS232
12	TXD[05]	Transmit Data Serial Channel 6	Output	RS232
13	RTS#[05]	Request To Send Serial Channel 6	Output	RS232
14	TXD[06]	Transmit Data Serial Channel 7	Output	RS232
15	RTS#[06]	Request To Send Serial Channel 7	Output	RS232
16	TXD[07]	Transmit Data Serial Channel 8	Output	RS232
17	RTS#[07]	Request To Send Serial Channel 8	Output	RS232
18	TXD[08]	Transmit Data Serial Channel 9	Output	RS232
19	RTS#[08]	Request To Send Serial Channel 9	Output	RS232
20	TXD[09]	Transmit Data Serial Channel 10	Output	RS232
21	RTS#[09]	Request To Send Serial Channel 10	Output	RS232
22	TXD[10]	Transmit Data Serial Channel 11	Output	RS232
23	RTS#[10]	Request To Send Serial Channel 11	Output	RS232
24	TXD[11]	Transmit Data Serial Channel 12	Output	RS232
25	RTS#[11]	Request To Send Serial Channel 12	Output	RS232
26	GND			
27	TXD[12]	Transmit Data Serial Channel 13	Output	RS232
28	RTS#[12]	Request To Send Serial Channel 13	Output	RS232
29	TXD[13]	Transmit Data Serial Channel 14	Output	RS232
30	RTS#[13]	Request To Send Serial Channel 14	Output	RS232
31	TXD[14]	Transmit Data Serial Channel 15	Output	RS232
32	RTS#[14]	Request To Send Serial Channel 15	Output	RS232
33	TXD[15]	Transmit Data Serial Channel 16	Output	RS232
34	RTS#[15]	Request To Send Serial Channel 16	Output	RS232
35	RXD[00]	Receive Data Serial Channel 1	Input	RS232
36	CTS#[00]	Clear To Send Serial Channel 1	Input	RS232
37	RXD[01]	Receive Data Serial Channel 2	Input	RS232
38	CTS#[01]	Clear To Send Serial Channel 2	Input	RS232

Pin	Signal	Description	Direction	Level
39	RXD[02]	Receive Data Serial Channel 3	Input	RS232
40	CTS#[02]	Clear To Send Serial Channel 3	Input	RS232
41	RXD[03]	Receive Data Serial Channel 4	Input	RS232
42	CTS#[03]	Clear To Send Serial Channel 4	Input	RS232
43	GND			
44	RXD[04]	Receive Data Serial Channel 5	Input	RS232
45	CTS#[04]	Clear To Send Serial Channel 5	Input	RS232
46	RXD[05]	Receive Data Serial Channel 6	Input	RS232
47	CTS#[05]	Clear To Send Serial Channel 6	Input	RS232
48	RXD[06]	Receive Data Serial Channel 7	Input	RS232
49	CTS#[06]	Clear To Send Serial Channel 7	Input	RS232
50	RXD[07]	Receive Data Serial Channel 8	Input	RS232
51	CTS#[07]	Clear To Send Serial Channel 8	Input	RS232
52	RXD[08]	Receive Data Serial Channel 9	Input	RS232
53	CTS#[08]	Clear To Send Serial Channel 9	Input	RS232
54	RXD[09]	Receive Data Serial Channel 10	Input	RS232
55	CTS#[09]	Clear To Send Serial Channel 10	Input	RS232
56	RXD[10]	Receive Data Serial Channel 11	Input	RS232
57	CTS#[10]	Clear To Send Serial Channel 11	Input	RS232
58	RXD[11]	Receive Data Serial Channel 12	Input	RS232
59	CTS#[11]	Clear To Send Serial Channel 12	Input	RS232
60	GND			
61	RXD[12]	Receive Data Serial Channel 13	Input	RS232
62	CTS#[12]	Clear To Send Serial Channel 13	Input	RS232
63	RXD[13]	Receive Data Serial Channel 14	Input	RS232
64	CTS#[13]	Clear To Send Serial Channel 14	Input	RS232
65	RXD[14]	Receive Data Serial Channel 15	Input	RS232
66	CTS#[14]	Clear To Send Serial Channel 15	Input	RS232
67	RXD[15]	Receive Data Serial Channel 16	Input	RS232
68	CTS#[15]	Clear To Send Serial Channel 16	Input	RS232

Table 8-1 : TPMC868-10R HD68 SCSI-3 type female connector

8.2 TPMC868-10R Back I/O PMC Connector (P14)

Pin	Signal	Description	Direction	Level
1	TXD[00]	Transmit Data Serial Channel 1	Output	RS232
2	RXD[00]	Receive Data Serial Channel 1	Input	RS232
3	RTS#[00]	Request To Send Serial Channel 1	Output	RS232
4	CTS#[00]	Clear To Send Serial Channel 1	Input	RS232
5	TXD[01]	Transmit Data Serial Channel 2	Output	RS232
6	RXD[01]	Receive Data Serial Channel 2	Input	RS232
7	RTS#[01]	Request To Send Serial Channel 2	Output	RS232
8	CTS#[01]	Clear To Send Serial Channel 2	Input	RS232
9	TXD[02]	Transmit Data Serial Channel 3	Output	RS232
10	RXD[02]	Receive Data Serial Channel 3	Input	RS232
11	RTS#[02]	Request To Send Serial Channel 3	Output	RS232
12	CTS#[02]	Clear To Send Serial Channel 3	Input	RS232
13	TXD[03]	Transmit Data Serial Channel 4	Output	RS232
14	RXD[03]	Receive Data Serial Channel 4	Input	RS232
15	RTS#[03]	Request To Send Serial Channel 4	Output	RS232
16	CTS#[03]	Clear To Send Serial Channel 4	Input	RS232
17	TXD[04]	Transmit Data Serial Channel 5	Output	RS232
18	RXD[04]	Receive Data Serial Channel 5	Input	RS232
19	RTS#[04]	Request To Send Serial Channel 5	Output	RS232
20	CTS#[04]	Clear To Send Serial Channel 5	Input	RS232
21	TXD[05]	Transmit Data Serial Channel 6	Output	RS232
22	RXD[05]	Receive Data Serial Channel 6	Input	RS232
23	RTS#[05]	Request To Send Serial Channel 6	Output	RS232
24	CTS#[05]	Clear To Send Serial Channel 6	Input	RS232
25	TXD[06]	Transmit Data Serial Channel 7	Output	RS232
26	RXD[06]	Receive Data Serial Channel 7	Input	RS232
27	RTS#[06]	Request To Send Serial Channel 7	Output	RS232
28	CTS#[06]	Clear To Send Serial Channel 7	Input	RS232
29	TXD[07]	Transmit Data Serial Channel 8	Output	RS232
30	RXD[07]	Receive Data Serial Channel 8	Input	RS232
31	RTS#[07]	Request To Send Serial Channel 8	Output	RS232
32	CTS#[07]	Clear To Send Serial Channel 8	Input	RS232
33	TXD[08]	Transmit Data Serial Channel 9	Output	RS232
34	RXD[08]	Receive Data Serial Channel 9	Input	RS232
35	RTS#[08]	Request To Send Serial Channel 9	Output	RS232
36	CTS#[08]	Clear To Send Serial Channel 9	Input	RS232
37	TXD[09]	Transmit Data Serial Channel 10	Output	RS232
38	RXD[09]	Receive Data Serial Channel 10	Input	RS232
39	RTS#[09]	Request To Send Serial Channel 10	Output	RS232
40	CTS#[09]	Clear To Send Serial Channel 10	Input	RS232
41	TXD[10]	Transmit Data Serial Channel 11	Output	RS232

Pin	Signal	Description	Direction	Level
42	RXD[10]	Receive Data Serial Channel 11	Input	RS232
43	RTS#[10]	Request To Send Serial Channel 11	Output	RS232
44	CTS#[10]	Clear To Send Serial Channel 11	Input	RS232
45	TXD[11]	Transmit Data Serial Channel 12	Output	RS232
46	RXD[11]	Receive Data Serial Channel 12	Input	RS232
47	RTS#[11]	Request To Send Serial Channel 12	Output	RS232
48	CTS#[11]	Clear To Send Serial Channel 12	Input	RS232
49	TXD[12]	Transmit Data Serial Channel 13	Output	RS232
50	RXD[12]	Receive Data Serial Channel 13	Input	RS232
51	RTS#[12]	Request To Send Serial Channel 13	Output	RS232
52	CTS#[12]	Clear To Send Serial Channel 13	Input	RS232
53	TXD[13]	Transmit Data Serial Channel 14	Output	RS232
54	RXD[13]	Receive Data Serial Channel 14	Input	RS232
55	RTS#[13]	Request To Send Serial Channel 14	Output	RS232
56	CTS#[13]	Clear To Send Serial Channel 14	Input	RS232
57	TXD[14]	Transmit Data Serial Channel 15	Output	RS232
58	RXD[14]	Receive Data Serial Channel 15	Input	RS232
59	RTS#[14]	Request To Send Serial Channel 15	Output	RS232
60	CTS#[14]	Clear To Send Serial Channel 15	Input	RS232
61	TXD[15]	Transmit Data Serial Channel 16	Output	RS232
62	RXD[15]	Receive Data Serial Channel 16	Input	RS232
63	RTS#[15]	Request To Send Serial Channel 16	Output	RS232
64	CTS#[15]	Clear To Send Serial Channel 16	Input	RS232

Table 8-2 : TPMC868-10R Back I/O PMC Connector (P14)

8.3 TPMC868-11R Front Panel I/O Connector

Pin	Signal	Description	Direction	Level
1	TXD+[00]	Transmit Data Pos. Serial Ch. 1	Output	RS422
2	RXD+[00]	Receive Data Pos. Serial Ch. 1	Input	RS422
3	TXD+[01]	Transmit Data Pos. Serial Ch. 2	Output	RS422
4	RXD+[01]	Receive Data Pos. Serial Ch. 2	Input	RS422
5	TXD+[02]	Transmit Data Pos. Serial Ch. 3	Output	RS422
6	RXD+[02]	Receive Data Pos. Serial Ch. 3	Input	RS422
7	TXD+[03]	Transmit Data Pos. Serial Ch. 4	Output	RS422
8	RXD+[03]	Receive Data Pos. Serial Ch. 4	Input	RS422
9	GND			
10	TXD+[04]	Transmit Data Pos. Serial Ch. 5	Output	RS422
11	RXD+[04]	Receive Data Pos. Serial Ch. 5	Input	RS422
12	TXD+[05]	Transmit Data Pos. Serial Ch. 6	Output	RS422
13	RXD+[05]	Receive Data Pos. Serial Ch. 6	Input	RS422
14	TXD+[06]	Transmit Data Pos. Serial Ch. 7	Output	RS422
15	RXD+[06]	Receive Data Pos. Serial Ch. 7	Input	RS422
16	TXD+[07]	Transmit Data Pos. Serial Ch. 8	Output	RS422
17	RXD+[07]	Receive Data Pos. Serial Ch. 8	Input	RS422
18	TXD+[08]	Transmit Data Pos. Serial Ch. 9	Output	RS422
19	RXD+[08]	Receive Data Pos. Serial Ch. 9	Input	RS422
20	TXD+[09]	Transmit Data Pos. Serial Ch. 10	Output	RS422
21	RXD+[09]	Receive Data Pos. Serial Ch. 10	Input	RS422
22	TXD+[10]	Transmit Data Pos. Serial Ch. 11	Output	RS422
23	RXD+[10]	Receive Data Pos. Serial Ch. 11	Input	RS422
24	TXD+[11]	Transmit Data Pos. Serial Ch. 12	Output	RS422
25	RXD+[11]	Receive Data Pos. Serial Ch. 12	Input	RS422
26	GND			
27	TXD+[12]	Transmit Data Pos. Serial Ch. 13	Output	RS422
28	RXD+[12]	Receive Data Pos. Serial Ch. 13	Input	RS422
29	TXD+[13]	Transmit Data Pos. Serial Ch. 14	Output	RS422
30	RXD+[13]	Receive Data Pos. Serial Ch. 14	Input	RS422
31	TXD+[14]	Transmit Data Pos. Serial Ch. 15	Output	RS422
32	RXD+[14]	Receive Data Pos. Serial Ch. 15	Input	RS422
33	TXD+[15]	Transmit Data Pos. Serial Ch. 16	Output	RS422
34	RXD+[15]	Receive Data Pos. Serial Ch. 16	Input	RS422
35	TXD-[00]	Transmit Data Neg. Serial Ch. 1	Output	RS422
36	RXD-[00]	Receive Data Neg. Serial Ch. 1	Input	RS422
37	TXD-[01]	Transmit Data Neg. Serial Ch. 2	Output	RS422
38	RXD-[01]	Receive Data Neg. Serial Ch. 2	Input	RS422
39	TXD-[02]	Transmit Data Neg. Serial Ch. 3	Output	RS422
40	RXD-[02]	Receive Data Neg. Serial Ch. 3	Input	RS422
41	TXD-[03]	Transmit Data Neg. Serial Ch. 4	Output	RS422

Pin	Signal	Description	Direction	Level
42	RXD-[03]	Receive Data Neg. Serial Ch. 4	Input	RS422
43	GND			
44	TXD-[04]	Transmit Data Neg. Serial Ch. 5	Output	RS422
45	RXD-[04]	Receive Data Neg. Serial Ch. 5	Input	RS422
46	TXD-[05]	Transmit Data Neg. Serial Ch. 6	Output	RS422
47	RXD-[05]	Receive Data Neg. Serial Ch. 6	Input	RS422
48	TXD-[06]	Transmit Data Neg. Serial Ch. 7	Output	RS422
49	RXD-[06]	Receive Data Neg. Serial Ch. 7	Input	RS422
50	TXD-[07]	Transmit Data Neg. Serial Ch. 8	Output	RS422
51	RXD-[07]	Receive Data Neg. Serial Ch. 8	Input	RS422
52	TXD-[08]	Transmit Data Neg. Serial Ch. 9	Output	RS422
53	RXD-[08]	Receive Data Neg. Serial Ch. 9	Input	RS422
54	TXD-[09]	Transmit Data Neg. Serial Ch. 10	Output	RS422
55	RXD-[09]	Receive Data Neg. Serial Ch. 10	Input	RS422
56	TXD-[10]	Transmit Data Neg. Serial Ch. 11	Output	RS422
57	RXD-[10]	Receive Data Neg. Serial Ch. 11	Input	RS422
58	TXD-[11]	Transmit Data Neg. Serial Ch. 12	Output	RS422
59	RXD-[11]	Receive Data Neg. Serial Ch. 12	Input	RS422
60	GND			
61	TXD-[12]	Transmit Data Neg. Serial Ch. 13	Output	RS422
62	RXD-[12]	Receive Data Neg. Serial Ch. 13	Input	RS422
63	TXD-[13]	Transmit Data Neg. Serial Ch. 14	Output	RS422
64	RXD-[13]	Receive Data Neg. Serial Ch. 14	Input	RS422
65	TXD-[14]	Transmit Data Neg. Serial Ch. 15	Output	RS422
66	RXD-[14]	Receive Data Neg. Serial Ch. 15	Input	RS422
67	TXD-[15]	Transmit Data Neg. Serial Ch. 16	Output	RS422
68	RXD-[15]	Receive Data Neg. Serial Ch. 16	Input	RS422

Table 8-3 : TPMC868-11R HD68 SCSI-3 type Female Connector

8.4 TPMC868-11R Back I/O PMC Connector (P14)

Pin	Signal	Description	Direction	Level
1	TXD+[00]	Transmit Data Pos. Serial Ch. 1	Output	RS422
2	TXD-[00]	Transmit Data Neg. Serial Ch. 1	Output	RS422
3	RXD+[00]	Receive Data Pos. Serial Ch. 1	Input	RS422
4	RXD-[00]	Receive Data Neg. Serial Ch. 1	Input	RS422
5	TXD+[01]	Transmit Data Pos. Serial Ch. 2	Output	RS422
6	TXD-[01]	Transmit Data Neg. Serial Ch. 2	Output	RS422
7	RXD+[01]	Receive Data Pos. Serial Ch. 2	Input	RS422
8	RXD-[01]	Receive Data Neg. Serial Ch. 2	Input	RS422
9	TXD+[02]	Transmit Data Pos. Serial Ch. 3	Output	RS422
10	TXD-[02]	Transmit Data Neg. Serial Ch. 3	Output	RS422
11	RXD+[02]	Receive Data Pos. Serial Ch. 3	Input	RS422
12	RXD-[02]	Receive Data Neg. Serial Ch. 3	Input	RS422
13	TXD+[03]	Transmit Data Pos. Serial Ch. 4	Output	RS422
14	TXD-[03]	Transmit Data Neg. Serial Ch. 4	Output	RS422
15	RXD+[03]	Receive Data Pos. Serial Ch. 4	Input	RS422
16	RXD-[03]	Receive Data Neg. Serial Ch. 4	Input	RS422
17	TXD+[04]	Transmit Data Pos. Serial Ch. 5	Output	RS422
18	TXD-[04]	Transmit Data Neg. Serial Ch. 5	Output	RS422
19	RXD+[04]	Receive Data Pos. Serial Ch. 5	Input	RS422
20	RXD-[04]	Receive Data Neg. Serial Ch. 5	Input	RS422
21	TXD+[05]	Transmit Data Pos. Serial Ch. 6	Output	RS422
22	TXD-[05]	Transmit Data Neg. Serial Ch. 6	Output	RS422
23	RXD+[05]	Receive Data Pos. Serial Ch. 6	Input	RS422
24	RXD-[05]	Receive Data Neg. Serial Ch. 6	Input	RS422
25	TXD+[06]	Transmit Data Pos. Serial Ch. 7	Output	RS422
26	TXD-[06]	Transmit Data Neg. Serial Ch. 7	Output	RS422
27	RXD+[06]	Receive Data Pos. Serial Ch. 7	Input	RS422
28	RXD-[06]	Receive Data Neg. Serial Ch. 7	Input	RS422
29	TXD+[07]	Transmit Data Pos. Serial Ch. 8	Output	RS422
30	TXD-[07]	Transmit Data Neg. Serial Ch. 8	Output	RS422
31	RXD+[07]	Receive Data Pos. Serial Ch. 8	Input	RS422
32	RXD-[07]	Receive Data Neg. Serial Ch. 8	Input	RS422
33	TXD+[08]	Transmit Data Pos. Serial Ch. 9	Output	RS422
34	TXD-[08]	Transmit Data Neg. Serial Ch. 9	Output	RS422
35	RXD+[08]	Receive Data Pos. Serial Ch. 9	Input	RS422
36	RXD-[08]	Receive Data Neg. Serial Ch. 9	Input	RS422
37	TXD+[09]	Transmit Data Pos. Serial Ch. 10	Output	RS422
38	TXD-[09]	Transmit Data Neg. Serial Ch. 10	Output	RS422
39	RXD+[09]	Receive Data Pos. Serial Ch. 10	Input	RS422
40	RXD-[09]	Receive Data Neg. Serial Ch. 10	Input	RS422
41	TXD+[10]	Transmit Data Pos. Serial Ch. 11	Output	RS422

Pin	Signal	Description	Direction	Level
42	TXD-[10]	Transmit Data Neg. Serial Ch. 11	Output	RS422
43	RXD+[10]	Receive Data Pos. Serial Ch. 11	Input	RS422
44	RXD-[10]	Receive Data Neg. Serial Ch. 11	Input	RS422
45	TXD+[11]	Transmit Data Pos. Serial Ch. 12	Output	RS422
46	TXD-[11]	Transmit Data Neg. Serial Ch. 12	Output	RS422
47	RXD+[11]	Receive Data Pos. Serial Ch. 12	Input	RS422
48	RXD-[11]	Receive Data Neg. Serial Ch. 12	Input	RS422
49	TXD+[12]	Transmit Data Pos. Serial Ch. 13	Output	RS422
50	TXD-[12]	Transmit Data Neg. Serial Ch. 13	Output	RS422
51	RXD+[12]	Receive Data Pos. Serial Ch. 13	Input	RS422
52	RXD-[12]	Receive Data Neg. Serial Ch. 13	Input	RS422
53	TXD+[13]	Transmit Data Pos. Serial Ch. 14	Output	RS422
54	TXD-[13]	Transmit Data Neg. Serial Ch. 14	Output	RS422
55	RXD+[13]	Receive Data Pos. Serial Ch. 14	Input	RS422
56	RXD-[13]	Receive Data Neg. Serial Ch. 14	Input	RS422
57	TXD+[14]	Transmit Data Pos. Serial Ch. 15	Output	RS422
58	TXD-[14]	Transmit Data Neg. Serial Ch. 15	Output	RS422
59	RXD+[14]	Receive Data Pos. Serial Ch. 15	Input	RS422
60	RXD-[14]	Receive Data Neg. Serial Ch. 15	Input	RS422
61	TXD+[15]	Transmit Data Pos. Serial Ch. 16	Output	RS422
62	TXD-[15]	Transmit Data Neg. Serial Ch. 16	Output	RS422
63	RXD+[15]	Receive Data Pos. Serial Ch. 16	Input	RS422
64	RXD-[15]	Receive Data Neg. Serial Ch. 16	Input	RS422

Table 8-4 : TPMC868-11R Back I/O PMC Connector (P14)

Connect channel I/O either to front I/O or P14 back I/O at a time. Do not connect an I/O channel to both front I/O connector and P14 back I/O connector at the same time.

There is no GND signal present on the P14 back I/O connector. Make sure that back I/O connected systems are using the same ground as the TPMC868 system.

The TPMC868-11R (RS422) provides on board termination resistors. Do not apply additional external termination resistors here.

Please note that on the TPMC868-10R and TPMC868-11R, the P14 back I/O connector is always populated and connected to on board logic. Do not use these modules on carrier boards where P14/J14 is reserved for other system signals but PMC I/O. Ask support for special board options with front I/O only in this case.