The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC881

10/100Mbit/s Ethernet Adapter

Version 1.0

Revision A

User Manual

Issue 1.1

September 2006

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TPMC881-10

10/100Mbit/s Ethernet Adapter
Front panel connector

TPMC881-10-ET

10/100Mbit/s Ethernet Adapter
Extended Temperature Range
Front panel connector

TPMC881-11

10/100Mbit/s Ethernet Adapter
P14 Back I/O

TPMC881-11-ET

10/100Mbit/s Ethernet Adapter
Extended Temperature Range
P14 Back I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	Preliminary Issue	May 2004
1.1	New address TEWS LLC	September 2006

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1 Product Description

The TPMC881 is a PCI Mezzanine Card (PMC) compatible module providing a single channel Ethernet 10BASE-T/100BASE-TX interface.

An Intel™ 82551ER/82551IT Ethernet Controller is used, which supports 10 and 100Mbit/s transmission rates for half and full duplex operation. The TPMC881-10 is capable of performing an auto negotiation algorithm which allows both link-partners to find out the best link-parameters by themselves. The TPMC881 is widely user configurable via configuration and status register access over the PCI bus. Front panel mounted LEDs indicate various network activities.

The TPMC881-10 provides a 10/100Mbit/s network connection via a front panel RJ45 connector, TPMC881-11 provides rear panel I/O via P14. The ports are galvanically isolated from the Ethernet Controller.

The module versions TPMC881-10/-11 operates from 0 °C to +85 °C and the TPMC881-10-ET/-11-ET meets the requirements to operate in extended temperature range from -40° to +85°C.

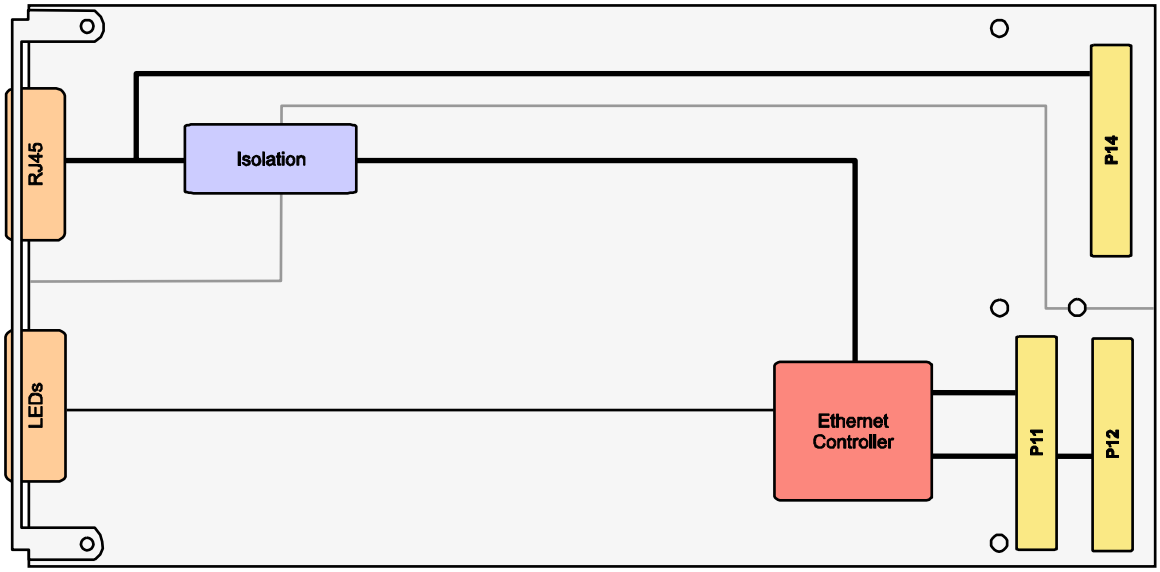

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI Rev. 2.1 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
Ethernet Controller with Integrated PCI and Physical Interface	82551ER/82551IT (Intel)	
Ethernet Interface		
Number of Channels	1	
FIFO	3 Kbyte Transmit and Receive FIFOs	
Interrupts	Using PCI INTA	
I/O Connector	-10: Front panel Modular Jack -11: PMC P14 I/O (64 pin Mezzanine Connector)	
Physical Data		
Power Requirements	150mA typical @ +3.3V DC	
Temperature Range	Operating Storage	0 °C to +85 °C (TPMC881-10/-11) -40°C to +85°C (TPMC881-10-ET/-11-ET) -40°C to +85°C
MTBF	600.000 h	
Humidity	5 – 95 % non-condensing	
Weight	58g	

Figure 2-1 : Technical Specification

3 82551 Ethernet Controller

3.1 82551 PCI Header

Offset	PCI Configuration Register				Setting
	31 - 24	23 - 16	15 - 08	07 - 00	
0x00	Device ID		Vendor ID		0x1209_8086
0x04	Status		Command		0x0290_0007
0x08	Class Code			Revision ID	0x0200_00xx
0x0C	BIST	Header	Latency	Cache Line	0x0000_xx00
0x10	PCI Base Address 0 (Memory Mapped Configuration Register)				0xFFFF_F000 (4 Kbyte)
0x14	PCI Base Address 0 (I/O Mapped Configuration Register)				0xFFFF_FF81 (64 Byte)
0x18	PCI Base Address 0 (Memory Mapped FLASH Space)				0xFFFE_0000 (128 Kbyte)
0x1C	Reserved				0x0000_0000
0x20	Reserved				0x0000_0000
0x24	Reserved				0x0000_0000
0x28	Reserved				0x0000_0000
0x2C	Subsystem ID		Subsystem Vendor ID		0x1209_8086
0x30	Expansion ROM PCI Base Address				0x0000_0000
0x34	Reserved			Cap. Pointer	0x0000_00DC
0x38	Reserved				0x0000_0000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	0xxx08_0100
0xDC	Power Management Cap.		Next Cap.	Cap. ID	0x7E22_0001
0xE0	Reserved	Data	Power Management CSR		0x4B00_4000

Figure 3-1 : 82551 PCI Header

3.2 Configuration EEPROM

After power-on or PCI reset the 82551 loads the initial configuration register data from the on board configuration EEPROM.

See the 82551 Manual for more information.

EEPROM Address (16 bit Address)	Description	
	Bits 15 - 8	**Bits 07 - 00**
0x00	Ethernet Address Byte 1	Ethernet Address Byte 0
	0x01	0x00
0x01	Ethernet Address Byte 3	Ethernet Address Byte 2
	xx	0x06
0x02	Ethernet Address Byte 5	Ethernet Address Byte 4
	zz	*yy*
..		
0x0A	EEPROM-ID	
	0x4840	
0x0B	Subsystem-ID	
	0x1209	
0x0C	Subsystem-Vendor-ID	
	0x8086	
..		
0x23	Subsystem-ID	
	0x1209	
..		
0x3F	EEPROM Checksum	
	variant	

Figure 3-2 : 82551 Configuration EEPROM Settings

4 Pin Assignment – I/O Connector

4.1 Front Panel I/O Connector

Pin	Signal
1	TX+
2	TX-
3	RX+
4	Not Used
5	Not Used
6	RX-
7	Not Used
8	Not Used

Figure 4-1 : Front I/O Pin Assignment

4.2 Back I/O PMC Connector

Pin	Signal
1 … 24	N.C.
25	TX+
26	TX-
27	N.C.
28	N.C.
29	RX+
30	RX-
31 ... 64	N.C.

Figure 4-2 : P14 I/O Pin Assignment