The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC882

4 Channel 10/100Mbit/s Ethernet Adapter

Version 1.0

User Manual

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TEWS TECHNOLOGIES GmbH
Am Bahnhof 7
25469 Halstenbek, Germany www.tews.com
Phone: +49-(0)4101-4058-0
Fax: +49-(0)4101-4058-19
e-mail: info@tews.com

TPMC882-10R

4 Channel 10Base-T/100Base-TX Ethernet Interface
Front panel I/O, Extended Temperature Range

TPMC882-11R

4 Channel 10Base-T/100Base-TX Ethernet Interface
Back I/O, Extended Temperature Range

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	Preliminary Issue	April 2005
1.1	Removed preliminary status, Back I/O information added	May 2005
1.2	New address TEWS LLC	September 2006
1.0.3	New User Manual Issue Notation	April 2009
1.0.4	General Revision	August 2014

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1 Product Description

The TPMC882 is a PCI Mezzanine Card (PMC) compatible module providing a four channel Ethernet 10BASE-T/100BASE-TX interface.

A transparent 32 Bit / 66 MHz PCI-to-PCI Bridge provides access to the four Intel™ 82551IT Ethernet Controllers which support 10 and 100Mbit/s transmission rates for half and full duplex operation. Each Ethernet Interface of the TPMC882 is capable of performing an auto negotiation algorithm which allows both link-partners to find out the best link-parameters by themselves. The TPMC882 is widely user configurable via configuration and status register access over the PCI bus.

The TPMC882-10R provides four 10/100Mbit/s network connections via front panel RJ45 connectors. The TPMC882-11R routes all four Ethernet ports to the Back I/O P14 connector. The ports are galvanically isolated from the Ethernet Controller.

The module meets the requirements to operate in extended temperature range from -40° to +85°C.

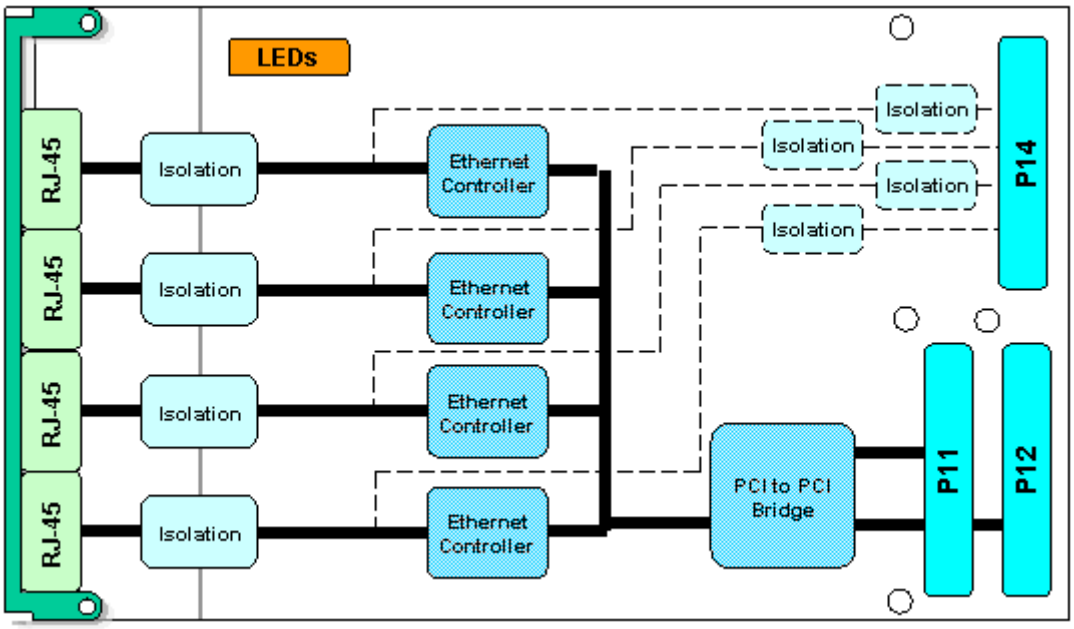

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface Single Size	
Electrical Interface	PCI Rev. 2.1 compliant 66 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
PCI-to-PCI Bridge	PCI2050B (Texas Instruments)	
Ethernet Controller with Integrated PCI and Physical Interface	82551IT (Intel) per Channel	
Ethernet Interface		
Number of Interfaces	4	
FIFO	3 Kbyte Transmit and Receive FIFOs per Channel	
Interrupts	Using PCI INTA, INTB, INTC, and INTD	
I/O Connector	TPMC822-10R: 4 x RJ45 Modular Jack located in the Front Panel	
	TPMC822-11R: PMC P14 Back I/O	
Physical Data		
Power Requirements	700 mA typical @ +3.3V DC	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	TPMC882-10R: 341000 h TPMC882-11R: 447000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	55 g	

Table 2-1 : Technical Specification

3 Local PCI-to-PCI Bridge

3.1 Secondary PCI Bus Overview

The TPMC882 uses four Intel 82551IT Fast Ethernet Controllers to provide and control the 4 10/100MBit Ethernet Interfaces. A transparent 32 bit / 66 MHz PCI-to-PCI Bridge provides access to the four Ethernet Controllers. The PCI-to-PCI Bridge allows 32 bit accesses on the local PCI bus and permits the high data throughput necessary for the high performance Fast Ethernet Interfaces.

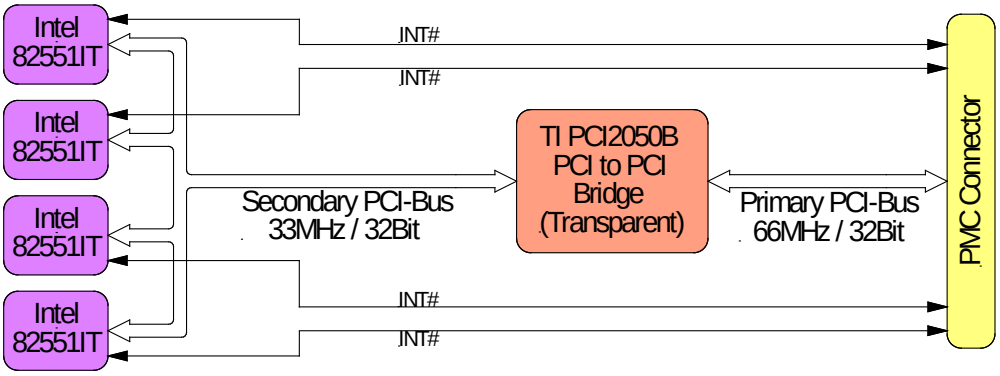

Figure 3-1 : Primary and secondary PCI Bus

The following chart gives information about the device numbers of the Ethernet Controllers and how their interrupts are wired to the Primary PCI Bus:

	Secondary PCI Bus Device Number	Secondary AD-Line used as IDSEL	Primary PCI Bus Interrupt Line
Ethernet Port 1	4	AD20	INTA#
Ethernet Port 2	5	AD21	INTB#
Ethernet Port 3	6	AD22	INTC#
Ethernet Port 4	7	AD23	INTD#

Table 3-1 : Secondary PCI Bus Overview

3.2 PCI2050B PCI-to-PCI Bridge General Info

Vendor ID: 0x104C (Texas Instruments)

Device ID: 0xAC28 (PCI2050B)

The general purpose I/O interface is not used. GPIO pins are pulled up.

Only secondary clock outputs 0-3 and 9 are used to clock secondary devices. The host software may disable clock outputs 4-8 through the secondary clock control register located at PCI offset 0x68 to save power.

For detailed description of the PCI2050B PCI-to-PCI Bridge refer to the PCI2050B datasheet, which is available on the Texas Instruments website (www.ti.com).

3.2.1 PCI2050B PCI Header

PCI CFG Register Address	PCI Configuration Register				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	AC28 104C
0x04	Status		Command		Y	0290 0000
0x08	Class Code			Revision ID	N	06 04 00 02
0x0C	BIST	Header Type	Primary Latency Timer	Cache Line Size	Y[15:0]	00 01 00 00
0x10	Base Address 0				N	00000000
0x14	Base Address 1				N	00000000
0x18	Secondary Bus Latency Timer	Subordinate Bus Number	Secondary Bus Number	Primary Bus Number	Y	00 00 00 00
0x1C	Secondary Status		I/O Limit Address	I/O Base Address	Y	0280 01 01
0x20	Memory Limit Address		Memory Base Address		Y	0000 0000
0x24	Prefetchable Memory Limit Address		Prefetchable Memory Base Address		Y	0000 0000
0x28	Prefetchable Memory Base Address Upper 32 Bits				Y	00000000
0x2C	Prefetchable Memory Limit Address Upper 32 Bits				Y	00000000
0x30	I/O Limit Address Upper 16 Bits		I/O Base Address Upper 16 Bits		Y	0000 0000
0x34	Reserved			Cap. Pointer	Y	000000 DC
0x38	Expansion ROM Base Address				N	00000000
0x3C	Bridge Control		Interrupt Pin	Interrupt Line	Y/N[15:8]	0000 00 00
0x40	Arbiter Control		Extended Diagnostic	Chip Control	Y	0200 00 00
0x44 – 0x60	Reserved				N	00000000
0x64	GPIO Input Data	GPIO Output Enable Control	GPIO Output Data	P_SERR# Event Disable	Y / N[31:24]	X0 00 00 00
0x68	Reserved	P_SERR# Status	Secondary Clock Control		Y	00 00 0000
0x6C – 0xD8	Reserved				N	00000000
0xDC	Power Management Capabilities		PM Next Item Pointer.	PM Capability ID	N	0001 00 01
0xE0	Data	PMCSR Bridge Support	Power Management Control/Status Register		Y / N[31:16]	00 00 0000
0xE4	Reserved	Hot Swap Control Status	HS Next Item Pointer	HS Capability ID	N	00 00 00 00
0xE8 – 0xEC	Reserved				N	00000000
0xF0	Reserved			Diagnostics	Y	000000 00
0xF4 – 0xFF	Reserved				N	00000000

Table 3-2 : PCI2050B PCI Header

4 Ethernet Controller

4.1 Intel 82551IT PCI Header

Offset	PCI Configuration Register				Setting
	31 - 24	23 - 16	15 - 08	07 - 00	
0x00	Device ID		Vendor ID		0x1209_8086
0x04	Status		Command		0x0290_0007
0x08	Class Code			Revision ID	0x0200_00xx
0x0C	BIST	Header	Latency	Cache Line	0x0000_xx00
0x10	PCI Base Address 0 (Memory Mapped Configuration Register)				0xFFFF_F000 (4 Kbyte)
0x14	PCI Base Address 1 (I/O Mapped Configuration Register)				0xFFFF_FF81 (64 Byte)
0x18	PCI Base Address 2 (Memory Mapped FLASH Space)				0xFFFE_0000 (128 Kbyte)
0x1C	Reserved				0x0000_0000
0x20	Reserved				0x0000_0000
0x24	Reserved				0x0000_0000
0x28	Reserved				0x0000_0000
0x2C	Subsystem ID		Subsystem Vendor ID		0x0000_0000
0x30	Expansion ROM PCI Base Address				0x0000_0000
0x34	Reserved			Cap. Pointer	0x0000_00DC
0x38	Reserved				0x0000_0000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	0xxx08_0100
0xDC	Power Management Cap.		Next Cap.	Cap. ID	0x7E22_0001
0xE0	Reserved	Data	Power Management CSR		0x4B00_4000

Table 4-1 : Intel 82551IT PCI Header

4.2 Configuration EEPROM

After power-on or PCI reset each Intel 82551IT Ethernet controller loads its initial configuration register data from its own on board configuration EEPROM.

See the Intel 82551IT Manual for more information.

EEPROM Address (16 bit Address)	Description		Value
	Bits 15 - 8	Bits 07 - 00	
0x00	Ethernet Address Byte [1:0]		0x0100
0x01	Ethernet Address Byte [3:2]		0xww06
0x02	Ethernet Address Byte [5:4]		0xzzyy
0x03	Compatibility Byte[1:0]		0x0387
0x04	reserved		0x0000
0x05	Controller Type	Connectors	0x0201
0x06	Primary PHY Record		0x4701
0x07	Secondary PHY Record		0x0000
0x08	PWA Byte [1:0]		0x0000
0x09	PWA Byte [3:2]		0x0000
0x0A	EEPROM-ID		0xDF44
0x0B	Subsystem-ID		s.b.
0x0C	Subsystem-Vendor-ID		0x1498
0x0D – 0x22	Reserved		0x0000
0x23	Device-ID		0x1209
0x24 – 0x2F	Reserved		0x0000
0x30	Boot Agent Main Setup Options		0x900C
0x31	Boot Agent Configuration Customization Options		0x0000
0x32	Boot Agent Configuration Customization Options		0x0000
0x33	IBA Capabilities		0x0001
0x34 – 0x3E	Reserved		0x0000
0x3F	EEPROM Checksum		

Table 4-2 : Intel 82551IT Configuration EEPROM Settings

The EEPROM Addresses 0x00 to 0x02 contain the factory programmed individual Ethernet Address. The value of ww, zz and yy is unique for each Intel 82551IT Ethernet controller.

Subsystem-ID (Module dependent):

0x000A = TPMC882-10R

0x000B = TPMC882-11R

5 LED Indicators

The TPMC882 provides 4 Status LEDs for quick visual inspection and debugging.

Due to the fact that PMCs are mounted headfirst on the carrier card, the LED indicators are visible on the back side of the TPMC882. A marking is placed close to each LED, to indicate the Ethernet Port the LED corresponds to.

Each Ethernet Port has one LED indicator. See figures below for more details:

LED Status	Description
OFF	No Cable is connected or no Link is established.
ON	A LINK is established at the corresponding Ethernet Port.
BLINK	Indicates Activity. The Ethernet Port transmits or receives data.

Table 5-1 : LED Status Definitions

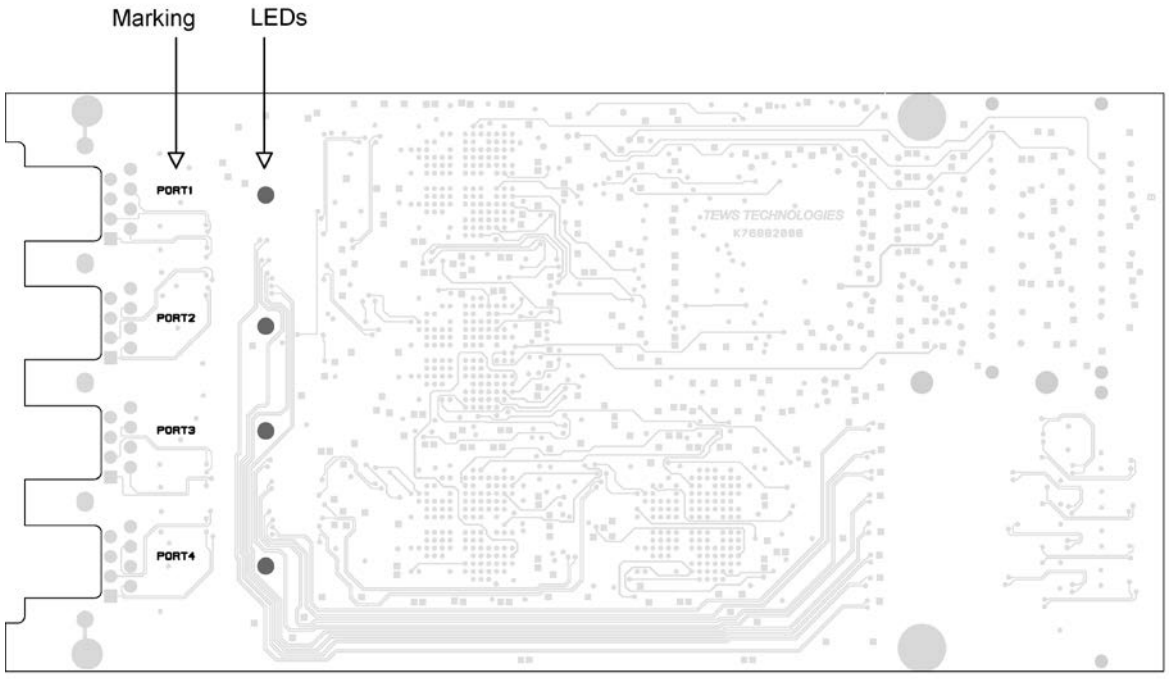

Figure 5-1 : LED Position and Marking (TPMC882 Bottom View)

6 Pin Assignment – I/O Connectors

6.1 Front Panel I/O Connectors (TPMC882-10R only)

On the TPMC882-10R, the Ethernet signals are accessible by four RJ45 Modular Jacks. The connectors are located in the PMC Front Panel.

For Pin Assignment and Front Panel labeling, see the figures below.

Pin	Signal
1	TX+
2	TX-
3	RX+
4	Not Used*)
5	Not Used*)
6	RX-
7	Not Used*)
8	Not Used*)

*) These pins are connected to the Termination Plane via 75 Ohm Resistors. This provides a low frequency return path for the Ethernet signals.

Figure 6-1 : Per Channel Front I/O Pin Assignment

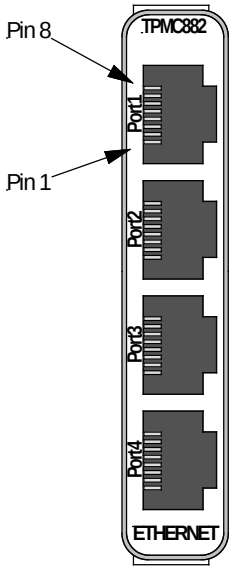

Figure 6-2 : Front Panel View

6.2 Back I/O Connector P14 (TPMC882-11R only)

Pin	Signal	Description	Pin	Signal	Description
1	-	Not Connected	2	-	Not Connected
3	-	Not Connected	4	-	Not Connected
5	-	Not Connected	6	-	Not Connected
7	-	Not Connected	8	-	Not Connected
9	-	Not Connected	10	-	Not Connected
11	-	Not Connected	12	-	Not Connected
13	COMMON4	Termination Plane LAN 4	14	COMMON4	Termination Plane LAN 4
15	LAN4_TDP	Tx+ LAN 4	16	LAN4_RDP	Rx+ LAN 4
17	COMMON4	Termination Plane LAN 4	18	COMMON4	Termination Plane LAN 4
19	LAN4_TDN	Tx- LAN 4	20	LAN4_RDN	Rx- LAN 4
21	-	Not Connected	22	-	Not Connected
23	COMMON3	Termination Plane LAN 3	24	COMMON3	Termination Plane LAN 3
25	LAN3_TDP	Tx+ LAN 3	26	LAN3_RDP	Rx+ LAN 3
27	COMMON3	Termination Plane LAN 3	28	COMMON3	Termination Plane LAN 3
29	LAN3_TDN	Tx- LAN 3	30	LAN3_RDN	Rx- LAN 3
31	-	Not Connected	32	-	Not Connected
33	COMMON2	Termination Plane LAN 2	34	COMMON2	Termination Plane LAN 2
35	LAN2_TDP	Tx+ LAN 2	36	LAN2_RDP	Rx+ LAN 2
37	COMMON2	Termination Plane LAN 2	38	COMMON2	Termination Plane LAN 2
39	LAN2_TDN	Tx- LAN 2	40	LAN2_RDN	Rx- LAN 2
41	-	Not Connected	42	-	Not Connected
43	COMMON1	Termination Plane LAN 1	44	COMMON1	Termination Plane LAN 1
45	LAN1_TDP	Tx+ LAN 1	46	LAN1_RDP	Rx+ LAN 1
47	COMMON1	Termination Plane LAN 1	48	COMMON1	Termination Plane LAN 1
49	LAN1_TDN	Tx- LAN 1	50	LAN1_RDN	Rx- LAN 1
51	-	Not Connected	52	-	Not Connected
53	-	Not Connected	54	-	Not Connected
55	-	Not Connected	56	-	Not Connected
57	-	Not Connected	58	-	Not Connected
59	-	Not Connected	60	-	Not Connected
61	-	Not Connected	62	-	Not Connected
63	-	Not Connected	64	-	Not Connected

Table 6-1 : P14 Pin Assignment

The TPMC882-11R (Back I/O) routes the Ethernet lines to the P14 mezzanine connector. In most cases, the P14 connects to the PMC Carrier that routes the Ethernet lines from P14 to the Backplane. A Transition Module connects to the backside of the Backplane and routes the Ethernet lines to the RJ45. Care must be taken to avoid impedance mismatches and high resistive routing in the Ethernet lines, because it leads to signal distortion and low voltage amplitude.