The Embedded I/O Company

TPMC885

Dual/Four Channel 10/100/1000 Mbit/s Ethernet Adapter

Version 1.0

User Manual

Issue 1.0.5

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TPMC885-10R

Four channel 10/100/1000 Mbit/s Ethernet interface RJ45 front panel I/O, extended temperature range
(RoHS compliant)

TPMC885-11R

Four channel 10/100/1000 Mbit/s Ethernet interface back I/O, extended temperature range
(RoHS compliant)

TPMC885-20R

Dual channel 10/100/1000 Mbit/s Ethernet interface RJ45 front panel I/O, extended temperature range
(RoHS compliant)

TPMC885-21R

Dual channel 10/100/1000 Mbit/s Ethernet interface back I/O, extended temperature range
(RoHS compliant)

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial issue	November 2010
1.0.1	Front I/O variant hardware revision update to Rev.B Note on Ethernet Device Numbering added to PCI Device Topology chapter	September 2011
1.0.2	PCI Device Topology chapter revised	March 2012
1.0.3	Back I/O variant hardware revision update to Rev.B	July 2012
1.0.4	Dual Channel variants -20 and -21 added	March 2014
1.0.5	Hardware revision update to Rev.E	June 2016

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1 Product Description

The TPMC885 is a PCI Mezzanine Card (PMC) compatible module providing a dual or four channel Ethernet 10BASE-T / 100BASE-TX / 1000BASE-T interface.

A transparent 64 bit, up to 133 MHz PCI-X/PCI to PCIe Bridge and a PCIe Switch provide access to the Intel 82574IT Gigabit Ethernet controllers. Each Ethernet interface supports 10, 100 and 1000 Mbit/s transmission rates for full duplex operation, 10 and 100 Mbit/s transmissions for half duplex operation, and is equipped with a 32 Kbit Serial EEPROM.

The two/four Ethernet interfaces of the TPMC885 are capable of performing an auto negotiation algorithm which allows both link-partners to find out the best link-parameters by themselves. The TPMC885 is widely user configurable via configuration and status register access over the PCI bus.

The TPMC885-10R provides four 10/100/1000 Mbit/s Ethernet connections via front panel RJ45 connectors.

The TPMC885-11R routes four Ethernet ports to the back I/O P14 connector without any RJ45 connector at the front.

The TPMC885-20R provides two 10/100/1000 Mbit/s Ethernet connections via front panel RJ45 connectors.

The TPMC885-21R routes two Ethernet ports to the back I/O P14 connector without any RJ45 connector at the front.

All ports are galvanically isolated from the Ethernet controllers and LEDs on the board indicate the different network activities.

The module meets the requirements to operate in extended temperature range from -40° to +85°C.

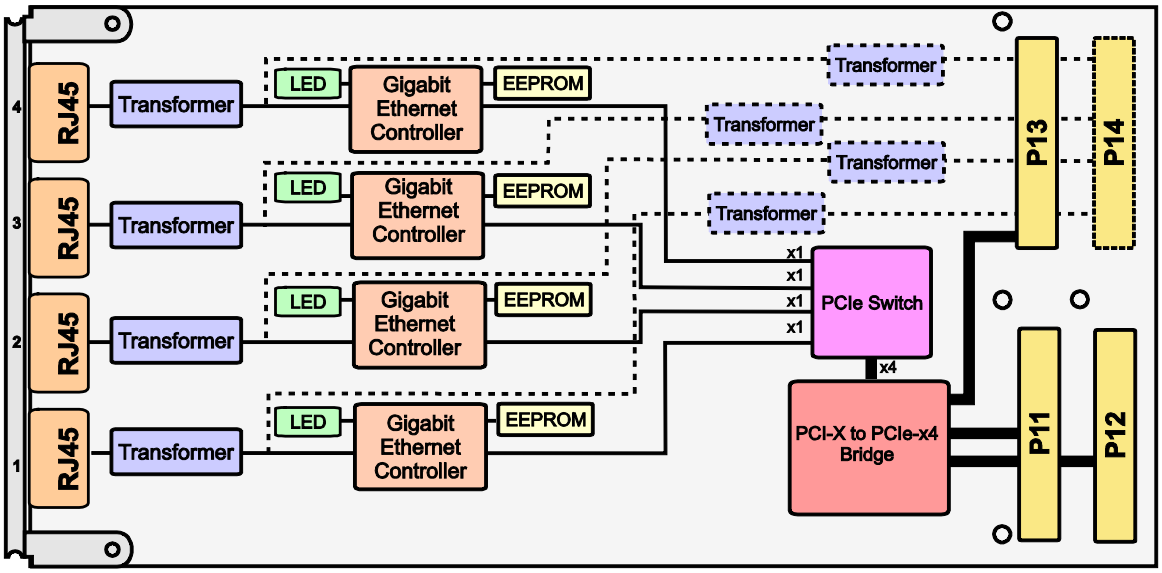

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1 Single Size	
Electrical Interface	PCI Rev. 3.0 compliant and PCI-X Rev. 2.0a compliant 66 MHz / 64 bit PCI and 133 MHz / 64 bit PCI-X 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
PCI/PCI-X to PCIe Bridge	PI7C9X130 (Pericom)	
PCIe Switch	89HPES8T5A (IDT)	
Gigabit Ethernet Controller	For each interface: 82574IT (Intel)	
Ethernet Interface		
Number of Interfaces	2/4	
FIFO	For each interface: Configurable receive and transmit data FIFO, programmable in 1 KB increments	
Interrupts	Using PCI INTA, INTB, INTC and INTD	
I/O Connector	TPMC885-x0R: RJ45 jacks (Tyco 406732-2 or compatible) TPMC885-x1R: PMC P14 back I/O (Molex 71436-2864 or compatible)	
Physical Data		
Ambient Air Cooling	Constant airflow of 2 m/s required	
Power Requirements	1700 mA typical @ +3.3V DC (four channel, no link) app. additional 70mA per 100 Mbit/s link app. additional 300mA per 1 Gbit/s link	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +85°C
MTBF	TPMC885-10R: 359000 h TPMC885-11R: 502000 h TPMC885-20R: 491000 h TPMC885-21R: 579000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	TPMC885-10R: 78 g TPMC885-11R: 68 g	

Table 2-1 : Technical Specification

3 PCI Device Topology on TPMC885

The TPMC885 uses two/four Gigabit Ethernet Controllers (Intel 82574IT) each communicating via a PCIe Rev. 1.1 compliant x1 Interface. To be able to access the Ethernet controllers they are connected to the x1 Downstream Ports of a PCIe Switch (IDT 89HPES8T5A). The x4 Upstream Port of the Switch is connected to a PCI/PCI-X to PCIe Bridge (Pericom PI7C9X130) which communicates with the host system.

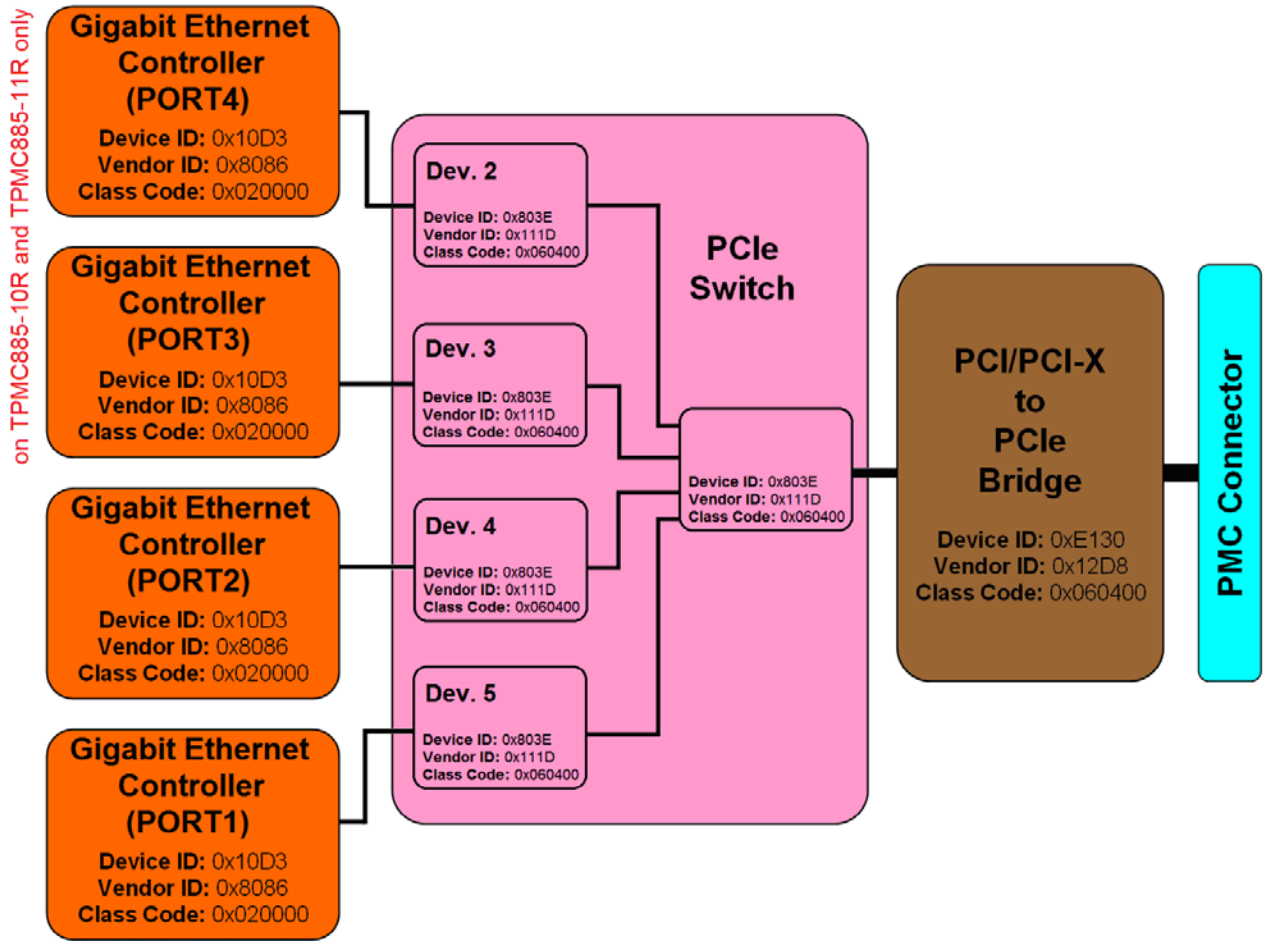

Figure 3-1 : PCI Device Topology

NOTE: Operating systems typically assign the lowest available Ethernet device number to PORT4 or PORT2 (ETHERNET 4 or ETHERNET 2 interface on I/O Connector P14), thus initializing the four or two ports in descending order.

4 Gigabit Ethernet Controller

4.1 Intel 82574IT PCI Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				Initial Values (Hex Values)
	31 24	23 16	15 8	7 0	
0x00	Device ID		Vendor ID		10D3 8086
0x04	Status Register		Command Register		0010 0000
0x08	Class Code			Revision ID	020000 00
0x0C	BIST	Header Type	Latency Timer	Cache Line Size	00 00 00 10
0x10	Base Address 0 (Memory BAR)				FFFE0000 (128 KByte)
0x14	Base Address 1 (Flash BAR)				00000000
0x18	Base Address 2 (IO BAR)				FFFFFFE1 (32 Byte)
0x1C	Base Address 3 (MSI-X BAR)				FFFFC000 (16 KByte)
0x20	Base Address 4				00000000
0x24	Base Address 5				00000000
0x28	CardBus CIS Pointer				00000000
0x2C	Subsystem ID		Subsystem Vendor ID		0000 8086
0x30	Expansion ROM Base Address				00000000
0x34	Reserved			Cap_Ptr	000000 C8
0x38	Reserved				00000000
0x3C	Max_Latency	Min_Grant	Interrupt Pin	Interrupt Line	00 00 01 00

Table 4-1 : Intel 82574IT PCI Header

5 LEDs

The TPMC885 provides two/four Status LEDs for quick visual inspection and debugging. Due to the fact that PMCs are mounted headfirst on the carrier card, the LED indicators are visible on the back side of the TPMC885. A marking is placed close to each LED, to indicate the Ethernet Port the LED corresponds to.

Each Ethernet Port has one LED indicator. See figures below for more details:

LED Status	Description
OFF	No cable is connected or no link is established
ON	A link is established at the corresponding Ethernet Port
BLINKING	Indicates activity: The Ethernet Port transmits or receives data

Table 5-1 : LED Status

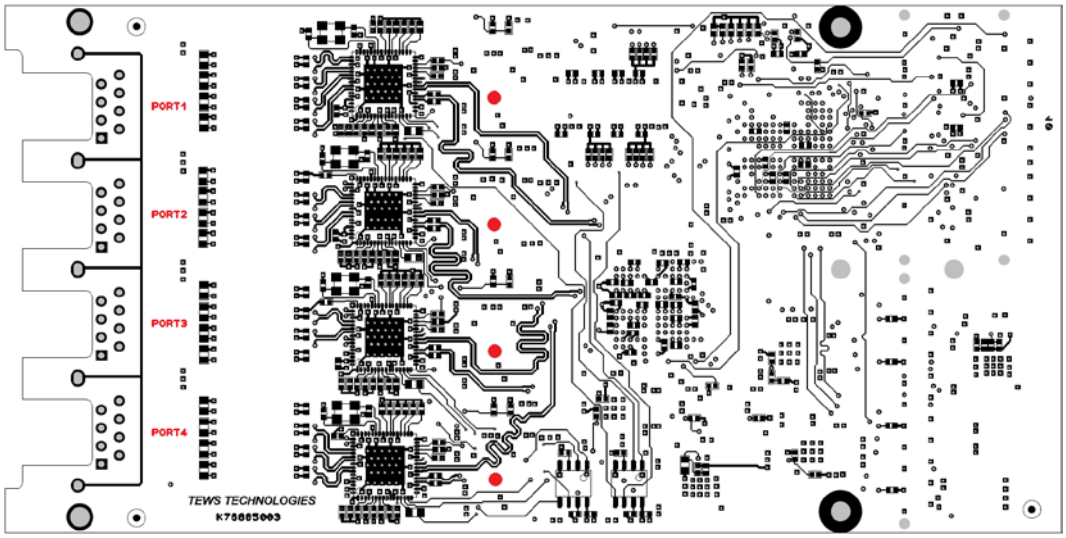

Figure 5-1 : LEDs and markings (TPMC885-x0R bottom view)

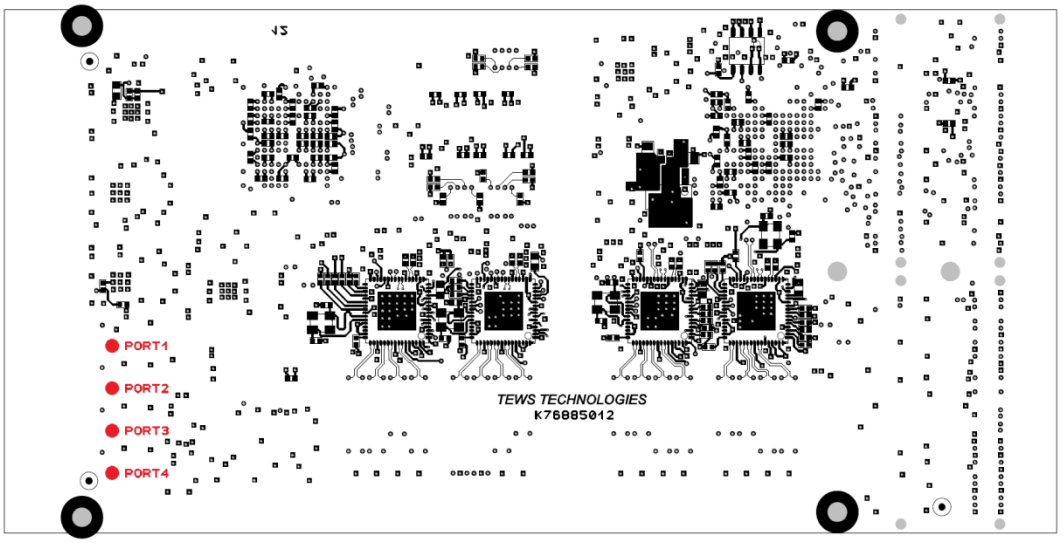

Figure 5-2 : LEDs and markings (TPMC885-x1R bottom view)

6 Pin Assignment – I/O Connectors

6.1 TPMC885-10R

On the TPMC885-10R, the Ethernet signals are accessible by four RJ45 jacks. The connectors are located in the PMC front panel.

For pin assignment and front panel labeling, see the figures below.

Pin	Signal (1000)	Signal (100, 10)
1	TX0/RX0+	TX+
2	TX0/RX0-	TX-
3	TX1/RX1+	RX+
4	TX2/RX2+	not used
5	TX2/RX2-	not used
6	TX1/RX1-	RX-
7	TX3/RX3+	not used
8	TX3/RX3-	not used

Table 6-1 : Front I/O pin assignment

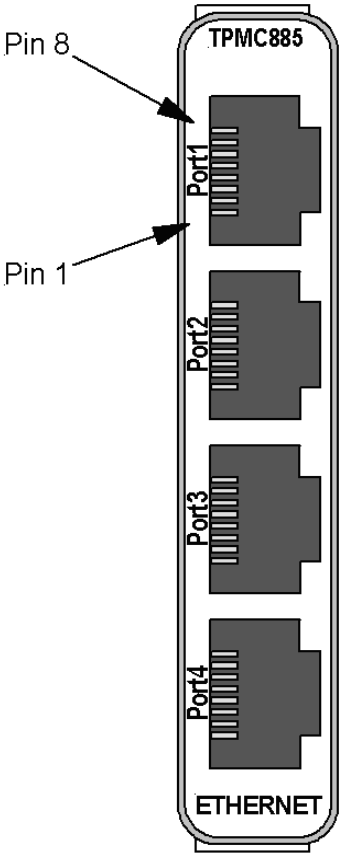

Figure 6-1 : TPMC885-10R front panel view

6.2 TPMC885-11R

The TPMC885-11R routes the Ethernet lines to the P14 mezzanine connector. In most cases, the P14 is connected to the PMC Carrier that routes the Ethernet lines from P14 to the Backplane. A Transition Module is connected to the backside of the Backplane and routes the Ethernet lines to the RJ45. Care must be taken to avoid impedance mismatches and high resistive routing in the Ethernet lines, because this leads to signal distortion and low voltage amplitude.

Pin	Signal	Pin	Signal
1	Termination Plane	2	Termination Plane
3	ETHERNET 4 TX3/RX3+	4	ETHERNET 3 TX3/RX3+
5	ETHERNET 4 TX3/RX3-	6	ETHERNET 3 TX3/RX3-
7	Termination Plane	8	Termination Plane
9	ETHERNET 4 TX2/RX2+	10	ETHERNET 3 TX2/RX2+
11	ETHERNET 4 TX2/RX2-	12	ETHERNET 3 TX2/RX2-
13	Termination Plane	14	Termination Plane
15	ETHERNET 4 TX0/RX0+	16	ETHERNET 4 TX1/RX1+
17	Termination Plane	18	Termination Plane
19	ETHERNET 4 TX0/RX0-	20	ETHERNET 4 TX1/RX1-
21	Termination Plane	22	Termination Plane
23	Termination Plane	24	Termination Plane
25	ETHERNET 3 TX0/RX0+	26	ETHERNET 3 TX1/RX1+
27	Termination Plane	28	Termination Plane
29	ETHERNET 3 TX0/RX0-	30	ETHERNET 3 TX1/RX1-
31	Termination Plane	32	Termination Plane
33	Termination Plane	34	Termination Plane
35	ETHERNET 2 TX0/RX0+	36	ETHERNET 2 TX1/RX1+
37	Termination Plane	38	Termination Plane
39	ETHERNET 2 TX0/RX0-	40	ETHERNET 2 TX1/RX1-
41	Termination Plane	42	Termination Plane
43	Termination Plane	44	Termination Plane
45	ETHERNET 1 TX0/RX0+	46	ETHERNET 1 TX1/RX1+
47	Termination Plane	48	Termination Plane
49	ETHERNET 1 TX0/RX0-	50	ETHERNET 1 TX1/RX1-
51	Termination Plane	52	Termination Plane
53	ETHERNET 2 TX2/RX2+	54	ETHERNET 1 TX2/RX2+
55	ETHERNET 2 TX2/RX2-	56	ETHERNET 1 TX2/RX2-
57	Termination Plane	58	Termination Plane
59	ETHERNET 2 TX3/RX3+	60	ETHERNET 1 TX3/RX3+
61	ETHERNET 2 TX3/RX3-	62	ETHERNET 1 TX3/RX3-
63	Termination Plane	64	Termination Plane

Table 6-2 : TPMC885-11R Back I/O P14 pin assignment

6.3 TPMC885-20R

On the TPMC885-20R, the Ethernet signals are accessible by two RJ45 jacks. The connectors are located in the PMC front panel.

For pin assignment and front panel labeling, see the figures below.

Pin	Signal (1000)	Signal (100, 10)
1	TX0/RX0+	TX+
2	TX0/RX0-	TX-
3	TX1/RX1+	RX+
4	TX2/RX2+	not used
5	TX2/RX2-	not used
6	TX1/RX1-	RX-
7	TX3/RX3+	not used
8	TX3/RX3-	not used

Table 6-3 : Front I/O pin assignment

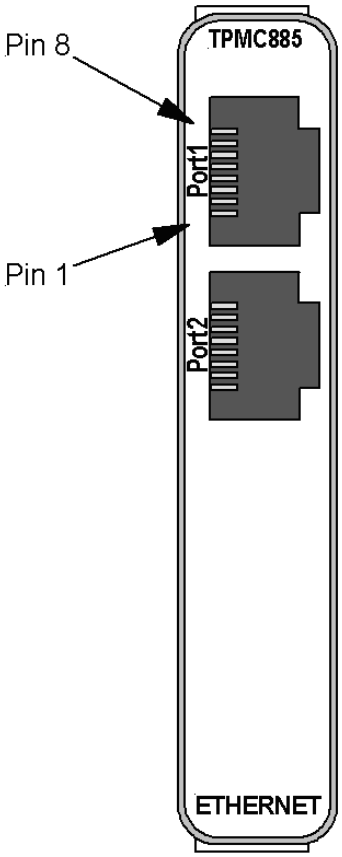

Figure 6-2 : TPMC885-20R front panel view

6.4 TPMC885-21R

The TPMC885-21R routes the Ethernet lines to the P14 mezzanine connector. In most cases, the P14 is connected to the PMC Carrier that routes the Ethernet lines from P14 to the Backplane. A Transition Module is connected to the backside of the Backplane and routes the Ethernet lines to the RJ45. Care must be taken to avoid impedance mismatches and high resistive routing in the Ethernet lines, because this leads to signal distortion and low voltage amplitude.

Pin	Signal	Pin	Signal
1	Termination Plane	2	Termination Plane
3	not connected	4	not connected
5	not connected	6	not connected
7	Termination Plane	8	Termination Plane
9	not connected	10	not connected
11	not connected	12	not connected
13	Termination Plane	14	Termination Plane
15	not connected	16	not connected
17	Termination Plane	18	Termination Plane
19	not connected	20	not connected
21	Termination Plane	22	Termination Plane
23	Termination Plane	24	Termination Plane
25	not connected	26	not connected
27	Termination Plane	28	Termination Plane
29	not connected	30	not connected
31	Termination Plane	32	Termination Plane
33	Termination Plane	34	Termination Plane
35	ETHERNET 2 TX0/RX0+	36	ETHERNET 2 TX1/RX1+
37	Termination Plane	38	Termination Plane
39	ETHERNET 2 TX0/RX0-	40	ETHERNET 2 TX1/RX1-
41	Termination Plane	42	Termination Plane
43	Termination Plane	44	Termination Plane
45	ETHERNET 1 TX0/RX0+	46	ETHERNET 1 TX1/RX1+
47	Termination Plane	48	Termination Plane
49	ETHERNET 1 TX0/RX0-	50	ETHERNET 1 TX1/RX1-
51	Termination Plane	52	Termination Plane
53	ETHERNET 2 TX2/RX2+	54	ETHERNET 1 TX2/RX2+
55	ETHERNET 2 TX2/RX2-	56	ETHERNET 1 TX2/RX2-
57	Termination Plane	58	Termination Plane
59	ETHERNET 2 TX3/RX3+	60	ETHERNET 1 TX3/RX3+
61	ETHERNET 2 TX3/RX3-	62	ETHERNET 1 TX3/RX3-
63	Termination Plane	64	Termination Plane

Table 6-4 : TPMC885-21R Back I/O P14 pin assignment