The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC895

Dual/Four Channel 10/100/1000 Mbit/s Ethernet

Version 1.0

User Manual

Issue 1.0.1

December 2021

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TPMC895-10R

Four Channel 10/100/1000 Mbit/s Ethernet, Intel I210IT, RJ45

(RoHS compliant)

TPMC895-11R

Four Channel 10/100/1000 Mbit/s Ethernet, Intel I210IT, P14 Back I/O

(RoHS compliant)

TPMC895-20R

Two Channel 10/100/1000 Mbit/s Ethernet, Intel I210IT, RJ45

(RoHS compliant)

TPMC895-21R

Two Channel 10/100/1000 Mbit/s Ethernet, Intel I210IT, P14 Back I/O

(RoHS compliant)

TPMC895-30R

Four Channel 10/100/1000 Mbit/s Ethernet, Intel I210IT, RJ45, IEEE 1588 auxiliary devices via P14

(RoHS compliant)

Issue	Description	Date
1.0.0	Initial issue	January 2021
1.0.1	Issue after Revision Update to V1.0 Rev.B	December 2021

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1 Product Description

The TPMC895 is a PCI Mezzanine Card (PMC) compatible module providing a dual or four channel Ethernet 10Base-T / 100Base-TX / 1000Base-T interface.

A transparent 64 bit, up to 133 MHz PCI-X/PCI to PCIe Bridge and a PCIe Switch provide access to the Intel I210IT Gigabit Ethernet controllers. Each Ethernet interface supports 10, 100 and 1000 Mbit/s transmission rates and is equipped with a 16 Mbit Serial Flash to support PXE and iSCSI boot.

The two/four Ethernet interfaces of the TPMC895 are capable of performing an auto negotiation algorithm which allows both link-partners to determine the best link-parameters. The TPMC895 supports IEEE 1588/802.1AS Precision Time Protocol (PTP) and IEEE 802.1Qav Audio/Video Bridging (AVB) traffic shaping (with software extensions).

The TPMC895-10R provides four 10/100/1000 Mbit/s Ethernet connections via front panel RJ45 connectors.

The TPMC895-11R routes four Ethernet ports to the Back I/O P14 connector without any RJ45 connector at the front.

The TPMC895-20R provides two 10/100/1000 Mbit/s Ethernet connections via front panel RJ45 connectors.

The TPMC895-21R routes two Ethernet ports to the Back I/O P14 connector without any RJ45 connector at the front.

The TPMC895-30R is a TPMC895-10R with an additional Back I/O P14 connector for IEEE 1588 auxiliary device connections.

All ports are galvanically isolated from the Ethernet controllers and LEDs on the board indicate the different network activities.

The module meets the requirements to operate in extended temperature range from -40°C to +85°C.

Software Support:

- Software support for Intel I210IT at www.intel.com
- For operating systems not supported by Intel, please contact TEWS.

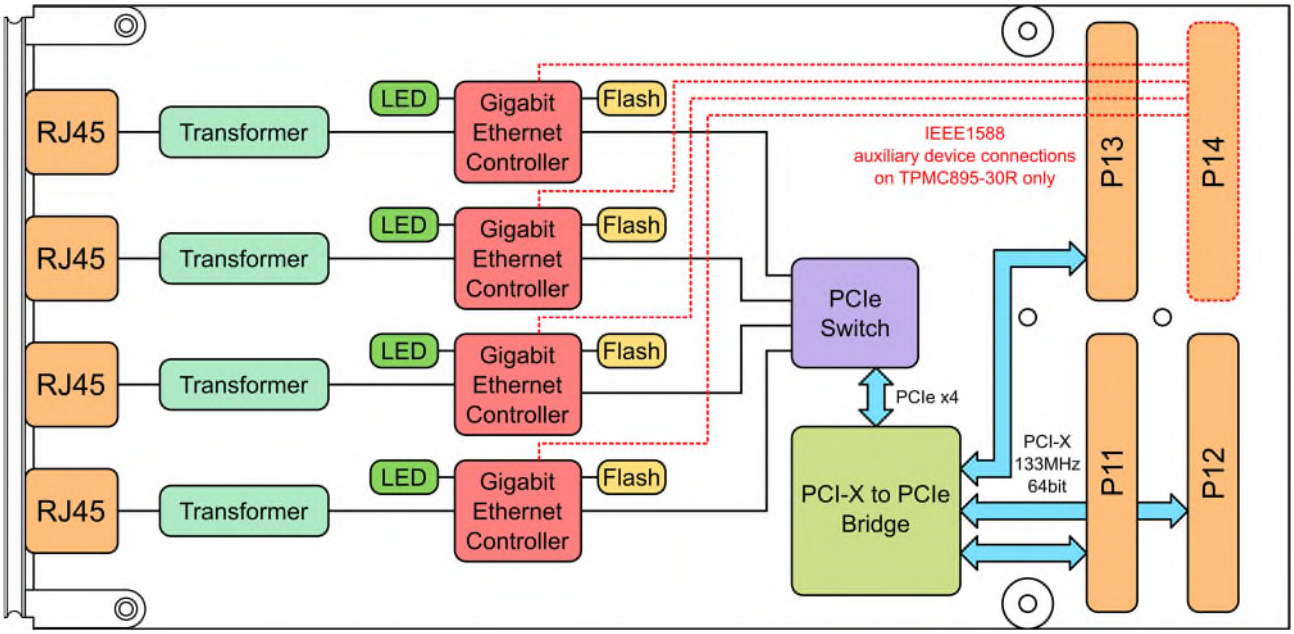


Figure 1-1 : Block Diagram RJ45

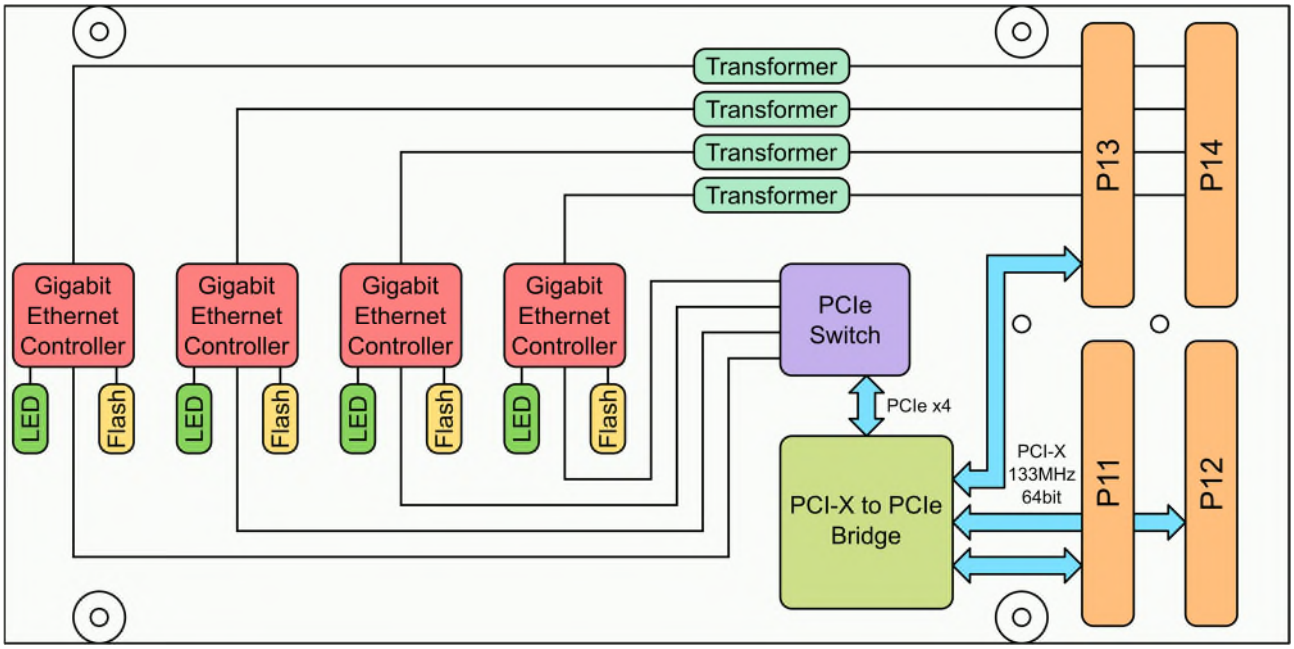


Figure 1-2 : Block Diagram P14 Back I/O

2 Technical Specification

PMC Interface	
Mechanical Interface	PCI Mezzanine Card (PMC) Interface conforming to IEEE P1386/P1386.1 Standard single-width (149 mm x 74 mm)
Electrical Interface	64 bit PCI (Specification 3.0) up to 66 MHz and 64 bit PCI-X (Specification 2.0a) up to 133 MHz compliant interface conforming to 3.3V PCI signaling with 5V I/O tolerance

On Board Devices	
PCI/PCI-X to PCIe Bridge	PI7C9X130 (Diodes Incorporated)
PCIe Switch	PI7C9X2G608GP (Diodes Incorporated)
Gigabit Ethernet Controllers	For each interface: I210-IT (Intel)
16 Mbit Serial Flashes for Boot ROM	For each interface: W25Q16JV (Winbond)

I/O Interface	
Number of Channels	2/4
I/O Standards	1000Base-T 100Base-TX 10Base-T
I/O Connector	TPMC895-x0R: RJ45 (TE Connectivity 406732 or compatible) TPMC895-x1R: Back I/O P14 (Molex 714362864 or compatible)

Physical Data		
Power Requirements	1000mA typical @ +5V (four channel, no link) app. additional 10mA to 100mA per link	
Temperature Range	Operating Storage	-40°C to +85°C (constant airflow of 2m/s is required) -40°C to +85°C
MTBF	TPMC895-10R: 427000 h TPMC895-11R: 587000 h TPMC895-20R: 593000 h TPMC895-21R: 679000 h TPMC895-30R: 389000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	

Weight	TPMC895-10R: 83 g TPMC895-11R: 72 g TPMC895-20R: 73 g TPMC895-21R: 69 g TPMC895-30R: 85 g

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This PMC module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with appropriate care.

3.2 Power Dissipation

This PMC module requires adequate forced air cooling!

4 PCI Interface

4.1 TPMC895 PCI Device Topology

The TPMC895 uses two/four Gigabit Ethernet Controllers (Intel I210-IT) each communicating via a PCIe Rev. 2.1 compliant x1 Interface.

To be able to access the Ethernet controllers they are connected to the x1 Downstream Ports of a PCIe Switch (Diodes Incorporated PI7C9X2G608GP).

The x4 Upstream Port of the PCIe Switch is connected to a PCI/PCI-X to PCIe Bridge (Diodes Incorporated PI7C9X130) which communicates with the host system.

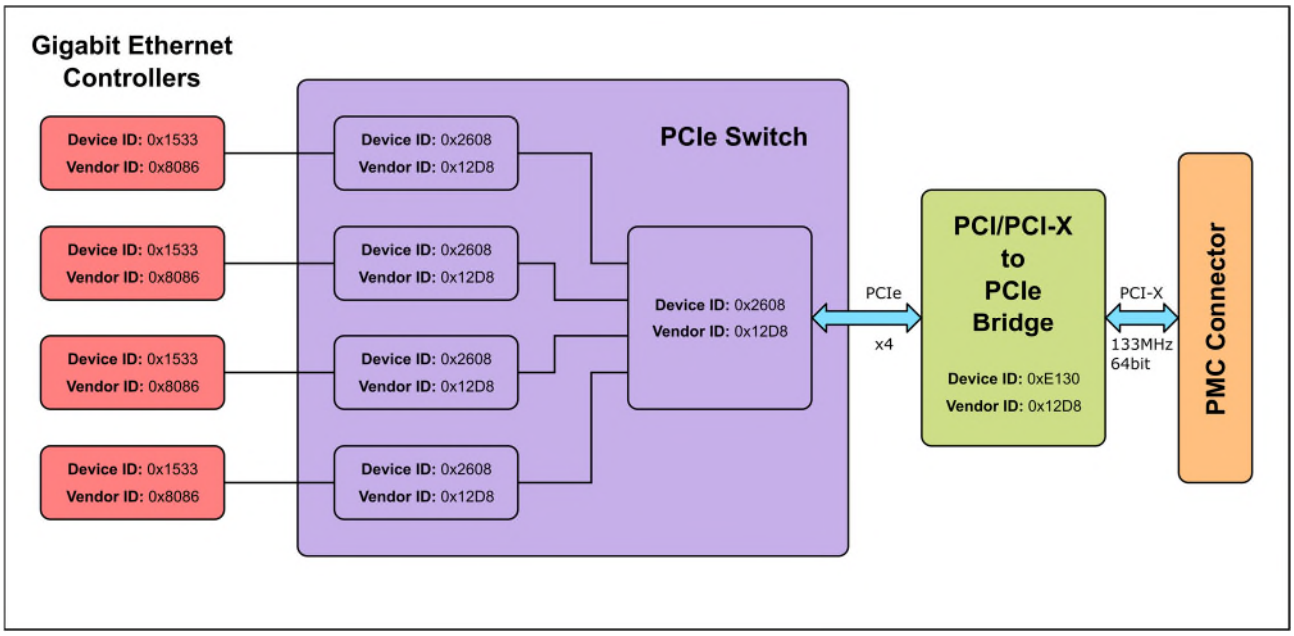


Figure 4-1 : TPMC895 PCI Device Topology

4.2 TPMC895 PCI Memory and I/O Size Requirements

PCI Space Mapping	Four Channel (Byte)	Two Channel (Byte)
MEM	4M	2M
I/O	16K	8K

Table 4-1 : TPMC895 PCI Memory and I/O Size Requirements

4.3 I210 PCI Identifiers

Vendor-ID	0x8086 (Intel)
Device-ID	0x1533 (I210-IT copper only)
Class Code	0x020000 (Ethernet Controller)
Subsystem Vendor-ID	0xFFFF
Subsystem Device-ID	0x0000

Table 4-2 : I210 PCI Identifiers

4.4 I210 PCI Base Address Register Configuration

PCI Base Address Register (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Description
0 (0x10)	MEM	128K	Internal Registers
1 (0x14)	-	-	-
2 (0x18)	I/O	32	Internal Registers via I/O Space
3 (0x1C)	MEM	16K	MSI-X

Table 4-3 : I210 PCI Base Address Register Configuration

5 Ethernet Interface Status LEDs

The TPMC895 provides an individual Status LED for every Ethernet Interface. Due to the fact that PMCs are mounted upside-down on the carrier card the Status LEDs are visible on the back side of the TPMC895. A marking is placed close to each Status LED to indicate the Ethernet Port it corresponds to.

See table below for more details:

Status LED	Description
OFF	No cable is connected or no link is established
ON	A link is established
BLINKING	Activity (the Ethernet Port transmits or receives data)

Table 5-1 : Status LED

6 Synchronization with IEEE 1588 Auxiliary Devices

The TPMC895 supports IEEE 1588/802.1AS Precision Time Protocol (PTP).

If you additionally want to synchronize with IEEE 1588 auxiliary devices, this can be realized with TPMC895-30R via the Ethernet Controllers' GPIO Software-Definable Pins (SDPx) that are connected to the Back I/O P14 connector.

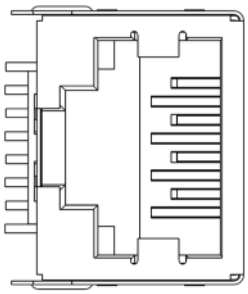
The electrical characteristics of the Ethernet Controllers' GPIO Pins are listed in the following table:

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -8 mA; VCC3P3 = Min	2.4		V
		I_{OH} = -100 µA; VCC3P3 = Min	VCC3P3 - 0.2		V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA; VCC = Min		0.4	V
		I_{OL} = 100 µA; VCC = Min		0.2	V
V_{IH}	Input High Voltage		0.7 * VCC3P3	VCC3P3 + 0.4	V
V_{IL}	Input Low Voltage		-0.4	0.3 * VCC3P3	V

Table 6-1 : Electrical characteristics of Ethernet Controllers' GPIO Pins

7 Pin Assignment – I/O Connectors

7.1 RJ45 Connector



Pin	Signal (1000Base-T)	Signal (100Base-TX/10Base-T)
1	TX0/RX0+	TX+
2	TX0/RX0-	TX-
3	TX1/RX1+	RX+
4	TX2/RX2+	not used
5	TX2/RX2-	not used
6	TX1/RX1-	RX-
7	TX3/RX3+	not used
8	TX3/RX3-	not used

Table 7-1 : RJ45 Connector

7.2 Back I/O P14 Connector (TPMC895-11R)

Signal	Pin		Pin	Signal
TERM_PLANE	63		64	TERM_PLANE
ETHERNET_2_TX3/RX3-	61		62	ETHERNET_1_TX3/RX3-
ETHERNET_2_TX3/RX3+	59		60	ETHERNET_1_TX3/RX3+
TERM_PLANE	57		58	TERM_PLANE
ETHERNET_2_TX2/RX2-	55		56	ETHERNET_1_TX2/RX2-
ETHERNET_2_TX2/RX2+	53		54	ETHERNET_1_TX2/RX2+
TERM_PLANE	51		52	TERM_PLANE
ETHERNET_1_TX0/RX0-	49		50	ETHERNET_1_TX1/RX1-
TERM_PLANE	47		48	TERM_PLANE
ETHERNET_1_TX0/RX0+	45		46	ETHERNET_1_TX1/RX1+
TERM_PLANE	43		44	TERM_PLANE
TERM_PLANE	41		42	TERM_PLANE
ETHERNET_2_TX0/RX0-	39		40	ETHERNET_2_TX1/RX1-
TERM_PLANE	37		38	TERM_PLANE
ETHERNET_2_TX0/RX0+	35		36	ETHERNET_2_TX1/RX1+
TERM_PLANE	33		34	TERM_PLANE
TERM_PLANE	31		32	TERM_PLANE
ETHERNET_3_TX0/RX0-	29		30	ETHERNET_3_TX1/RX1-
TERM_PLANE	27		28	TERM_PLANE
ETHERNET_3_TX0/RX0+	25		26	ETHERNET_3_TX1/RX1+
TERM_PLANE	23		24	TERM_PLANE
TERM_PLANE	21		22	TERM_PLANE
ETHERNET_4_TX0/RX0-	19		20	ETHERNET_4_TX1/RX1-
TERM_PLANE	17		18	TERM_PLANE
ETHERNET_4_TX0/RX0+	15		16	ETHERNET_4_TX1/RX1+
TERM_PLANE	13		14	TERM_PLANE
ETHERNET_4_TX2/RX2-	11		12	ETHERNET_3_TX2/RX2-
ETHERNET_4_TX2/RX2+	9		10	ETHERNET_3_TX2/RX2+
TERM_PLANE	7		8	TERM_PLANE
ETHERNET_4_TX3/RX3-	5		6	ETHERNET_3_TX3/RX3-
ETHERNET_4_TX3/RX3+	3		4	ETHERNET_3_TX3/RX3+
TERM_PLANE	1		2	TERM_PLANE

Table 7-2 : Back I/O P14 Connector (TPMC895-11R)

7.3 Back I/O P14 Connector (TPMC895-21R)

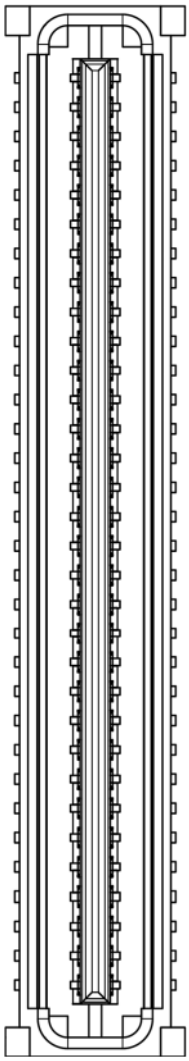
Signal	Pin		Pin	Signal
TERM_PLANE	63		64	TERM_PLANE
ETHERNET_2_TX3/RX3-	61		62	ETHERNET_1_TX3/RX3-
ETHERNET_2_TX3/RX3+	59		60	ETHERNET_1_TX3/RX3+
TERM_PLANE	57		58	TERM_PLANE
ETHERNET_2_TX2/RX2-	55		56	ETHERNET_1_TX2/RX2-
ETHERNET_2_TX2/RX2+	53		54	ETHERNET_1_TX2/RX2+
TERM_PLANE	51		52	TERM_PLANE
ETHERNET_1_TX0/RX0-	49		50	ETHERNET_1_TX1/RX1-
TERM_PLANE	47		48	TERM_PLANE
ETHERNET_1_TX0/RX0+	45		46	ETHERNET_1_TX1/RX1+
TERM_PLANE	43		44	TERM_PLANE
TERM_PLANE	41		42	TERM_PLANE
ETHERNET_2_TX0/RX0-	39		40	ETHERNET_2_TX1/RX1-
TERM_PLANE	37		38	TERM_PLANE
ETHERNET_2_TX0/RX0+	35		36	ETHERNET_2_TX1/RX1+
TERM_PLANE	33		34	TERM_PLANE
TERM_PLANE	31		32	TERM_PLANE
NC	29		30	NC
TERM_PLANE	27		28	TERM_PLANE
NC	25		26	NC
TERM_PLANE	23		24	TERM_PLANE
TERM_PLANE	21		22	TERM_PLANE
NC	19		20	NC
TERM_PLANE	17		18	TERM_PLANE
NC	15		16	NC
TERM_PLANE	13		14	TERM_PLANE
NC	11		12	NC
NC	9		10	NC
TERM_PLANE	7		8	TERM_PLANE
NC	5		6	NC
NC	3		4	NC
TERM_PLANE	1		2	TERM_PLANE

Table 7-3 : Back I/O P14 Connector (TPMC895-21R)

7.4 Back I/O P14 Connector (TPMC895-30R)

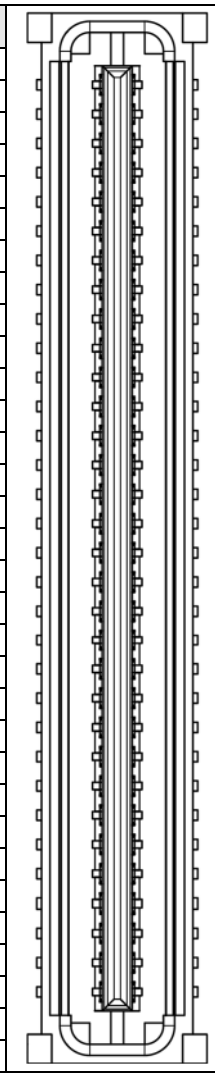
Signal	Pin		Pin	Signal
NC	63		64	NC
NC	61		62	NC
NC	59		60	NC
NC	57		58	NC
NC	55		56	NC
NC	53		54	NC
NC	51		52	NC
NC	49		50	NC
NC	47		48	NC
NC	45		46	NC
NC	43		44	NC
NC	41		42	NC
NC	39		40	NC
NC	37		38	NC
NC	35		36	NC
GND	33		34	ETHERNET_4_SDP3
GND	31		32	ETHERNET_4_SDP2
GND	29		30	ETHERNET_4_SDP1
GND	27		28	ETHERNET_4_SDP0
GND	25		26	ETHERNET_3_SDP3
GND	23		24	ETHERNET_3_SDP2
GND	21		22	ETHERNET_3_SDP1
GND	19		20	ETHERNET_3_SDP0
GND	17		18	ETHERNET_2_SDP3
GND	15		16	ETHERNET_2_SDP2
GND	13		14	ETHERNET_2_SDP1
GND	11		12	ETHERNET_2_SDP0
GND	9		10	ETHERNET_1_SDP3
GND	7		8	ETHERNET_1_SDP2
GND	5		6	ETHERNET_1_SDP1
GND	3		4	ETHERNET_1_SDP0
NC	1		2	NC

Table 7-4 : Back I/O P14 Connector (TPMC895-30R)