The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC901

6/4/2 Channel Extended CAN Bus Adapter

Version 1.2

User Manual

Issue 1.2.1

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TPMC901-10R

6 Channel Extended CAN Bus Interface, D-Sub male 25-pin front panel I/O, extended temperature range

TPMC901-11R

4 Channel Extended CAN Bus Interface, D-Sub male 25-pin front panel I/O, extended temperature range

TPMC901-12R

2 Channel Extended CAN Bus Interface, D-Sub male 25-pin front panel I/O, extended temperature range

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	Initial issue	September 1997
1.1	Revised manual	September 1999
1.2	General revision	May 2003
1.3	New address TEWS LLC	September 2006
1.0.4	New notation for user manual and engineering documentation	January 2009
1.1.0	Hardware minor version update to V1.1 Rev.A	February 2012
1.2.0	Hardware minor version update to V1.2 Rev.A	January 2013
1.2.1	General Revision	August 2014

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1 Product Description

The TPMC901 is a PCI Mezzanine Card (PMC) compatible module.

The TPMC901-10R provides six independent CAN Bus interfaces using six Bosch CC770F CAN Controllers. The CC770 offers pin compatibility with Intel's 82527 CAN Controller and is a function replacement. Additionally to the standard data and remote frame, all channels support the extended data and remote frame according to the CAN specification 2.0 part A and B (standard 11 bit identifier and extended 29 bit identifier).

All channels have the capability to transmit, receive and perform message filtering on extended and standard messages.

Each channel supports CAN High Speed according to ISO11898 as the physical interface. The bus line termination is selectable by a jumper separate for each bus line pair. The data transfer rates of up to 1 Mbps are supported for a bus line length of 40 m.

The TPMC901-11R supports four CAN Bus channels and the TPMC901-12R has two CAN Bus channels.

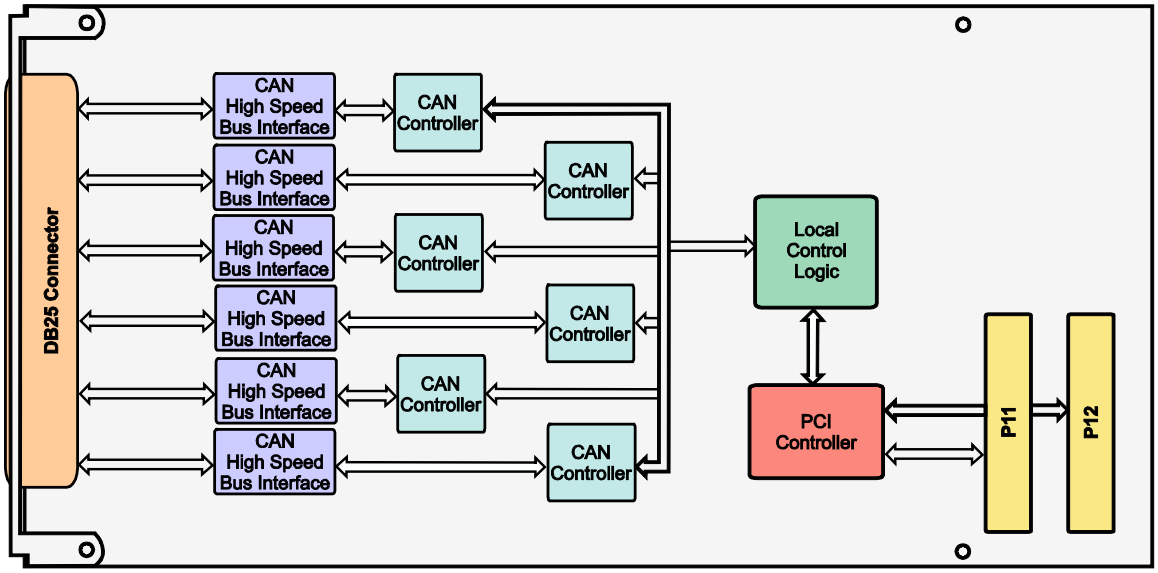

Figure 1-1 : Block Diagram

2 Technical Specification

PMC Interface		
Mechanical Interface	PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1 Single Size	
Electrical Interface	PCI Rev. 2.2 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage	
On Board Devices		
PCI Target Chip	PCI9030 (PLX Technology)	
Local Control Logic	XC9572XL (Xilinx)	
CAN Controller	For each interface: CC770F (Bosch) @ 8 MHz	
CAN Transceiver	For each interface: TJA1050 (NXP)	
Physical Interface	CAN High Speed (according to ISO 11898)	
Bus Line Termination	On board 120Ω, selectable by jumper for each channel	
Transfer Rate	The TJA1050 High-Speed CAN Transceiver supports bit rates from 60 kbit/s up to 1 Mbit/s 1 Mbit/s -> maximum bus line length 40 m	
I/O Interface		
Number of Channels	TPMC901-10R: 6 channels TPMC901-11R: 4 channels TPMC901-12R: 2 channels	
I/O Connector	D-Sub male 25-pin (Harting 09653626816 or compatible)	
Physical Data		
Power Requirements	TPMC901-10R: 165mA typical @ +5V DC 130mA typical @ +3.3V DC	
Temperature Range	Operating Storage	-40°C to +85°C -40°C to +105°C
MTBF	TPMC901-10R: 621000 h TPMC901-11R: 632000 h TPMC901-12R: 645000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	TPMC901-10R: 81 g	

Table 2-1 : Technical Specification

3 Local Space Addressing

3.1 PCI9030 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9030 local spaces.

PCI9030 Local Space	PCI9030 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	2 (0x18)	MEM	s.b.	8	LITTLE	CAN Controller Space
1	3 (0x1C)	I/O	4	8	LITTLE	Interrupt Status Space
2	4 (0x20)	-	-	-	-	Local Address Space 2
3	5 (0x24)	-	-	-	-	Local Address Space 3

Table 3-1 : PCI9030 Local Space Configuration

Size of CAN Controller Space: TPMC901-10R: 2048 byte
TPMC901-11R: 1024 byte
TPMC901-12R: 512 byte

3.2 CAN Controller Space

PCI Base Address: **PCI9030 PCI Base Address 2 (Offset 0x18 in PCI Configuration Space).**

The complete CAN Controllers' register sets of the TPMC901 are accessible in the CAN Controller Space of the PMC module. Each register set has a size of 256byte.

The TPMC901-10R uses all six channels (CANCH0 to CANCH5), the TPMC901-11R uses only the channels CANCH0 to CANCH3 and the TPMC901-12R uses only the channels CANCH0 and CANCH1.

Offset to PCI Base Address 2	CAN Controller channel	TPMC901-10R	TPMC901-11R	TPMC901-12R
0x000	CAN Controller channel 0 (CANCH0)	X	X	X
0x100	CAN Controller channel 1 (CANCH1)	X	X	X
0x200	CAN Controller channel 2 (CANCH2)	X	X	
0x300	CAN Controller channel 3 (CANCH3)	X	X	
0x400	CAN Controller channel 4 (CANCH4)	X		
0x500	CAN Controller channel 5 (CANCH5)	X		

Table 3-2 : CAN Controller Space

3.2.1 CAN Controller Register Set

Each CAN Controller Register Set includes 256 8bit locations that provide device configuration registers and message storage.

Offset to CANCHx	Register Name	Size (Bit)
0x00	Control Register	8
0x01	Status Register	8
0x02	CPU Interface Register	8
0x03	Reserved	8
0x04 – 0x05	High Speed Read Register	16
0x06 – 0x07	Global Mask – Standard	16
0x08 – 0x0B	Global Mask – Extended	32
0x0C – 0x0F	Message 15 Mask	32
0x10 – 0x1E	Message Object 1	120
0x1F	CLKOUT Register	8
0x20 – 0x2E	Message Object 2	120
0x2F	Bus Configuration Register	8
0x30 – 0x3E	Message Object 3	120
0x3F	Bit Timing Register 0	8
0x40 – 0x4E	Message Object 4	120
0x4F	Bit Timing Register 1	8
0x50 – 0x5E	Message Object 5	120
0x5F	Interrupt Register	8
0x60 – 0x6E	Message Object 6	120
0x6F	Reserved	8
0x70 – 0x7E	Message Object 7	120
0x7F	Reserved	8
0x80 – 0x8E	Message Object 8	120
0x8F	Reserved	8
0x90 – 0x9E	Message Object 9	120
0x9F	P1CONF Register	8
0xA0 - 0xAE	Message Object 10	120
0xAF	P2CONF Register	8
0xB0 - 0xBE	Message Object 11	120
0xBF	P1IN Register	8
0xC0 - 0xCE	Message Object 12	120
0xCF	P2IN Register	8
0xD0 - 0xDE	Message Object 13	120
0xDF	P1OUT Register	8
0xE0 - 0xEE	Message Object 14	120
0xEF	P2OUT Register	8
0xF0 - 0xFE	Message Object 15	120
0xFF	Serial Reset Address Register	8

Table 3-3 : CAN Controller Address Map

3.2.1.1 Message Object Structure

The CAN Controller Register Set contains 15 Message Objects each with a length of 15byte (120bit). The structure of each of these Message Objects is described in the following table.

Offset to Message Object x	Message Component	Size (Bit)
0x00	Control Register 0	8
0x01	Control Register 1	8
0x02	Arbitration Register 0	8
0x03	Arbitration Register 1	8
0x04	Arbitration Register 2	8
0x05	Arbitration Register 3	8
0x06	Message Configuration Register	8
0x07	Data Byte 0	8
0x08	Data Byte 1	8
0x09	Data Byte 2	8
0x0A	Data Byte 3	8
0x0B	Data Byte 4	8
0x0C	Data Byte 5	8
0x0D	Data Byte 6	8
0x0E	Data Byte 7	8

Table 3-4 : Message Object Structure

For more information about the register sets of the CAN controller refer to the user manual of the CC770F Stand Alone CAN Controller.

3.3 Interrupt Status Space

PCI Base Address:	PCI9030 PCI Base Address 3 (Offset 0x1C in PCI Configuration Space).

The Interrupt Status Register of the TPMC901 is accessible in the Interrupt Status Space of the PMC module.

Offset to PCI Base Address 3	Register Name	Size (Bit)
0x000	Interrupt Status Register (STATREG)	8

Table 3-5 : Interrupt Status Space

3.3.1 Interrupt Status Register

All CAN Controllers generate interrupts at pin INTA# of the PCI Bus. The interrupt status can be read at the Interrupt Status Register (STATREG).

The Interrupt Status Register is a byte wide read register.

Bit	Symbol	Description	Access	Reset Value
7		Always read as '1'	R	
6		Always read as '1'	R	
5	CAN5	Interrupt Status of all six channels. '0' indicates interrupt is pending on corresponding channel. TPMC901-10R: uses bits 0 to 5 TPMC901-11R: uses only bits 0 to 3 (bits 4 to 7 are always '1') TPMC901-12R: uses only bits 0 to 1 (bits 2 to 7 are always '1')	R	
4	CAN4		R	
3	CAN3		R	
2	CAN2		R	
1	CAN1		R	
0	CAN0		R	

Table 3-6 : STATREG

4 PCI9030 Target Chip

4.1 PCI Configuration Registers (PCR)

4.1.1 PCI9030 Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Hex Values
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	9050 10B5
0x04	Status		Command		Y	0280 0000
0x08	Class Code			Revision ID	N	028000 00
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers				Y	FFFFFF80
0x14	PCI Base Address 1 for I/O Mapped Config. Registers				Y	FFFFFF81
0x18	PCI Base Address 2 for CAN Controller Space				Y	FFFFF800
0x1C	PCI Base Address 3 for Interrupt Status Space				Y	FFFFFFFD
0x20	PCI Base Address 4 for Local Address Space 2				Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3				Y	00000000
0x28	PCI CardBus Information Structure Pointer				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	0385 1498
0x30	PCI Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved			New Cap. Ptr.	N	000000 40
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00
0x40	PM Cap.		PM Nxt Cap.	PM Cap. ID	N	4801 48 01
0x44	PM Data	PM CSR EXT	PM CSR		Y	00 00 0000
0x48	Reserved	HS CSR	HS Nxt Cap.	HS Cap. ID	Y[23:16]	00 80 00 06
0x4C	VPD Address		VPD Nxt Cap.	VPD Cap. ID	Y[31:16]	0000 00 03
0x50	VPD Data				Y	00000000

Table 4-1 : TPMC901-10R Example PCI Header

4.2 Local Configuration Register (LCR)

After reset, the PCI9030 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9030 Local Configuration Registers is

PCI9030 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9030 PCI Configuration Register Space)

or PCI9030 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9030 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9030 Local Configuration Registers.

Offset to PCI Base Address	Register	Value
0x00	Local Address Space 0 Range	0x0FFF_F800
0x04	Local Address Space 1 Range	0x0FFF_FFFD
0x08	Local Address Space 2 Range	0x0000_0000
0x0C	Local Address Space 3 Range	0x0000_0000
0x10	Expansion ROM Range	0x0000_0000
0x14	Local Address Space 0 Local Base Address (Remap)	0x0000_0001
0x18	Local Address Space 1 Local Base Address (Remap)	0x0000_0801
0x1C	Local Address Space 2 Local Base Address (Remap)	0x0000_0000
0x20	Local Address Space 3 Local Base Address (Remap)	0x0000_0000
0x24	Expansion ROM Local Base Address (Remap)	0x0000_0000
0x28	Local Address Space 0 Bus Region Descriptor	0x8030_7802
0x2C	Local Address Space 1 Bus Region Descriptor	0x0000_0080
0x30	Local Address Space 2 Bus Region Descriptor	0x0000_0000
0x34	Local Address Space 3 Bus Region Descriptor	0x0000_0000
0x38	Expansion ROM Bus Region Descriptor	0x0000_0000
0x3C	Chip Select 0 Base Address	0x0000_0401
0x40	Chip Select 1 Base Address	0x0000_0803
0x44	Chip Select 2 Base Address	0x0000_0000
0x48	Chip Select 3 Base Address	0x0000_0000
0x4C	Interrupt Control/Status	0x0043
0x4E	Serial EEPROM Write-Protected Address Boundary	0x0030
0x50	PCI Target Response, Serial EEPROM Control, and Initialization Control	0x0078_0000
0x54	General Purpose I/O Control	0x026D_B6D2
0x70	Hidden 1 Register for Power Management Data Select	0x0000_0000
0x74	Hidden 2 Register for Power Management Data Scale	0x0000_0000

Table 4-2 : PCI9030 Local Configuration Registers

4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9030 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values
- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values
- Address 0x88 to 0xFF : Reserved

See the PCI9030 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x9050	0x10B5	0x0280	0x0000	0x0280	0x0000	0x0385	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x0006	0x0000	0x0003	0x0FFF	s.b.	0x0FFF	0xFFFD
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0000	0x0801	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x8030	0x7802	0x0000	0x0080	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0000	s.b.	0x0000	0x0803	0x0000	0x0000
0x70	0x0000	0x0000	0x0030	0x0053	0x0078	0x0000	0x0000	0x0000
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 4-3 : Configuration EEPROM

LSW of Local Address Space 0 Range (Offset 0x2A): TPMC901-10R 0xF800

TPMC901-11R 0xFC00

TPMC901-12R 0xFE00

LSW of Chip Select 0 Base Address (Offset 0x66): TPMC901-10R 0x0401

TPMC901-11R 0x0201

TPMC901-12R 0x0101

4.4 Local Software Reset

The PCI9030 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9030 local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9030 local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of '1' resets the PCI9030 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9030 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9030 PCI and Local Configuration Registers are not reset. The PCI9030 PCI Interface is not reset.

5 CAN Bus Termination

Each end of a CAN Bus must be terminated by a 120Ω resistor between the CAN Bus lines CAN High and CAN Low.

This termination is activated by installing jumpers on the jumper field **J3**:

Jumper J3 (1-2) installed:	Bus line termination for CAN Bus channel 0 active
Jumper J3 (3-4) installed:	Bus line termination for CAN Bus channel 1 active
Jumper J3 (5-6) installed:	Bus line termination for CAN Bus channel 2 active
Jumper J3 (7-8) installed:	Bus line termination for CAN Bus channel 3 active
Jumper J3 (9-10) installed:	Bus line termination for CAN Bus channel 4 active
Jumper J3 (11-12) installed:	Bus line termination for CAN Bus channel 5 active

Factory setting for J3: Bus line termination active for all channels

Figure 5-1 : Jumper field J3

6 Pin Assignment – I/O Connector

6.1 Overview

D-Sub male 25-pin (Harting 09653626816 or compatible)

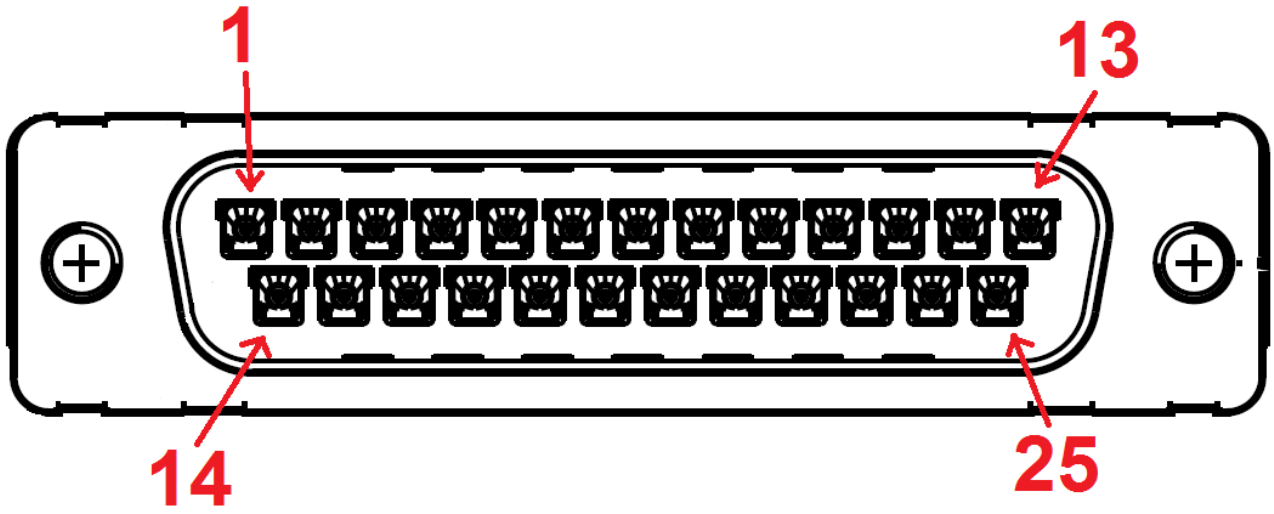

Figure 6-1 : Front I/O Connector

6.2 Pin Assignment

Pin	Signal		
	TPMC901-10R	TPMC901-11R	TPMC901-12R
01	GND	GND	GND
14	CAN Low Channel 0	CAN Low Channel 0	CAN Low Channel 0
02	CAN High Channel 0	CAN High Channel 0	CAN High Channel 0
15	GND	GND	GND
03	GND	GND	GND
16	CAN Low Channel 1	CAN Low Channel 1	CAN Low Channel 1
04	CAN High Channel 1	CAN High Channel 1	CAN High Channel 1
17	GND	GND	GND
05	GND	GND	GND
18	CAN Low Channel 2	CAN Low Channel 2	NC
06	CAN High Channel 2	CAN High Channel 2	NC
19	GND	GND	GND
07	GND	GND	GND
20	CAN Low Channel 3	CAN Low Channel 3	NC
08	CAN High Channel 3	CAN High Channel 3	NC
21	GND	GND	GND
09	GND	GND	GND
22	CAN Low Channel 4	NC	NC
10	CAN High Channel 4	NC	NC
23	GND	GND	GND
11	GND	GND	GND
24	CAN Low Channel 5	NC	NC
12	CAN High Channel 5	NC	NC
25	GND	GND	GND
13	NC	NC	NC

Table 6-1 : Pin Assignment Front I/O Connector