The Embedded I/O Company

TEWS TECHNOLOGIES

TPMC917

4MB SRAM with Battery Backup and 4 Channel RS232 Adapter

Version 1.1

User Manual

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TPMC917-10R

4MB SRAM with Battery Backup and 4 Channel RS232

TPMC917-20R

4MB SRAM with Battery Backup

TPMC917-21R

2MB SRAM with Battery Backup

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	First Issue	September 2000
1.1	General Revision	May 2003
1.2	Added Security Warning (Lithium Battery)	August 2004
1.3	TPMC917-20 added	March 2005
1.4	PCI Class Code changed, PCI Header and EEPROM Correction	June 2005
1.5	New address TEWS LLC	September 2006
1.6	TPMC917-21 added Correction in “Interrupt Status Register” description	July 2008
1.0.7	Changed / Corrected PCI9030 Configuration PROM settings User Manual Issue Notation changed	November 2008
1.0.8	Hardware revision update to Rev.H	April 2011
1.0.9	General Revision	August 2014
1.1.0	Typical data retention current changed. Chapter “Data Retention Time” added Chapter “Baud Rate Programming Formula” added	February 2018

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1 Product Description

The TPMC917 is a standard single-width 32bit PMC module providing 4MByte of SRAM with battery backup by an on board lithium cell and four ESD protected RS232 channels (TPMC917-10R only).

The 4MByte of NV-SRAM are organized in two banks, each providing 512K x 32bit of memory. During normal operation (standard 5V supply applied to the SRAM) the capacity of the lithium cell is monitored every 24 hours by a battery monitor device and an interrupt can be generated if the battery voltage is too low.

The monitor device switches the power supply of the SRAM from the standard 5V to the battery if the 5V supply drops below the battery monitor device threshold level. Any active access to the SRAM at this point is executed correctly within 1.5µs. After this time any further accesses to the SRAM are not possible.

A miniature DIP switch allows the selection of the battery backup source either from the on board lithium cell or from an external battery via the P14 I/O connector.

The TPMC917-10R provides four RS232 channels. Each channel has a programmable baud rate up to 115.2Kbaud. The 4 channel UART provides a 64Byte transmit FIFO and a 64Byte receive FIFO for each channel to significantly reduce the overhead required to provide data to and get data from the transmitter and the receiver. The FIFO trigger levels are programmable. The channels are ESD protected up to +/-15kV according to the human body model and IEC1000-4-2.

For applications which do not need the UARTs of the TPMC917-10R, the TPMC917-20R provides 4MByte of NV-SRAM without any UARTs.

The TPMC917-21R has a reduced memory size. It provides 2MByte of NV-SRAM and has no UARTs.

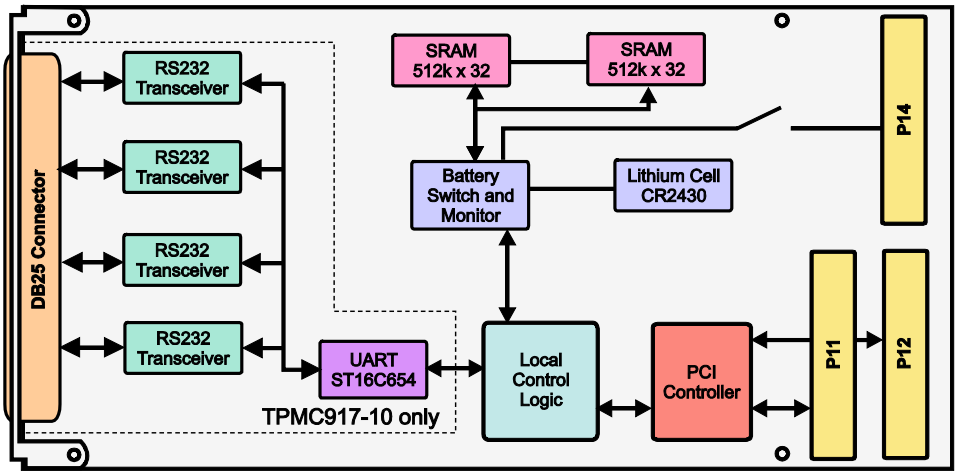

Figure 1-1 : Block Diagram

CAUTION! - This system contains a lithium battery.

Lithium batteries may explode if mishandled.

Please refer to chapter "Security Warning (Lithium Battery)".

2 Technical Specification

PMC Interface	
Mechanical Interface	PCI Mezzanine Card (PMC) Interface confirming to IEEE P1386/P1386.1 Single Size
Electrical Interface	PCI Rev. 2.2 compliant 33 MHz / 32 bit PCI 3.3V and 5V PCI Signaling Voltage
On Board Devices	
PCI Target Chip	PCI9030 (PLX Technology)

RS232 Interface (TPMC917-10R only)	
UART Controller	ST16C654
Number of RS232 Channels	4
FIFO	64Byte transmit FIFO per channel 64Byte receive FIFO per channel
Interrupts	PCI INTA for all channels, on board Interrupt Status Register
I/O Signals per Channel	TX, RX, RTS, CTS, GND
Maximum Transfer Rate	Up to 115.2Kbaud @ 2.5nF and 3kΩ load impedance
ESD Protection	+/-15kV Human Body Model, +/-6kV IEC1000-4-2 model
I/O Connector	DB25 female connector

SRAM Interface	
Memory Capacity	TPMC917-10R/20R: 4MByte, 2 banks organized as 512K x 32 TPMC917-21R: 2MByte, 1 bank organized as 512K x 32
On Board Battery Type	CR2430 Lithium Cell (285mAh capacity)
Battery Fault Voltage	2.6V typical
Battery Lifetime	@+25°C: approx. 8 years @+45°C: approx. 4 years Caused by self-discharging effects
Battery Current in Memory Backup Mode	20µA typical @ +25°C
Minimum Data Retention Voltage	2.0V minimum
5V Power Failure Threshold	4.37V typical
Max./Min. External Battery Voltage via P14 I/O	5.5V maximum / 3.0V minimum

Physical Data		
Power Requirements	+5V	300mA typical
	+12V	360µA typical (no load on serial ports, TPMC917-10R only)
	-12V	360µA typical (no load on serial ports, TPMC917-10R only)
Temperature Range	Operating Storage	0°C to +70°C -55°C to +125°C
MTBF	TPMC917-10R: 346000 h TPMC917-20R: 380000 h TPMC917-21R: 560000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	79 g	

Table 2-1 : Technical Specification

3 Local Space Addressing

3.1 PCI9030 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the PCI9030 local spaces.

PCI9030 Local Space	PCI9030 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0	0x18	MEM	4 MByte (2 MByte*)	32		Battery Backup Memory
1	0x1C	MEM	64	8		Local Register

Table 3-1 : PCI9030 Local Space Configuration

* TPMC917-21R has only 2 MByte Battery Backup Memory

3.2 Local I/O Space

Not used by the TPMC917.

3.3 Local Memory Space

The complete SRAM of the TPMC917 is accessible in the memory space of the PMC module.

Address range: PCI Base Address 2 for Local Address Space 0 + (0x00000 to 0x3FFFFF)

PCI Base Address 2+	Description	Size (byte)	Comment
0x00000 to 0x3FFFFF	Battery backup memory	4M	TPMC917-10R/20R
0x00000 to 0x1FFFFF		2M	TPMC917-21R

Table 3-2 : SRAM Memory Map

All local registers of the TPMC917 are accessible in the memory space of the PMC module.

Address range: PCI Base Address 3 for Local Address Space 1 + (0x00 to 0x21)

PCI Base Address 3+	Description	Size (byte)	Comment
0x00 to 0x07	UART controller channel 0	8	TPMC917-10R only
0x08 to 0x0F	UART controller channel 1	8	
0x10 to 0x17	UART controller channel 2	8	
0x18 to 0x1F	UART controller channel 3	8	
0x20	FIFO Ready Register CH0-CH3	1	
0x21	Interrupt Status Register	1	-

Table 3-3 : Local Register Memory Map

3.3.1 Register Set of each UART channel (TPMC917-10R only)

Each of the four serial channels of the TPMC917-10R is accessed in the PCI memory space by two sets of registers. Both register sets have a common register, the Line Control Register (LCR). Bit 7 of the LCR is used to switch between the two register sets of a channel.

Register Set 1 is only accessible if bit 7 of the LCR (PCI Base Address 3 + Channel Offset + 0x03) is set to '0'. After reset Register Set 1 is accessible.

PCI Base Address + Channel Offset +	Read Mode	Write Mode	Size (bit)
0x00	Receive Holding Register	Transmit Holding Register	8
0x01	Interrupt Enable Register	Interrupt Enable Register	8
0x02	Interrupt Status Register	FIFO Control Register	8
0x03	Line Control Register	Line Control Register	8
0x04	Modem Control Register	Modem Control Register	8
0x05	Line Status Register (LCR)	-	8
0x06	Modem Status Register	-	8
0x07	Scratchpad Register	Scratchpad Register	8

Table 3-4 : Register Set 1

To get access to Register Set 2 of the serial channels bit 7 of the LCR must be set to '1'. The Enhanced Feature Registers, Xon-1/2 and Xoff-1/2 registers are only accessible if the LCR is set to '0xBF'.

PCI Base Address + Channel Offset +	READ/WRITE	Size (bit)	Comment
0x00	LSB of Divisor Latch	8	LCR bit 7 set to '1'
0x01	MSB of Divisor Latch	8	LCR bit 7 set to '1'
0x02	Enhanced Feature Register	8	LCR is set to '0xBF'
0x03	Line Control Register (LCR)	8	Always accessible
0x04	Xon-1 Word	8	LCR is set to '0xBF'
0x05	Xon-2 Word	8	LCR is set to '0xBF'
0x06	Xoff-1 Word	8	LCR is set to '0xBF'
0x07	Xoff-2 Word	8	LCR is set to '0xBF'

Table 3-5 : Register Set 2

The TPMC917-20R/21R has no UARTs. Write access to these registers of a TPMC917-20R/2R has no effect. Reading these registers of a TPMC917-20R/21R returns random data.

3.3.2 Special Registers

The TMPC917 provides two special registers. For fast status detection there is a FIFO Status Register for channel 0 to channel 3, and an Interrupt Status Register for all four channels and the battery interrupts.

For TPMC917-20R/21R, only the battery interrupt bits of the Interrupt Status Register carry valid data.

Offset to PCI Base Address 3	Register Name	Size (bit)
0x20	FIFO Ready Register CH0-CH3	8
0x21	Interrupt Status Register	8

Table 3-6 : Special Register

3.3.2.1 FIFO Ready Register Channel 0-3 (TPMC917-10R only)

The FIFO Ready Register FIFORDY1 is a byte wide read only register. The FIFO Ready Register provides the status of the transmit and the receive FIFOs of channel 0 to channel 3. Each TX and RX channel (0-3) has its own 64Byte FIFO. If any of the TX/RX FIFOs become empty/full, the status bit associated with the TX/RX function of channel 0-3 is set in the FIFO Ready Register.

For TPMC917-20R/21R, this register carries random data.

Bit	Symbol	Description	Access	Reset Value
7	RXRDY Channel 3	RX Ready Bit for channel 0-3 1 = the receiver is ready and is below the programmed trigger level 0 = the corresponding receive FIFO is above the programmed trigger level or a time-out has occurred	R	
6	RXRDY Channel 2			
5	RXRDY Channel 1			
4	RXRDY Channel 0			
3	TXRDY Channel 3	TX Ready Bit for channel 0-3 1 = one or more empty locations exist in the corresponding FIFO 0 = the corresponding transmit FIFO is full. This channel will not accept any more transmit data.	R	
2	TXRDY Channel 2			
1	TXRDY Channel 1			
0	TXRDY Channel 0			

Table 3-7 : FIFO Ready Register Channel 0-3

3.3.2.2 Interrupt Status Register

The Interrupt Status Register is a byte-wide read / write register located in the PCI Memory Space (PCI Base Address 3 + 0x21) and is useful for fast interrupt source detection.

It reflects the interrupt status of the four UART channels and the two Battery Status Interrupts.

The battery interrupts can be enabled and disabled.

Bit	Symbol	Description	Access	Reset Value
7	Enable Battery INT	Enable the Battery Monitor Interrupt 00 = Interrupt from battery monitor is disabled. Any other value enables the Battery Monitor Interrupt. After reset both battery interrupts are disabled. Both battery monitor devices generate interrupts on the local interrupt 2 of the PCI target chip if the monitored battery voltage (on board Lithium Cell or external battery) is lower than the specified battery fault voltage.	R/W	0
6				0
5	INT Status Bat2	Interrupt Status Battery 1/2 1 = indicates interrupt is pending on corresponding battery monitor (TPMC917-21R: only “INT Status BAT 1” carries valid data)	R	0
4	INT Status Bat1			0
3	Interrupt Channel 3	Interrupt Status of Channel 0-3 1 = indicates interrupt is pending on channel 0-3 0 = no interrupt on channel 0-3 Each of the four serial channels generates interrupts on the local interrupt 1 of the PCI target chip. If the “PCI Interrupt Enable” of the PCI target chip is disabled (Interrupt Control/Status Register bit 6 is set to ‘0’). This register can be used as a polling register for interrupts of the four serial controllers. Interrupts from the four serial channels can be individual enabled by the ST16C654 serial controller. After reset all UART interrupts are disabled. For TPMC917-20R/21R, these bits carry random data.	R	0
2	Interrupt Channel 2			
1	Interrupt Channel 1			
0	Interrupt Channel 0			

Table 3-8 : Interrupt Status Register (Address 0x21)

4 PCI9030 Target Chip

4.1 PCI Configuration Registers (PCR)

4.1.1 PCI9030 Header TPMC917-10R

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	0395 1498
0x04	Status		Command		Y	0280 0000
0x08	Class Code			Revision ID	N	088000 0A
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	00 00 00 00
0x10	PCI Base Address 0 for MEM Mapped Config. Registers				Y	FFFFFFE0
0x14	PCI Base Address 1 for I/O Mapped Config. Registers				Y	00000000
0x18	PCI Base Address 2 for Local Address Space 0				Y	FFC00000
0x1C	PCI Base Address 3 for Local Address Space 1				Y	s.b.
0x20	PCI Base Address 4 for Local Address Space 2				Y	00000000
0x24	PCI Base Address 5 for Local Address Space 3				Y	00000000
0x28	PCI CardBus Information Structure Pointer				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	s.b. 1498
0x30	PCI Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved			New Cap. Ptr.	N	000000 40
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00
0x40	PM Cap.		PM Nxt Cap.	PM Cap. ID	N	4801 48 01
0x44	PM Data	PM CSR EXT	PM CSR		Y	00 00 0000
0x48	Reserved	HS CSR	HS Nxt Cap.	HS Cap. ID	Y[23:16]	00 00 00 06
0x4C	VPD Address		VPD Nxt Cap.	VPD Cap. ID	Y[31:16]	0000 00 03
0x50	VPD Data				Y	00000000

Table 4-1 : PCI9030 Header

PCI Base Address 3 for Local Address Space 1:

0xFFFFFFC0 = TPMC917-10R/20R

0xFFFFFFE0 = TPMC917-21R

Subsystem-ID:

0x000A = TPMC917-10R

0x0014 = TPMC917-20R

0x0015 = TPMC917-21R

4.1.2 PCI Base Address Initialization

PCI Base Address Initialization is scope of the PCI host software.

PCI9030 PCI Base Address Initialization:

1. Write 0xFFFF_FFFF to the PCI9030 PCI Base Address Register.
2. Read back the PCI9030 PCI Base Address Register.
3. For PCI Base Address Registers 0:5, check bit 0 for PCI Address Space.

   Bit 0 = '0' requires PCI Memory Space mapping

   Bit 0 = '1' requires PCI I/O Space mapping

   For the PCI Expansion ROM Base Address Register, check bit 0 for usage.

   Bit 0 = '0': Expansion ROM not used

   Bit 0 = '1': Expansion ROM used
4. For PCI I/O Space mapping, starting at bit location 2, the first bit set determines the size of the required PCI I/O Space size.

   For PCI Memory Space mapping, starting at bit location 4, the first bit set to '1' determines the size of the required PCI Memory Space size.

   For PCI Expansion ROM mapping, starting at bit location 11, the first bit set to '1' determines the required PCI Expansion ROM size.

   For example, if bit 5 of a PCI Base Address Register is detected as the first bit set to '1', the PCI9030 is requesting a 32 byte space (address bits 4:0 are not part of base address decoding).
5. Determine the base address and write the base address to the PCI9030 PCI Base Address Register. For PCI Memory Space mapping the mapped address region must comply with the definition of bits 3:1 of the PCI9030 PCI Base Address Register.

After programming the PCI9030 PCI Base Address Registers, the software must enable the PCI9030 for PCI I/O and/or PCI Memory Space access in the PCI9030 PCI Command Register (Offset 0x04). To enable PCI I/O Space access to the PCI9030, set bit 0 to '1'. To enable PCI Memory Space access to the PCI9030, set bit 1 to '1'.

Offset in Config.	Description	Usage
0x10	PCI9030 LCR's MEM	Used
0x14	PCI9030 LCR's I/O	Not used
0x18	PCI9030 Local Space 0	Used
0x1C	PCI9030 Local Space 1	Used
0x30	Expansion ROM	Not used

Table 4-2 : PCI9030 PCI Base Address Usage

4.2 Local Configuration Register (LCR)

After reset, the PCI9030 Local Configuration Registers are loaded from the on board serial configuration EEPROM.

The PCI base address for the PCI9030 Local Configuration Registers is PCI9030 PCI Base Address 0 (PCI Memory Space) (Offset 0x10 in the PCI9030 PCI Configuration Register Space) or PCI9030 PCI Base Address 1 (PCI I/O Space) (Offset 0x14 in the PCI9030 PCI Configuration Register Space).

Do not change hardware dependent bit settings in the PCI9030 Local Configuration Registers.

Offset from PCI Base Address	Register	Value	Description
0x00	Local Address Space 0 Range	s.b.	4 MB / 2 MB Local memory space
0x04	Local Address Space 1 Range	0x0FFF_FC00	Local register space
0x08	Local Address Space 2 Range	0x0000_0000	Not used
0x0C	Local Address Space 3 Range	0x0000_0000	Not used
0x10	Local Exp. ROM Range	0x0000_0000	Not used
0x14	Local Re-map Register Space 0	0x0000_0001	Address offset for memory
0x18	Local Re-map Register Space 1	0x0040_0001	Address offset for registers
0x1C	Local Re-map Register Space 2	0x0000_0000	Not used
0x20	Local Re-map Register Space 3	0x0000_0000	Not used
0x24	Local Re-map Register ROM	0x0000_0000	Not used
0x28	Local Address Space 0 Descriptor	0x0082_0100	Local timing address space 0
0x2C	Local Address Space 1 Descriptor	0x5401_A0E0	Local timing address space 1
0x30	Local Address Space 2 Descriptor	0x0000_0000	Not used
0x34	Local Address Space 3 Descriptor	0x0000_0000	Not used
0x38	Local Exp. ROM Descriptor	0x0000_0000	Not used
0x3C	Chip Select 0 Base Address	0x0010_0001	Chip select lower 2 MB memory bank
0x40	Chip Select 1 Base Address	0x0030_0001	Chip select upper 2 MB memory bank
0x44	Chip Select 2 Base Address	0x0040_0011	UART registers
0x48	Chip Select 3 Base Address	0x0040_0023	Special registers
0x4C	Interrupt Control/Status	s.b.	Interrupt configuration
0x4E	EEPROM Write Protect Boundary	0x0000_0000	No write protection
0x50	Miscellaneous Control Register	0x807C_5000	Retry delay = maximum
0x54	General Purpose I/O Control	0x0249_06D3	GP4 is input, all others are outputs
0x70	Hidden1 Power Management data select	0x0000_0000	Not used
0x74	Hidden 2 Power Management data scale	0x0000_0000	Not used

Table 4-3 : PCI9030 Local Configuration Register for TPMC917-10R

Interrupt Control/Status: 0x0000_005B = TPMC917-10R

0x0000_005A = TPMC917-20R/21R

Local Address Space 0 Range: 0xFFFFFFC0 = TPMC917-10R/20R

0xFFFFFFE0 = TPMC917-21R

4.3 Configuration EEPROM

After power-on or PCI reset, the PCI9030 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Address 0x00 to 0x27 : PCI9030 PCI Configuration Register Values
- Address 0x28 to 0x87 : PCI9030 Local Configuration Register Values

See the PCI9030 Manual for more information.

Address	Offset							
	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x0395	0x1498	0x0281	0x0000	0x0880	0x000A	s.b.	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x0006	0x0000	0x0003	s.b.	0x0000	0x0FFF	0xFFC0
0x30	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0001
0x40	0x0040	0x0001	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000
0x50	0x4082	0x0100	0x5401	0xA0E0	0x0000	0x0000	0x0000	0x0000
0x60	0x0000	0x0000	0x0010	0x0001	0x0030	0x0001	0x0040	0x0011
0x70	0x0040	0x0023	0x0000	s.b.	0x807C	0x5000	0x0249	0x06D3
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Table 4-4 : Configuration EEPROM TPMC917-10R

TPMC917-10R: 0x0C = 0x000A, 0x76 = 0x005B 0x28 = 0x0FC0

TPMC917-20R: 0x0C = 0x0014, 0x76 = 0x005A 0x28 = 0x0FC0

TPMC917-21R: 0x0C = 0x0015, 0x76 = 0x005A 0x28 = 0x0FE0

4.4 Local Software Reset

The PCI9030 Local Reset Output LRESETo# is used to reset the on board local logic.

The PCI9030 local reset is active during PCI reset or if the PCI Adapter Software Reset bit is set in the PCI9030 local configuration register CNTRL (offset 0x50).

CNTRL[30] PCI Adapter Software Reset:

Value of '1' resets the PCI9030 and issues a reset to the Local Bus (LRESETo# asserted). The PCI9030 remains in this reset condition until the PCI Host clears this bit. The contents of the PCI9030 PCI and Local Configuration Registers are not reset. The PCI9030 PCI Interface is not reset.

5 Configuration Hints

5.1 PCI Interrupt Control/Status

The UART and battery status generate interrupts on pin INTA# of the PCI bus. The interrupt status can be read at the Interrupt Status Register INTCSR of the PCI Controller PCI9030.

Bit	Description	Access	Reset Value
31:8	Not used	R	0
7	Software Interrupt	R/W	0
6	PCI Interrupt Enable	R/W	1
5	Battery Interrupt Status	R	0
4	Local Interrupt 2 Polarity	R/W	1
3	Local Interrupt 2 Enable	R/W	1
2	UART Interrupt Status	R	0
1	Local Interrupt 1 Polarity	R/W	1
0	Local Interrupt 1 Enable	R/W	1 (TPMC917-10R) 0 (TPMC917-20R/21R)

Table 5-1 : Interrupt Control/Status Register (INTCSR, 0x4C)

The local interrupt 1 reflects the four channel UART interrupts (TPMC917-10R only). Bit 2 will be set if bit 1 is set and an interrupt is generated on one or more UART channels. For more information see chapter “Interrupt Status Register”.

The local interrupt 2 reflects the status of the backup battery supply voltage (either on board Lithium Cell or external battery via P14 mezzanine connector). This register will be initialized from the on board EEPROM after power-on the TPMC917 with the above shown initial values.

5.2 Big / Little Endian

- PCI – Bus (Little Endian)

Byte 0	AD[7..0]
Byte 1	AD[15..8]
Byte 2	AD[23..16]
Byte 3	AD[31..24]

- Every Local Address Space (0...3) and the Expansion ROM Space can be programmed to operate in Big or Little Endian Mode.

Big Endian		**Little Endian**	
32 Bit		**32 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
Byte 2	D[15..8]	Byte 2	D[23..16]
Byte 3	D[7..0]	Byte 3	D[31..24]
16 Bit upper lane		**16 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
Byte 1	D[23..16]	Byte 1	D[15..8]
16 Bit lower lane			
Byte 0	D[15..8]		
Byte 1	D[7..0]		
8 Bit upper lane		**8 Bit**	
Byte 0	D[31..24]	Byte 0	D[7..0]
8 Bit lower lane			
Byte 0	D[7..0]		

Table 5-2 : Local Bus Little/Big Endian

Standard use of the TPMC917:

Local Address Space 0	32 bit bus in Little Endian Mode
Local Address Space 1	8 bit bus in Little Endian Mode
Local Address Space 2	not used
Local Address Space 3	not used
Expansion ROM Space	not used

To change the Endian Mode use the Local Configuration Registers for the corresponding Space. Bit 24 of the according register sets the mode. A value of 1 indicates Big Endian and a value of 0 indicates Little Endian.

Use the PCI Base Address 0 + Offset or PCI Base Address 1 + Offset:

Short cut	Offset	Name
LAS0BRD	0x28	Local Address Space 0 Bus Region Description Register
LAS1BRD	0x2C	Local Address Space 0 Bus Region Description Register
LAS2BRD	0x30	Local Address Space 0 Bus Region Description Register
LAS3BRD	0x34	Local Address Space 0 Bus Region Description Register
EROMBRD	0x38	Expansion ROM Bus Region Description Register

You could also use the PCI - Base Address 1 I/O Mapped Configuration Registers.

5.3 Baud Rate Programming Formula

Each serial isolated channels of the TPMC917 contains a programmable baud rate generator. The clock of the ST16C654 can divided by any divisor from 1 to $2^{16} - 1$. The divisor can be programmed by the LSB and the MSB of the Divisor Latch Register. After reset the MCR bit 7 of each channel is default '0' and the value of LSB and MSB is 0xFFFF.

The basic formula of baud rate programming is:

$$\frac{7.3728MHz}{16 * DIVISOR * (1 + 3 * MCR\_BIT7)}$$

Baud Rate MCR bit 7=0	Baud Rate MCR bit 7=1	Divisor (DLM, DLL)
200	50	0x0900
300	75	0x0600
600	150	0x0300
1200	300	0x0180
2400	600	0x00C0
4800	1200	0x0060
9600	2400	0x0030
19.2K	4800	0x0018
28.8K	7200	0x0010
38.4K	9600	0x000C
76.8K	19.2K	0x0006
153.6K	38.4K	0x0003
230.4K	57.6K	0x0002
460.8K	115.2K	0x0001

Table 5-3 : Baud Rate Programming Table

Access to the DLM, DLL registers must be enabled in the LCR register.

These steps should be used to modify the DLM, DLL registers:

- **Write 0x80 to LCR register (enable access to DLM, DLL registers)**
- **Modify DLM, DLL registers**
- **Write normal operation byte value to LCR register**

The MCR (Modem Control Register) bits 5-7 must be enabled for modifying by setting EFR (Enhanced Feature Register) bit 4.

These steps should be used to modify MCR bit 7:

- **Write 0xBF to LCR register (enable access to EFR register)**
- **Set EFR register bit 4 to '1' (enable modification of MCR bits 5-7)**
- **Write 0x00 to LCR register (enable access to MCR register)**
- **Modify MCR bit 7**
- **Write 0xBF to LCR register (enable access to EFR register)**
- **Set EFR register bit 4 to '0' (Latch MCR bit setting)**
- **Write normal operation byte value to LCR register**

6 Data Retention Time

The contents of the TPMC917 SRAM will only be retained during system power-down while the battery is able to supply sufficient current to maintain the SRAM cell array.

TEWS uses a CR2430 lithium button cell battery with a capacity of 285mAh. It produces a nominal 2.9 V output with a flat discharge curve until the end of its effective live, and thus is suitable for providing battery backup to low-power SRAMs.

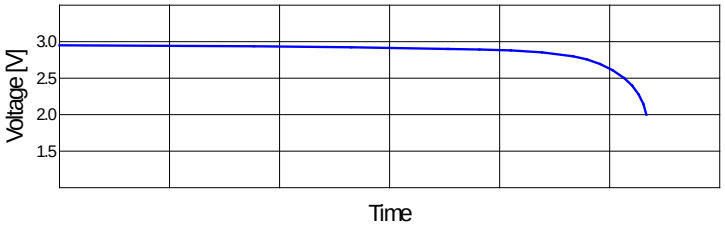

Figure 6-1 : Typical Lithium Battery Discharge Curve

The Battery will reach the end of its useful life, limiting the Data Retention Time, for one of two reasons:

- The effects of aging will have rendered the cell inoperative before the stored charge has been fully consumed by the SRAM. This is called Battery Lifetime.
- It becomes discharged by providing current to the SRAM in the battery backup mode. The time the battery can supply the SRAM is called Data Retention Time. It depends on Battery Capacity and SRAM Standby Current.

Whenever the TPMC917 is powered up, the SRAMs are supplied by system-power and no current is drawn from the battery. Only when the TPMC917 is powered down, the SRAM supply is switched from system-power to the on-board battery.

During Battery Backup, the SRAMs consume current from the Battery. With a typical backup current of 20µA and a fresh 285mAh battery, the resulting Data Retention Time would be:

$$T_{DataRetention} = 285mAh / 20\mu A = 14250 \text{ hours (app. 1.7 years)}$$

The currently remaining Data Retention Time of a TPMC917 is a function of battery age, already consumed Data Retention Time and SRAM backup current. As temperature has a non-linear influence on SRAM backup current and battery self-discharge rate, the remaining Data Retention Time is not calculable.

During normal operation, the TPMC917 monitors the lithium cell capacity every 24 hours. If enabled, an interrupt is generated in case the battery voltage is too low. Battery status can also be monitored by polling the Interrupt Status Register.

A battery low status is signaled when the battery voltage is below app. 2.6V. Since the SRAM data is preserved for battery voltages down to 2.0V, there is still some Battery Backup lifetime left and it is not necessary to exchange the battery immediately. But it should be replaced in the near future.

7 Installation

7.1 Security Warning (Lithium Battery)

CAUTION! - This system contains a lithium battery.

Lithium batteries may explode if mishandled.

Please observe the following warnings strictly. If misused, the battery may explode or leak, causing injury or damage to the equipment.

- Keep batteries out of reach for children. In case of ingestion of a cell or battery, the person involved should seek medical assistance promptly.
- The batteries must be inserted into the equipment with correct polarity (+ and -).
- Do not use metallic or other conductive extraction tools to replace the batteries.
- Do not attempt to revive used batteries by heating, charging or other means.
- Do not dispose of batteries in fire. Do not dismantle batteries.
- Do not short circuit batteries.
- Do not expose batteries to high temperatures, moisture or direct sunlight.
- Do not place batteries on a conductive surface (anti-static work mat, packaging bag or form trays) as it can cause the battery to short.

CAUTION !

The battery may explode if it is incorrectly replaced.

Replace only with the same or equivalent type recommended by the manufacturer.

Dispose of used batteries according to the manufacturer's instructions.

7.2 Battery Backup Selection

The TPMC917 provides two possibilities for battery backup operation: Either the on board Lithium Cell or an external battery connected via the P14 I/O connector.

An original packed Lithium Cell is delivered together with the TPMC917. Insert the Lithium Cell with the plus pole “+” visible. A four position miniature DIP switch is used to select the source for battery backup. Factory configuration is switched S3, S4 in position “ON” and S1, S2 in position “OFF” to provide battery backup by the on board Lithium Cell.

Switching S3, S4 to the “OFF” position and S1, S2 to the “ON” position enables an external battery connected via the P14 I/O connector as battery backup source.

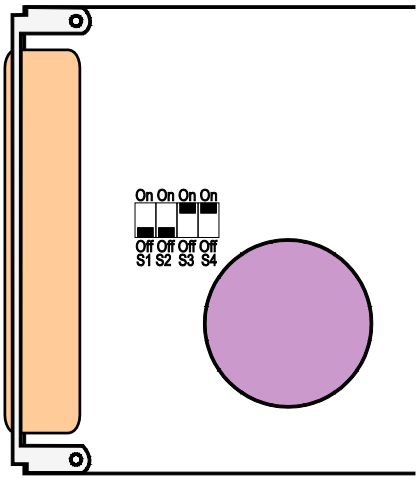

Figure 6-1 : DIP switch position

Following figures show the DIP switch configurations:

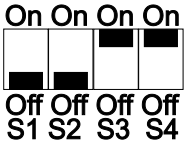

Figure 6-2 : DIP switch settings for Battery Backup by on board Lithium Cell

(factory configuration)

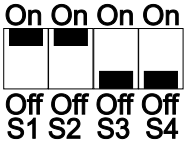

Figure 6-3 : DIP switch settings for battery backup via P14 I/O Connector

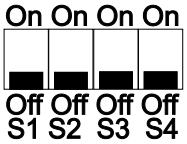

Figure 6-4 : DIP switch settings for battery backup disabled

Any other DIP switch settings are not allowed.

If the voltage of the backup battery is lower than the specified battery fault voltage, an interrupt will be issued to the PCI bus during normal operation (TPMC917 powered by standard 5V supply). In that case all memory data should be saved on another non-volatile memory medium, the TPMC917 should be switched off and the battery has to be changed.

To use the interrupt based battery monitor function of the TPMC917 the interrupts must be enabled in the Interrupt Control/Status Register (INTCSR) of the PCI target chip (default after EEPROM download). The battery interrupts must also be enabled in the Interrupt Status Register.

Insert the Lithium Cell with the plus pole "+" visible.

During battery operation no battery test will be executed to save battery power. It is recommended to power-up the module, at the latest after the specified data retention time, to check battery status.

The specified data retention depends on the ambient operating temperature. A higher ambient temperature as specified may lead to a significantly shorter data retention time.

8 Pin Assignment – I/O Connector

8.1 Mezzanine P14 I/O Connector

Pin	Signal	Function
1	Bat_Ext	External battery supply
2	NC	Not connected
3	Bat_Ext	External battery supply
4	NC	Not connected
5	Bat_Ext	External battery supply
6	NC	Not connected
7	GND	Board Ground
8	NC	Not connected
9	GND	Board Ground
10	NC	Not connected
11	GND	Board Ground
12…64	NC	Not connected

Table 7-1 : Mezzanine P14 I/O Connector

Figure 7-1 : P14 Pin Assignment

8.2 Front panel DB25 female Connector (TPMC917-10R only)

Pin	Signal	Function
1	TXA	Transmit Data UART A
2	RTSA#	Request to Send UART A
3	GND	Board Ground
4	TXB	Transmit Data UART B
5	RTSB#	Request to Send UART B
6	GND	Board Ground
7	TXC	Transmit Data UART C
8	RTSC#	Request to Send UART C
9	GND	Board Ground
10	TXD	Transmit Data UART D
11	RTSD#	Request to Send UART D
12	GND	Board Ground
13	NC	Not connected
14	RXA	Receive Data UART A
15	CTSA#	Clear to Send UART A
16	NC	Not connected
17	RXB	Receive Data UART B
18	CTSB#	Clear to Send UART B
19	NC	Not connected
20	RXC	Receive Data UART C
21	CTSC#	Clear to Send UART C
22	NC	Not connected
23	RXD	Receive Data UART D
24	CTSD#	Clear to Send UART D
25	NC	Not connected

Table 7-2 : Front panel DB25 female Connector (TPMC917-10R only)

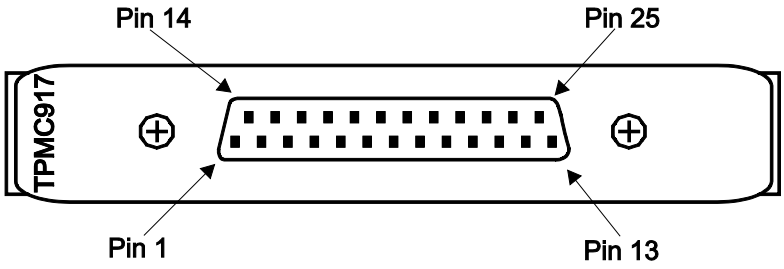

Figure 7-2 : DB25 Pin Assignment