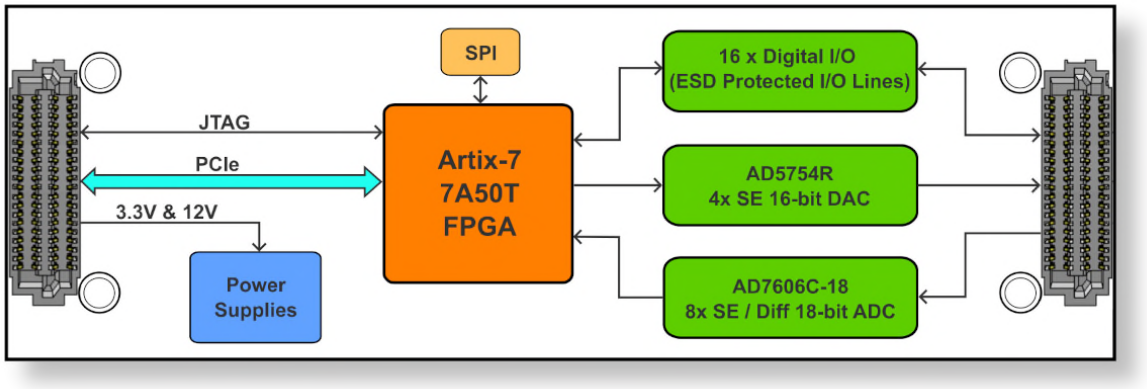
TQMC700 Reconfigurable FPGA with AD/DA & Digital I/O



TQMC700 Block Diagram

Application Information

The TQMC700 is a VITA 93.0 compatible single-width QMC offering a user programmable AMD Artix 7 7A50T FPGA.

The TQMC700 provides 16 ESD-protected 5V-tolerant TTL lines. All I/O lines are individually programmable as input or output. TTL I/O lines can be set to high, low, or tristate.

The 18 bit ADC offers 8 input channels, each of them has a sampling rate of up to 1 Msps. Each channel can be operated in bipolar single-ended, unipolar single-ended and bipolar differential mode. In the single-ended modes it offers software selectable input voltage ranges of 0-5 V, 0-10 V, 0-12.5 V, ±2.5 V, ±5 V, ±6.25 V, ±10 V and ±12.5V. In differential mode the input voltages are selectable between ±5 V, ±10 V, ±12.5 V and ±20 V. There is a flexible digital filter offering a oversampling ratio up to 256.

The DAC offers 4 channels of 16 bit analog outputs with software selectable output voltage ranges of 0-5 V, 0-10 V, 0-10.8 V, ±5 V, ±10 V or ±10.8 V. The output voltage range can be individually set per channel. The conversion time is typ. 10 µs and the DAC outputs are capable to drive a load of 2 kΩ, with a capacitance up to 4000 pF.

Each TQMC700 is factory calibrated. The correction data is stored in an on-board serial EEPROM unique to each TQMC700 module.

The User FPGA is configured by a SPI flash. An in-circuit debugging option is available via the QMC's JTAG interface for read back and real-time debugging of the FPGA design (using the Vivado ILA).

User applications for the TQMC700 with 7A50T FPGA can be developed using the design software Vivado Design Suite HL WebPACK Edition, which can be downloaded free of charge from www.xilinx.com.

TEWS offers a well-documented basic FPGA Example Application design. It includes a constraints file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TQMC700. It implements PCIe to register mapping and basic I/O. It comes as a Xilinx Vivado Design Suite project with source code and as a ready-to-download bit stream.

The TQMC700 is available as air cooled and conduction cooled variant.

Conduction Cooled QMC

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Technical Information

- Form Factor: Standard single QMC conforming to VITA 93.0
  - Board size: 78.25 mm x 26 mm
- PCI Express 2.0 compliant interface
- Artix-7 User programmable FPGA
  - Xilinx XC7A50T-2
  - PCIe endpoint in FPGA
- 128 Mbit SPI-EEPROM for FPGA configuration and User Data
- Digital I/O
  - 16 ESD-protected 5 V-tolerant TTL lines
  - Direction individually programmable
- 8 channels 18 bit analog input
  - Simultaneous sampling
  - differential or single-ended inputs
  - Programmable input voltage (one setting for all channels):
    0-5 V, 0-10 V, 0-12.5 V,
    ±2.5 V, ±5 V, ±6.25 V, ±10 V, ±12.5 V
  - Sampling rate: 1 Msps
  - Overvoltage protection
  - Factory calibration
- 4 channels single-ended 16 bit analog output
  - Simultaneous update
  - Programmable output voltage:
    0-5 V, 0-10 V, 0-10.8 V,
    ±5 V, ±10 V, ±10.8 V
  - Conversion time: typ.10 µs
  - Up to 2 kΩ resistive, 4000 pF capacitive load
  - Overcurrent protection
  - Factory calibration
- Operating temperature -40 °C to +85 °C

Order Information

RoHS Compliant

TQMC700-10R-A	16 TTL I/O, 8 AD, 4 DA, Artix-7 7A50T FPGA, air cooled
TQMC700-10R-H	16 TTL I/O, 8 AD, 4 DA, Artix-7 7A50T FPGA, conduction cooled

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Software

TDRV020-SW-25	Integrity Software Support
TDRV020-SW-42	VxWorks Software Support
TDRV020-SW-65	Windows Software Support
TDRV020-SW-82	Linux Software Support
TDRV020-SW-95	QNX Software Support

For other operating systems please contact TEWS.

Related Products

TPCE210	2 Site QMC Carrier, PCIe x4, Gen2, low-profile, VHDCI-68 I/O

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