The Embedded I/O Company

TEWS TECHNOLOGIES

TQMC400

4 Channel RS232/RS422/RS485 Programmable Serial Interface

Version 1.0

User Manual

Issue 1.0.0

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TQMC400-10R-A

4 Channel Full-Modem Programmable RS232/RS422/RS485, air cooled

TQMC400-10R-H

4 Channel Full-Modem Programmable RS232/RS422/RS485, conduction cooled

Document History

Issue	Description	Date
1.0.0	Initial Issue	February 2026

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1 Product Description

The TQMC400 is a VITA93.0 compatible Small Form Factor Mezzanine Card (QMC) offering 4 UART channels with multiprotocol transceivers. Each channel can be programmed to operate as an RS232, RS422/RS485 full-duplex or RS485 half-duplex interface.

Each RS232 channel supports RxD, TxD, RTS, CTS, DTR, DSR, CD, RI and GND. RS422 and RS485 full-duplex supports a four wire interface (RX+, RX-, TX+, TX-) plus ground (GND). RS485 half-duplex supports a two wire interface (DX+, DX-) plus ground (GND). On-chip switchable termination of 120 Ω is provided for the RS422/RS485 interfaces.

Selectable data rates are up to 1 Mbps for RS232 mode and 20 Mbps for RS422/RS485 half-duplex and full-duplex mode. Additionally a reduced slew rate mode with lower EMI provides data rates with max. 250 kbps for RS232 and max. 500 kbps for RS422/RS485.

Each channel has 256 byte transmit and receive FIFOs to significantly reduce the overhead required to provide data to and get data from the transmitters and receivers. The FIFO trigger levels are programmable. The UART offers readable FIFO levels.

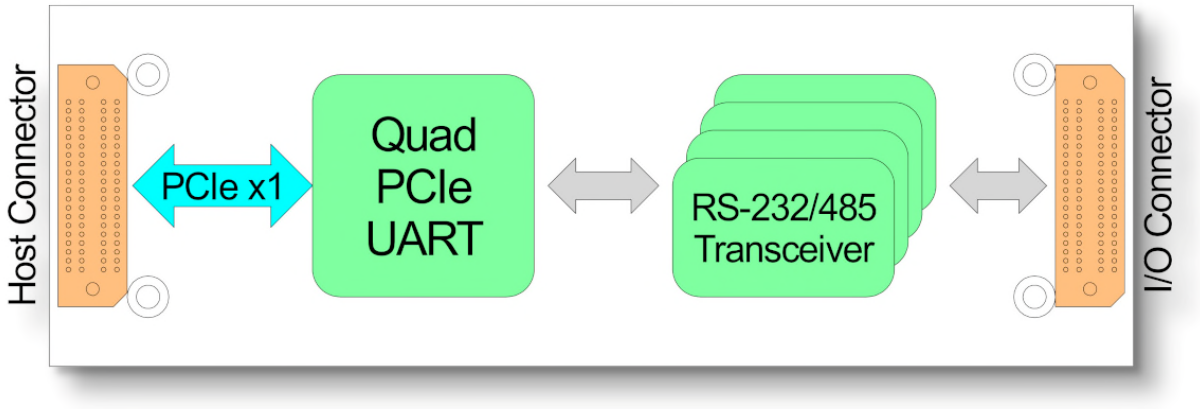

Figure 1-1 : Block Diagram

2 Technical Specification

General		
Mechanical Interface	Small Form Factor Mezzanine Card (QMC) air- or conduction-cooled conforming to VITA93.0 Standard Single-Width (26 mm x 78.25 mm)	
Electrical Interface	PCIe Revision 2.0 Gen1 x1	

Main On Board Devices	
PCIe Target Chip	XR17V354 (MaxLinear prev. Exar)
Multiprotocol Transceiver	THVD4431 (Texas Instruments)
IPMI Support	per serial EEPROM, as defined in VITA93.0

I/O Interface		
Interface Type	Asynchronous serial interface	
Number of Channels	4	
Physical Interface	Software selectable RS232, RS422, RS485 full-duplex, RS485 half-duplex	
Serial Channel I/O Signals	RS232 (full modem): RxD, TxD, RTS, CTS, DTR, DSR, CD, RI and GND RS422/RS485 full-duplex: Rx+, Rx-, Tx+, Tx-, GND RS485 half-duplex: Dx+/-, GND	
Termination	Software selectable 120 Ω	
Programmable Baud Rates	RS232 RS232 (reduced Slew Rate mode)	up to 1 Mbps max. 250 kbps
	RS422/RS485 RS422/RS485 (reduced Slew Rate mode)	up to 20 Mbps 500 kbps
ESD Protection	±16 kV - Human Body Model	

Physical Data		
Power Requirements	12V: not used 3.3V: Idle 60 mA typical RS232 100 mA typical RS422 250 mA typical RS485 390 mA typical	
Temperature Range	Operating -40 °C to +85 °C Storage -40 °C to +85 °C	
MTBF	1 530 0000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	TQMC400-10R-A	11 g
	TQMC400-10R-H	25 g

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This QMC module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with appropriate care!

3.2 Installing QMCs

QMCs are protected against mis- (or reverse-) insertion by a polarization feature incorporated in the connector. By virtue of the connector's size, this feature does not withstand brute force.

QMCs are easily installed by placing them aligned with the carrier's connectors and gently pressing them onto the carrier. There is a tactile snap when the QMC has taken seat on the carrier.

The QMC can now be screwed down as needed.

3.3 QMC Removal

When removing the QMC from the Carrier, care must also be taken to ensure that both plugs are disconnected simultaneously and in parallel. To do this, grasp both short sides of the PCB with both hands at the tabs and carefully lift the QMC.

- Remove the screws that secure the QMC on the carrier, if needed.
- Gently and simultaneously un-plug both connectors of the QMC.

Be aware that there is the potential for damaging the QMC Module or Carrier during QMC Module extraction. Applying an unequal force to the two connectors while unplugging can cause a misalignment, which then can potentially result in damaging the connectors or boards.

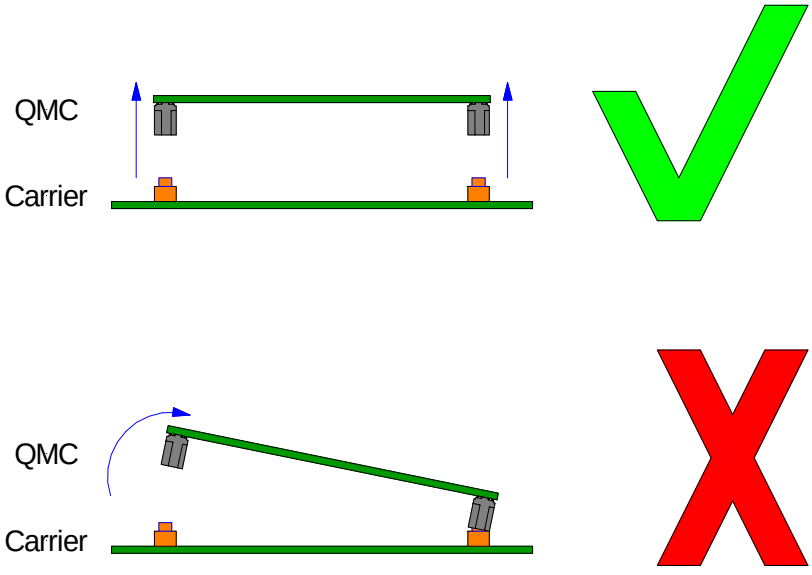

Figure 3-1 : QMC Removal

4 Terms and Definitions

4.1 Register Bit Access Types

Register Bit Access Type		Description
R	Read	The bit is readable by software (not writeable)
W	Write	The bit is writeable by software (not readable)
R/W	Read/Write	The bit is readable and writeable by software
R/C	Read/Clear	The bit is readable by software The bit is set by firmware Software may clear the bit by writing a '1'
R/S	Read/Set	The bit is readable by software Software may set this bit to '1' The bit is cleared by firmware

Table 4-1 : Register Bit Access Types

When reading reserved register bits, the read value is undefined.

For future software compatibility: For register write access, reserved bits shall be written '0'.

4.2 Signal Direction Types

Signal Direction Types as stated in Pin Assignment tables.

Signal Direction (Dir)	Description
I	TEWS card input Externally driven signal into the TEWS card
O	TEWS card output Signal driven out by TEWS card
I/O	Bi-Directional Signal
OD	TEWS card Open Drain output Signal driven low or tri-stated by TEWS card

Table 4-2 : Signal Direction Types

4.3 Style Conventions

Hexadecimal values are shown with prefix 0x (i.e. 0x029E).

Binary values are shown with prefix 0b (i.e. 0b0110).

"Active Low" signals are shown with a # suffix (i.e. RESET#).

5 Addressing

5.1 PCI Device Identification

	Offset	
Vendor ID	0x00	0x1498 (TEWS Technologies)
Device ID	0x02	0xC190 (TQMC400)
Revision ID	0x08	0x00
Class Code	0x09	0x070002 (Simple Communication Controller, Serial Controller, 16550-Compatible UART)
Subsystem Vendor ID	0x2C	0x1498 (TEWS Technologies)
Subsystem ID	0x2E	0xC00A (TQMC400-10R)

Table 5-1 : PCI Device Identification

5.2 XR17V354 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the XR17V354 local space.

XR17V354 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0 (0x10)	MEM	16k	32	BIG	Device Configuration Space

Table 5-2 : XR17V354 Local Space Configuration

5.3 Device Configuration Space

PCI Base Address: XR17V354 PCI Base Address 0 (Offset 0x10 in PCI Configuration Space).

The TQMC400 uses the XR17V354 Quad UART to provide and control the 4 channels.

Device Configuration Space Content	PCI Address	Size (Bit)
UART 0 Register Set	PCI Base Address 0 + (0x0000 to 0x03FF)	32
UART 1 Register Set	PCI Base Address 0 + (0x0400 to 0x07FF)	32
UART 2 Register Set	PCI Base Address 0 + (0x0800 to 0x0BFF)	32
UART 3 Register Set	PCI Base Address 0 + (0x0C00 to 0x0FFF)	32

Table 5-3 : Device Configuration Space

All registers can be accessed in 8, 16, 24 or 32 bit width with exception to one special case: When reading the receive data together with its LSR register content, the host must read them in 16 or 32 bits format in order to maintain integrity of the data byte with its associated error flags.

5.3.1 UART Register Sets

The Device Configuration Space provides a register set for each of the 4 UARTs.

UART Register Set	Register Set Offset
Serial Channel 0	0x0000
Serial Channel 1	0x0400
Serial Channel 2	0x0800
Serial Channel 3	0x0C00

Table 5-4 : UART Register Set Offset

Offset Address	Description	Access	Data Width
0x0000 – 0x000F	UART Channel Configuration Registers First 8 registers are 16550 compatible	R/W	8, 16, 24, 32
0x0010 – 0x007F	Reserved	-	-
0x0080 – 0x009A	Device Configuration Registers	R/W	8, 16, 24, 32
0x009B – 0x00FF	Reserved	-	-
0x0100 – 0x01FF	Read FIFO – 256 bytes of RX FIFO data	R	8, 16, 24, 32
	Write FIFO – 256 bytes of TX FIFO data	W	8, 16, 24, 32
0x0200 – 0x03FF	Read FIFO with errors – 256 bytes of RX FIFO data + LSR	R	16, 32

Table 5-5 : UART Register Set

5.3.2 Device Configuration Registers

The Device Configuration Registers control general operating conditions and monitor the status of various functions. This includes a 16 bit general purpose counter, multipurpose input/outputs (not supported by the TQMC400), sleep mode, soft-reset and device identification, and revision. They are embedded inside the UART register sets. Some registers are accessible from the Device Configuration Registers in all UART register sets, but control only the bit for that channel.

Address	Register	Description	Access	Reset Value
0x080	INT0 [7:0]	Channel Interrupt Indicator	R	0x00
0x081	INT1 [15:8]	Interrupt Source Details	R	0x00
0x082	INT2 [23:16]		R	0x00
0x083	INT3 [31:24]		R	0x00
0x084	TIMERCNTL	Timer Control Register	R/W	0x00
0x085	REGA	Reserved	-	0x00
0x086	TIMERLSB	Programmable Timer Value	R/W	0x00
0x087	TIMERMSB		R/W	0x00
0x088	8XMODE	8X Sampling Rate Enable	R/W	0x00
0x089	4XMODE	4X Sampling Rate Enable	R/W	0x00
0x08A	RESET	UART Reset	W	0x00
0x08B	SLEEP	UART Sleep Mode Enable	R/W	0x00
0x08C	DREV	Device Revision	R	Rev.
0x08D	DVID	Device Identification	R	0x88
0x08E	REGB	Simultaneous UART Write & EEPROM Interface	R/W	0x00
0x08F	MPIOINT	MPIO[7:0] Interrupt Mask	R/W	0x00
0x090	MPIOLVL	MPIO[7:0] Level Control	R/W	0x00
0x091	MPIO3T	MPIO[7:0] Output Pin Tri-state Control	R/W	0x00
0x092	MPIOINV	MPIO[7:0] Input Polarity Select	R/W	0x00
0x093	MPIOSEL	MPIO[7:0] Input/Output Select	R/W	0xFF
0x094	MPIOOD	MPIO[7:0] Open Drain Output Control	R/W	0x00
0x095	MPIOINT	MPIO[15:8] Interrupt Mask	R/W	0x00
0x096	MPIOLVL	MPIO[15:8] Level Control	R/W	0x00
0x097	MPIO3T	MPIO[15:8] Output Pin Tri-state Control	R/W	0x00
0x098	MPIOINV	MPIO[15:8] Input Polarity Select	R/W	0x00
0x099	MPIOSEL	MPIO[15:8] Input/Output Select	R/W	0xFF
0x09A	MPIOD	MPIO[15:8] Open Drain Output Control	R/W	0x00
0x09B	Reserved		-	0x00

Table 5-6 : Device Configuration Registers

For a detailed description of the Device Configuration Registers please refer to the XR17V354 data sheet which is available on the MaxLinear website (www.maxlinear.com/).

5.3.3 UART Channel Configuration Registers

Each UART channel has its own set of internal UART configuration registers for its own operation control and status reporting. The following table provides the register offsets within a register set, access types and access control:

Register Offset	Comment	Register	Access	Reset Value
16550 Compatible				
0x00	LCR[7] = 0	RHR – Receive Holding Register THR – Transmit Holding Register	R W	0xXX
	LCR[7] = 1	DLL – Baud Rate Generator Divisor Latch Low	R/W	0xXX
0x01	LCR[7] = 0	IER – Interrupt Enable Register	R/W	0x00
	LCR[7] = 1	DLM – Baud Rate Generator Divisor Latch High	R/W	0xXX
0x02	LCR[7] = 0	ISR – Interrupt Status Register FCR – FIFO Control Register	R W	0x01 0x00
	LCR[7] = 1	DLD – Divisor Fractional	R/W	0xXX
0x03		LCR – Line Control Register	R/W	0x00
0x04		MCR – Modem Control Register	R/W	0x00
0x05		LSR – Line Status Register Reserved	R W	0x60
0x06		MSR – Modem Status Register – Auto RS485 Delay (not supported by the TQMC400)	R W	0xX0
0x07	User Data	SPR – Scratch Pad Register	R/W	0xFF
Enhanced Registers				
0x08		FCTR – Feature Control Register	R/W	0x00
0x09		EFR – Enhanced Function Register	R/W	0x00
0x0A		TXCNT – Transmit FIFO Level Counter TXTRG – Transmit FIFO Trigger Level	R W	0x00
0x0B		RXCNT – Receiver FIFO Level Counter RXTRG – Receiver FIFO Trigger Level	R W	0x00
0x0C		Xchar – Xon, Xoff Received Flags Xoff-1 – Xoff Character 1	R W	0x00
0x0D		Reserved Xoff-2 – Xoff Character 2	R W	0x00
0x0E		Reserved Xon-1 – Xon Character 1	R W	0x00
0x0F		Reserved Xon-2 – Xon Character 2	R W	0x00

Table 5-7 : UART Channel Configuration Registers

The address for a UART Channel Configuration Register x in a UART Register Set for channel y is:

PCI Base Address 0 (PCI Base Address for the UART Register Space)

+ UART Register Set Offset for channel y

+ Register Offset for register x

Addressing example:

The address for the LCR register of UART channel 2 is:

PCI Base Address (PCI Base Address for the Device Configuration Space)

+ 0x0800 (Offset of the UART register set for serial channel 2)

+ 0x0003 (Offset of the LCR register within a UART register set)

For a detailed description of the serial channel registers please refer to the XR17V354 data sheet which is available on the MaxLinear website (www.maxlinear.com).

6 Configuration EEPROM

After power-on or PCI reset, the XR17V354 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Vendor ID
- Vendor Device ID
- Subsystem Vendor-ID
- Subsystem ID

See the XR17V354 Manual for more information.

Furthermore the EEPROM contains:

- The module version and revision
- The UART clock frequency in Hz
- The physical interface attached to the serial channels
- The maximal baud rate of the transceivers in bps
- The supported control signals of the serial channels

For the physical interfaces and the control signals applies: Bit 3 represents UART channel 3 and bit 0 represents UART channel 0. The appropriate bit is set to '1' for each UART channel attached to the physical interface represented by the word. Bit 15 to bit 4 are always '0'.

Address	Configuration Register	TQMC400
0x00	Address Word	0x0000
0x01	Vendor ID	0x1498
0x02	Adress Word	0x8001
0x03	Device ID	0xC190
0x04	Address Word	0x8004
0x05	Subsystem Vendor-ID	0x1498
0x06	Address Word	0x4005
0x07	Subsystem ID	0xC00A
0x08	Module Version	Reflects Module Version (i.e. V1.0)
0x09	Module Revision	Reflects Module Revision (i.e. Rev.A)
0x0A	EEPROM Revision	0x0005
0x0B	Oscillator Frequency (high)	0x0773
0x0C	Oscillator Frequency (low)	0x5940
0x0D	Reserved	-
0x0E	Reserved	-
0x0F	Controller Type	0x0002
0x10	RS232 Channels	0x000F
0x11	RS422 Channels	0x000F

Address	Configuration Register	TQMC400
0x12	TTL Channels	0x0000
0x13	RS485 Full Duplex Channels	0x000F
0x14	RS485 Half Duplex Channels	0x000F
0x15-0x1E	Reserved	-
0x1F	Programmable Interfaces	0x000F
0x20	Max Data Rate RS232 (high)	0x000F
0x21	Max Data Rate RS232 (low)	0x4240
0x22	Max Data Rate RS422 (high)	0x0131
0x23	Max Data Rate RS422 (low)	0x2D00
0x24	Max Data Rate TTL (high)	0x0000
0x25	Max Data Rate TTL (low)	0x0000
0x26	Max Data Rate RS485 Full Duplex (high)	0x0131
0x27	Max Data Rate RS485 Full Duplex (low)	0x2D00
0x28	Max Data Rate RS485 Half Duplex (high)	0x0131
0x29	Max Data Rate RS485 Half Duplex (low)	0x2D00
0x2A-0x2F	Reserved	-
0x30	RxD & TxD	0x000F
0x31	RTS & CTS	0x0000
0x32	Full modem	0x0000
0x33-0x37	Reserved	-
0x38	Enhanced RTS & CTS	0x0000
0x39	Enhanced Full Modem	0x0000
0x3A	Channels with enhanced RTS & CTS Support for RS232 only	0x000F
0x3B	Channels with RxD support only	0x0000
0x3C	Channels with enhanced Full-Modem Support for RS232 only	0x000F
0x3D-0x3F	Reserved	-

Table 6-1 : Configuration EEPROM

7 Configuration Hints

The TQMC400's physical interfaces of the serial channels are individually software programmable to various interface configurations. For this purpose a logical device chain simulates control registers for each interface channel.

7.1 Serial Channel Setup

After power-up, all transceivers are in shutdown mode, and all transceivers are disabled. Therefore the serial interfaces must be properly set up before they can be used.

The interfaces can be programmed to following modes:

- RS232
- RS485/RS422 full-duplex (with optional termination)
- RS485 half-duplex (Master/Slave, with optional termination)

Each channel is individually addressable.

The channel setup is done by shifting the channel's setup data to the on-board logic using the UART's MPIO pins.

For successful channel configuration, the following steps have to be performed:

- Control Data compilation
- MPIO initialization
- Control data write operation

In the following each step is described in detail.

7.1.1 Control Data compilation

The control data compilation is identical for all channels.

Bit	Symbol	Description	Access	Reset Value
6	SLR	Transmitter Speed-Select. Select slew-rate limiting for all protocols. Slew-rate limits with a logic-level high. 0b0: Normal data rate limit (RS232: 1 Mbps; RS485/422: 20 Mbps) 0b1: Limited data rate (RS232: 250 kbps; RS485/422: 500 kbps)	W	0
5	MODE2	0b000 : RS232 loopback 0b010 : RS232 0b001 : RS485 half-duplex 0b011 : RS422/RS485 full-duplex 0b111 : RS485 loopback Others : reserved	W	0b000
4	MODE0			
3	MODE1			
2	TERM_TX	Transmitter Termination Enable Terminate transmit line with a 120 Ω termination resistor '0': Termination inactive '1': Termination active	W	0

Bit	Symbol	Description	Access	Reset Value
1	TERM_RX	Receiver Termination Enable Terminate receive line with a 120 Ω termination resistor ‘0’: Termination inactive ‘1’: Termination active	W	0
0	SHDN#	Active-Low Shutdown-Control. Drive SHDN high to shut down transmitters and charge pump. Typical current consumption is 10 µA in shutdown mode. ‘0’: Shutdown ‘1’: Normal Operation	W	0

Table 7-1 : Channel Control Data (CCD)

7.1.2 MPIO Initialization

The MPIO pins form a simple bus to transfer the configuration data to the transceiver. The following chart gives an overview about the MPIO pin assignment.

MPIO Pin	Direction	Function
MPIO[0]	Output	RCLK – Storage Clock
MPIO[1]	-	not used
MPIO[2]	Output	SRCLK – Serial Register Clock
MPIO[5:3]	Output	ADR[2:0] – Channel selection 0b000 : Channel 0 0b001 : Channel 1 0b010 : Channel 2 0b011 : Channel 3 Others : reserved
MPIO[6]	Output	DATA – Serial Output of CCD
MPIO[15:7]	-	not used

Table 7-2 : MPIO Pins

For MPIO initialization, the following UART registers are used:

Address Offset	Register	Description	Access	Reset Value
0x090	MPIOLVL	MPIO[7:0] Level Control	R/W	0x00
0x093	MPIOSEL	MPIO[7:0] Input/Output Select	R/W	0xFF

Table 7-3 : UART MPIO Control Registers

MPIOLVL has to be initialized with the default value of 0x00. Subsequent, MPIOSEL must be set to 0x82 to configure MPIO[6:2] and MPIO[0] pins as outputs. All other UART MPIO register have to be left at their default values.

7.1.3 Control Data Write Operation

To transfer the desired control data to a channel, writes with the following data have to be performed to the UART's MPIOLVL register:

Step	MPIOLVL Data							
	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
1	0	0	ADR			0	0	0
2	0	CCD[6]	ADR			0	0	0
3	0	CCD[6]	ADR			1	0	0
4	0	CCD[5]	ADR			0	0	0
5	0	CCD[5]	ADR			1	0	0
6	0	CCD[4]	ADR			0	0	0
7	0	CCD[4]	ADR			1	0	0
8	0	CCD[3]	ADR			0	0	0
9	0	CCD[3]	ADR			1	0	0
10	0	CCD[2]	ADR			0	0	0
11	0	CCD[2]	ADR			1	0	0
12	0	CCD[1]	ADR			0	0	0
13	0	CCD[1]	ADR			1	0	0
14	0	CCD[0]	ADR			0	0	0
15	0	CCD[0]	ADR			1	0	0
16	0	0	ADR			0	0	1
17	0	0	000			0	0	0

Table 7-4 : Control Data Write Sequence

7.2 Special Features

7.2.1 Slew Rate Limiting

The SLEW LIMIT (SLR) control is used to select the slew-rate limiting of the RS232 transmitters and the RS485/RS422 drivers. With SLR asserted, the RS232 transmitters and the RS485/RS422 driver are slew-rate limited to reduce EMI, resulting in a max data rate of 250 kbps for RS232 and 500 kbps for RS485/RS422. RS232 data rates up to 1 Mbps and RS485/RS422 data rates up to 20 Mbps are possible when SLR is unasserted. SLR can be changed during operation without interrupting data communications.

7.2.2 Low-Power Shutdown

The THVD4431 has a shutdown control input, SHDN#. When SHDN# is LOW, all transmitters are shut down and supply current is reduced to 10 µA typical. The charge-pump capacitors must be recharged when coming out of shutdown before resuming operation in either RS232 or RS485/RS422 mode.

7.2.3 Auto RS485 Direction Control

In RS485 half-duplex applications it is necessary to tristate the driver when it is not active. The XR17V354 provides a special function, the “Auto RS485 Operation” for this purpose. The UART’s RTS# signal is connected to the DIR pin of the transceiver. The UART asserts RTS# to enable the driver before it starts to send a character and deasserts the RTS# signal after a programmable delay after the stop bit of the last transmitted character. The delay optimizes the time needed for the last transmission to reach the farthest station on a long cable network before switching off the line driver.

In RS485 full-duplex mode DIR always enables the transmitter while the receiver enable is connected to GND. (both are active simultaneously)

In RS232 mode the DIR Pin of the THVD4431 has no function.

The Auto RS485 Operation is enabled by FCTR bit 5. The delay is specified in MSR[7:4] (requires EFR[4] = 1).

7.2.4 RS485 Receiver Control

In RS485 half-duplex applications the driver and receiver are connected with each other. To prevent the echo of local data, the receive line can be inhibited for the time the driver is enabled. This is done by activating the “Auto RS485 Receiver Enable“ in the Channel Control Register.

When the Auto RS485 Receiver Enable is not activated in a half-duplex application, this will result in a kind of loopback mode. This may be done on purpose to monitor the loopback data for errors which would indicate a line contention. When the channel is unconnected, this may also be used as a build in self-test.

7.3 RS485/RS422 Configuration Examples

7.3.1 RS422 Multidrop

MODE2	MODE0	MODE1	TERM_TX	TERM_RX	FCTR[5]
OFF	ON	ON	OFF	ON*	OFF

* Terminate only if the device is a receiver and the end-point of the bus.

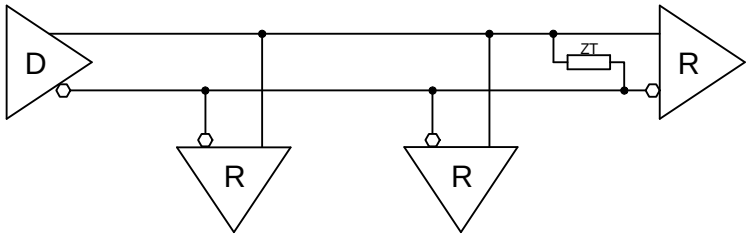

Figure 7-1 : RS422 Multidrop Configuration

7.3.2 RS422 Full Duplex Point to Point

MODE2	MODE0	MODE1	TERM_TX	TERM_RX	FCTR[5]
OFF	ON	ON	OFF	ON	OFF

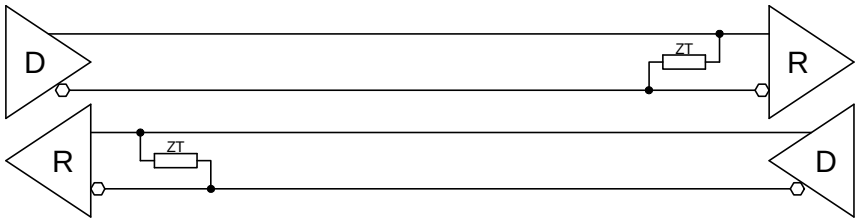

Figure 7-2 : RS422 Full Duplex Point to Point Configuration

7.3.3 RS485 Full Duplex Point to Point

MODE2	MODE0	MODE1	TERM_TX	TERM_RX	FCTR[5]
OFF	ON	ON	ON	ON	OFF

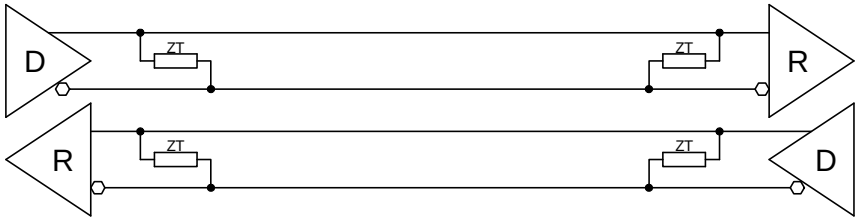

Figure 7-3 : RS485 Full Duplex Point to Point Configuration

7.3.4 RS485 Half Duplex Point to Point

MODE2	MODE0	MODE1	TERM_TX	TERM_RX	FCTR[5]
OFF	OFF	ON	OFF	ON	OFF

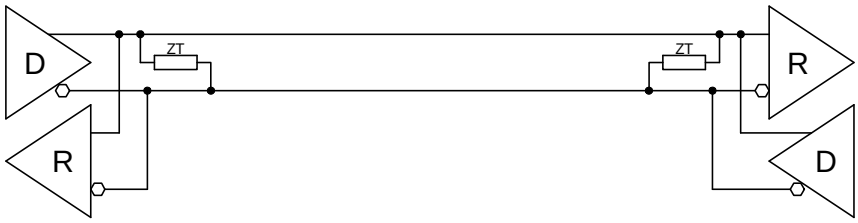

Figure 7-4 : RS485 Half Duplex Point to Point Configuration

7.3.5 RS485 Full Duplex Multi-point

Master

MODE2	MODE0	MODE1	TERM_TX	TERM_RX	FCTR[5]
OFF	ON	ON	ON	ON	OFF

Slave

MODE2	MODE0	MODE1	TERM_TX	TERM_RX	FCTR[5]
OFF	ON	ON	ON*	ON*	ON

* Terminate only if the device is the end-point of the bus.

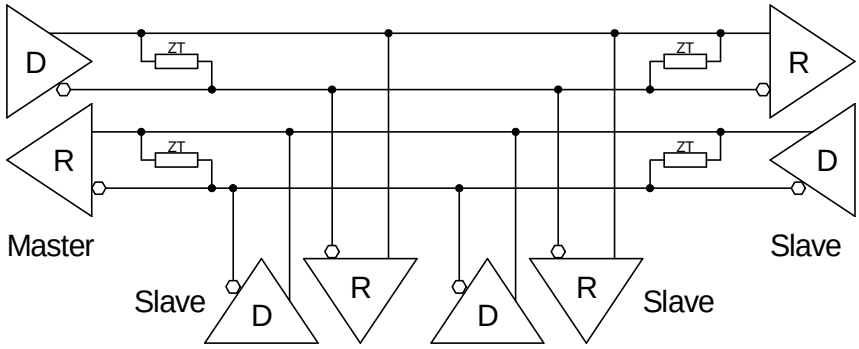

Figure 7-5 : RS485 Full Duplex Multi-Point Configuration

7.3.6 RS485 Half Duplex Multi-point

MODE2	MODE0	MODE1	TERM_TX	TERM_RX	FCTR[5]
OFF	OFF	ON	ON*	OFF	ON

* Terminate only if the device is the end-point of the bus.

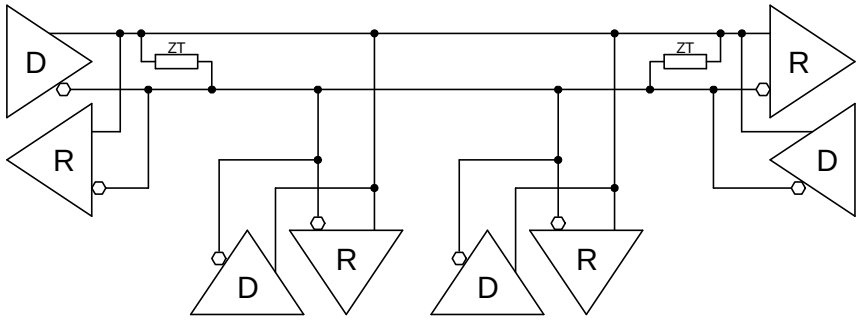

Figure 7-6 : RS485 Half Duplex Multi-Point Configuration

7.3.7 Channel Setup Summary

Each interface channel must be set up as described in section 7.1. Depending on the interface configuration the “Auto RS485 Operation” must be activated in the Feature Control Register in the XR17V354. Refer to the previous chapters “RS485/RS422 Configuration Examples” to find out which interface configurations suits your needs.

The following table shows how to program the interfaces to some commonly used modes:

Bit	Symbol	Reset Value	RS232 3T5R	RS422 Multidrop	RS422 FD	RS485 FD (Master)	RS485 FD Slave	RS485 HD
	Transceiver	**Channel Control Register**						
0	SHDN#	OFF	ON	ON	ON	ON	ON	ON
1	TERM_RX	OFF	OFF (1)	ON (2)	ON	ON	ON (2)	OFF
2	TERM_TX	OFF	OFF (1)	OFF	OFF	ON	ON (2)	ON (2)
3	MODE1	OFF	OFF	ON	ON	ON	ON	ON
4	MODE0	OFF	ON	ON	ON	ON	ON	OFF
5	MODE2	OFF	OFF	OFF	OFF	OFF	OFF	OFF
6	SLR	OFF	OFF	OFF	OFF	OFF	OFF	OFF
	XR17V354	**Feature Control Register (FCTR)**						
5	Auto RS485 Operation	OFF	OFF	OFF	OFF	OFF	ON	ON

(1) TERM_TX / TERM_RX settings are ignored in RS232 mode.
(2) Depends on bus configuration. Terminate only if the transceiver is the end-point of the bus.

Table 7-5 : Serial Channel Setup

7.4 I/O Electrical Interface

7.4.1 ESD Protection

The receiver inputs and transmitter outputs are characterized for ±16 kV ESD protection using the Human Body Model. Furthermore the device is protected against ±8 kV IEC 61000-4-2 contact, ±15 kV air-gap discharge and ±4 kV IEC 61000-4-4 fast transient burst.

7.4.2 Termination

In RS422 or RS485 mode, the receive and the transmit can be internally terminated with a 120 Ω termination resistor. The termination is software selectable.

7.4.3 Protection Features

The THVD4431 pins are protected against DC supply shorts in the range of ±16 V. In the RS485 mode, the short circuit current is limited to ±250 mA to comply the TIA/EIA-485A standard. In RS232 mode, current limiting of ±60 mA is applicable for scenarios where bus pins can short to ground.

The THVD4431 also features a thermal shutdown protection which will disable driver and receiver when juncture temperature exceeds a threshold of 150 °C minimum (170 °C typical).

Supply undervoltage protection is present on the transceiver supply.

For a detailed description of the protection features please refer to the THVD4431 data sheet available at the Texas Instruments Website. (www.ti.com)

7.4.4 RS485 Receiver Fail-Safe Operation

The RS485 differential receiver of the THVD4431 is failsafe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic high state so that the output of the receiver is not indeterminate.

8 Programming Hints

8.1 UART Baud Rate Programming

Each of the 4 UART channels of the TQMC400 provides a programmable Baud Rate Generator. The internal 125 MHz clock of the XR17V354 UART can be divided by any divisor from 1 to 2^{16} – 0.0625. The divisor can be programmed by the UART channel DLM (Divisor MSB), DLL (Divisor LSB) and DLD (Divisor Fractional) registers. After a reset, bit 7 of the UART channels MCR register defaults to '0' and the divisor value is 0xFFFF.

The sampling rate for a UART channel can be set to 8x (normal operation is 16x) in the 8XMODE register or 4x in the 4XMODE register. Transmit and receive data rates will double by selecting 8x sample rate or quadruple by selecting the 4x sample rate.

The basic formula of baud rate programming is:

$$\text{Baud Rate} = \frac{125MHz}{MODE \cdot Divisor \cdot (1 + 3 \cdot MCR[7])}$$

where MODE is 16 for 16XMODE, 8 for 8XMODE and 4 for 4XMODE.

Examples for standard baud rates are given in following chart (using 16XMODE sampling):

Baud Rate MCR[7] = 0	Baud Rate MCR[7] = 1	Divisor	DLM Value	DLL Value	DLD Value	Error (%)
9600	2400	813 12/16	0x03	0x2D	0xC	0.01
19.2k	4800	406 14/16	0x01	0x96	0xE	0.01
115.2k	28.8k	67 13/16	0x00	0x43	0xD	0.01
230.4k	57.6k	33 14/16	0x00	0x21	0xE	0.10
460.8k	115.2k	16 15/16	0x00	0x10	0xF	0.10
500k	125k	15 10/16	0x00	0x0F	0xA	0
750k	187.5	10 6/16	0x00	0x0A	0x6	0.40
921.6k	230.4k	8 7/16	0x00	0x08	0x7	0.47
1000k	250k	7 13/16	0x00	0x07	0xD	0
1250k	312.5k	6 4/16	0x00	0x06	0x4	0
1500k	375k	5 3/16	0x00	0x05	0x3	0.40

Table 8-1 : UART Baud Rate Programming

The achievable baud rate will not always exactly match the desired baud rate (see the "Error" column in the table above). A small error (up to 1%) will not affect the UART function.

To calculate a divisor value for a given baud rate, use following formula:

$$\text{Divisor} = \frac{125MHz}{MODE \cdot Baud\ Rate \cdot (1 + 3 \cdot MCR[7])}$$

where MODE is 16 for 16XMODE, 8 for 8XMODE and 4 for 4XMODE.

These steps should be used to modify the DLM, DLL and DLD registers of an UART channel:

1. Write 0x80 to the LCR register of the UART channel (enable access to the DLM, DLL and DLD registers).

2. Program the DLM, DLL and DLD registers of the UART channel.

3. Write normal operation byte value to the LCR register of the UART channel.

These steps should be used to modify MCR register bit 7 of an UART channel (set baud rate generator prescaler):

1. Set UART channel EFR register bit 4 to '1' (enable modification of MCR register bits 5-7).

2. Modify UART channel MCR register bit 7.

3. Set UART channel EFR register bit 4 to '0' (latch modified MCR register setting).

Note that the maximum baud rate for RS232 channel is 1 Mbps. Thus the minimum divisor value for RS232 channels is 0x0007D with MCR[7] = 0 and 16XMODE sampling.

9 I/O Interface Description

9.1 Overview

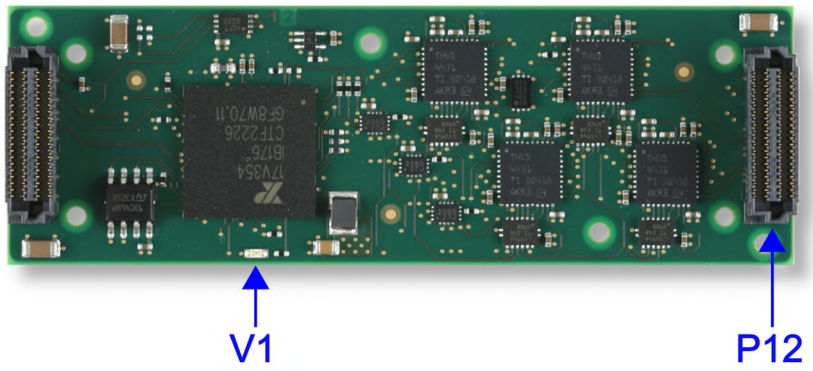

Figure 9-1 : Connector / LED Overview

9.2 LED Description

There is one status LED. It signals that board power supplies are operational.

LED	Color	State	Description
V1	Green	On	Power-Good indication for board power supplies

Table 9-1 : LED Description

9.3 I/O Connector P12

9.3.1 IOPIPE 1

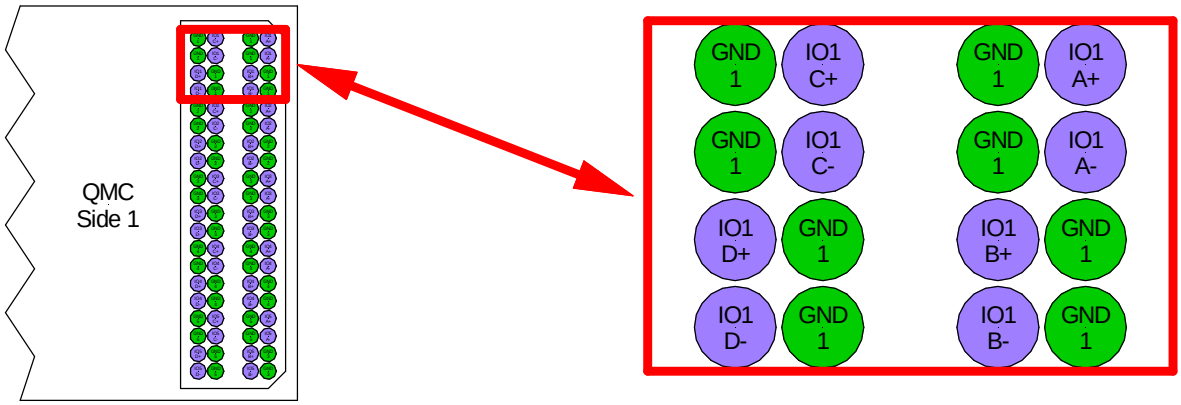

Figure 9-2 : P12 I/O Connector – IOPIPE 1

	Pin	RS232	Direction	RS485/422 Full-Duplex	Direction	RS485 Half-Duplex	Direction
IOPIPE 1	IO1A+	Rx0	In	TxD0+	Out	D0+	In/Out
	IO1A-	CTS0#	In	TxD0-	Out	D0-	In/Out
	IO1B+	Tx0	Out	RxD0+	In	-	-
	IO1B-	RTS0#	Out	RxD0-	In	-	-
	IO1C+	DSR0#	In	-	-	-	-
	IO1C-	DTR0#	Out	-	-	-	-
	IO1D+	CD0#	Out	-	-	-	-
	IO1D-	RI0#	Out	-	-	-	-
	GND1	System Ground					

Table 9-2 : P12 I/O Connector Pin Assignment – IOPIPE 1

9.3.2 IOPIPE 2

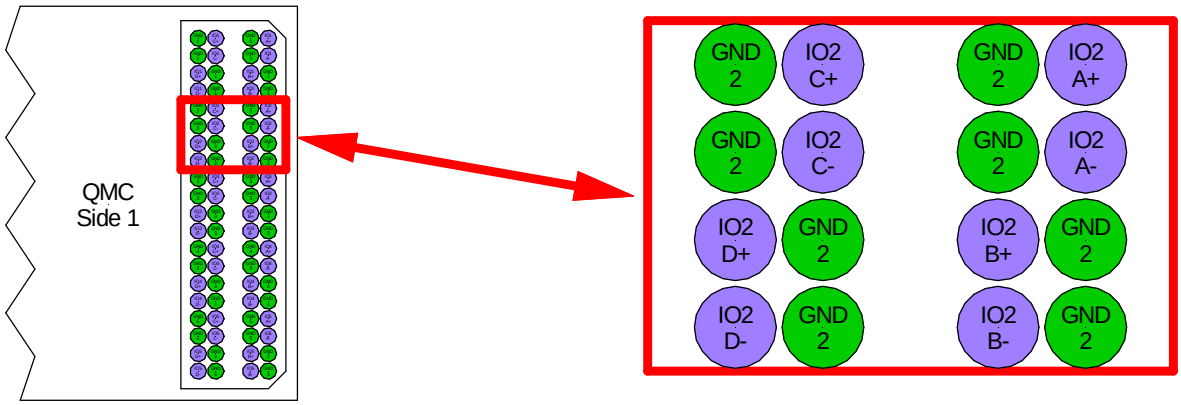

Figure 9-3 : P12 I/O Connector – IOPIPE 2

	Pin	RS232	Direction	RS485/422 Full-Duplex	Direction	RS485 Half-Duplex	Direction
IOPIPE 1	IO2A+	Rx1	In	TxD1+	Out	D1+	In/Out
	IO2A-	CTS1#	In	TxD1-	Out	D1-	In/Out
	IO2B+	Tx1	Out	RxD1+	In	-	-
	IO2B-	RTS1#	Out	RxD1-	In	-	-
	IO2C+	DSR1#	In	-	-	-	-
	IO2C-	DTR1#	Out	-	-	-	-
	IO2D+	CD1#	Out	-	-	-	-
	IO2D-	RI1#	Out	-	-	-	-
	GND2	System Ground					

Table 9-3 : P12 I/O Connector Pin Assignment – IOPIPE 2

9.3.3 IOPIPE 3

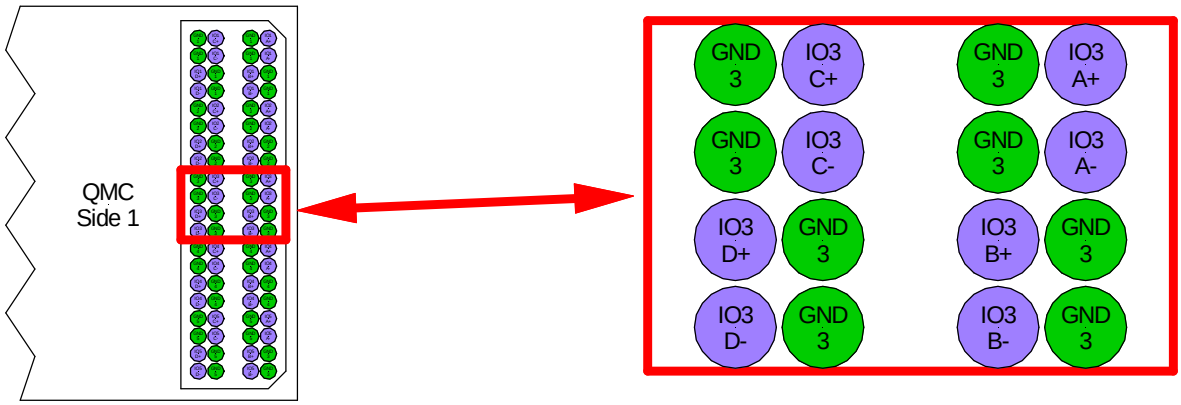

Figure 9-4 : P12 I/O Connector – IOPIPE 3

	Pin	RS232	Direction	RS485/422 Full-Duplex	Direction	RS485 Half-Duplex	Direction
IOPIPE 3	IO3A+	Rx2	In	TxD2+	Out	D2+	In/Out
	IO3A-	CTS2#	In	TxD2-	Out	D2-	In/Out
	IO3B+	Tx2	Out	RxD2+	In	-	-
	IO3B-	RTS2#	Out	RxD2-	In	-	-
	IO3C+	DSR2#	In	-	-	-	-
	IO3C-	DTR2#	Out	-	-	-	-
	IO3D+	CD2#	Out	-	-	-	-
	IO3D-	RI2#	Out	-	-	-	-
	GND3	System Ground					

Table 9-4 : P12 I/O Connector Pin Assignment – IOPIPE 3

9.3.4 IOPIPE 4

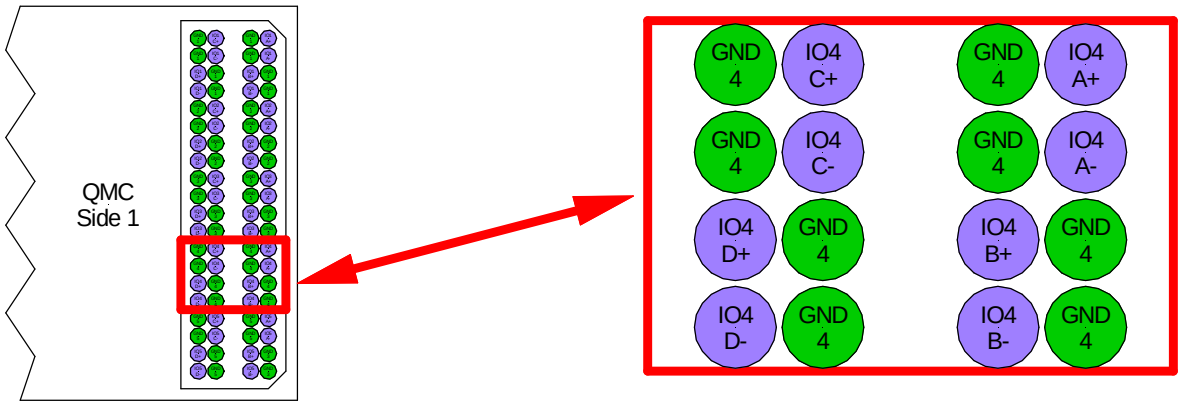

Figure 9-5 : P12 I/O Connector – IOPIPE 4

	Pin	RS232	Direction	RS485/422 Full-Duplex	Direction	RS485 Half-Duplex	Direction
IOPIPE 4	IO4A+	Rx3	In	TxD3+	Out	D3+	In/Out
	IO4A-	CTS3#	In	TxD3-	Out	D3-	In/Out
	IO4B+	Tx3	Out	RxD3+	In	-	-
	IO4B-	RTS3#	Out	RxD3-	In	-	-
	IO4C+	DSR3#	In	-	-	-	-
	IO4C-	DTR3#	Out	-	-	-	-
	IO4D+	CD3#	Out	-	-	-	-
	IO4D-	RI3#	Out	-	-	-	-
	GND4	System Ground					

Table 9-5 : P12 I/O Connector Pin Assignment – IOPIPE 4

9.3.5 IOPIPE 5

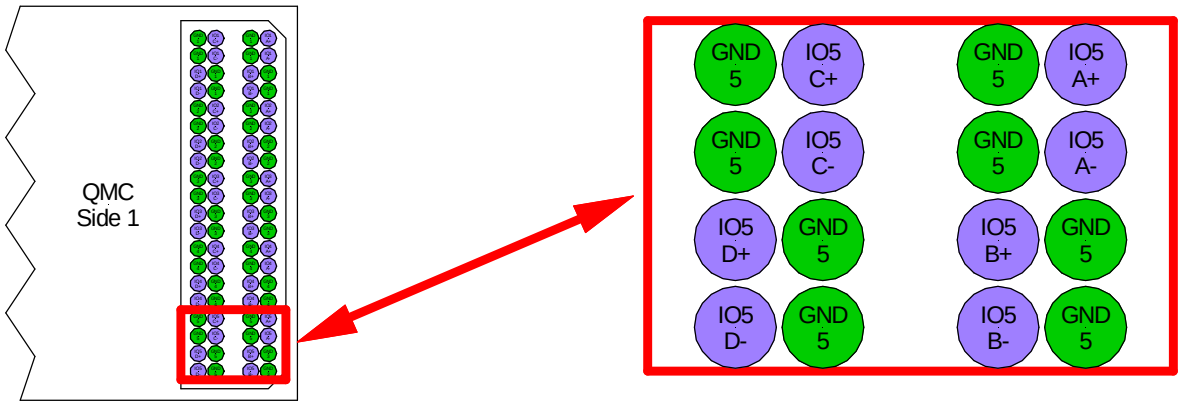

Figure 9-6 : P12 I/O Connector – IOPIPE 5

	Pin	RS232	Direction	RS485/422 Full-Duplex	Direction	RS485 Half-Duplex	Direction
IOPIPE 5	IO5A+	-	-	-	-	-	-
	IO5A-	-	-	-	-	-	-
	IO5B+	-	-	-	-	-	-
	IO5B-	-	-	-	-	-	-
	IO5C+	-	-	-	-	-	-
	IO5C-	-	-	-	-	-	-
	IO5D+	-	-	-	-	-	-
	IO5D-	-	-	-	-	-	-
	GND5	System Ground					

Table 9-6 : P12 I/O Connector Pin Assignment – IOPIPE 5