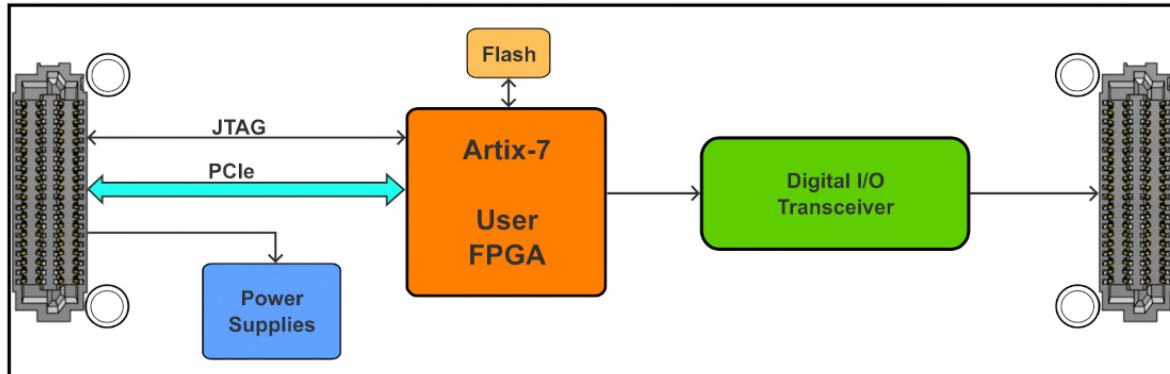


### TQMC600 Reconfigurable FPGA with Digital I/O



TQMC600 Block Diagram

#### Application Information

The TQMC600 is a VITA 93.0 compatible single-width QMC offering a user programmable AMD Artix 7 7A50T FPGA.

Depending on the order option the TQMC600 offers 32 ESD-protected 5V-tolerant TTL lines or 16 differential I/O lines using ESD-protected EIA-422 / EIA-485 compatible line transceivers or Multipoint-LVDS transceivers.

All I/O lines are individually programmable as input or output. TTL I/O lines can be set to high, low, or tristate. Differential I/O lines are terminated, EIA-422 / EIA-485 lines with 120  $\Omega$ , M-LVDS lines with 100  $\Omega$ .

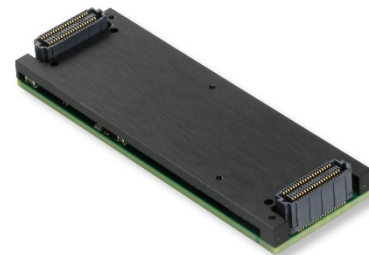
The User FPGA is configured by a SPI flash. An in-circuit debugging option is available via the QMC's JTAG interface for read back and real-time debugging of the FPGA design (using the Vivado ILA).

User applications for the TQMC600 with 7A50T FPGA can be developed using the design software Vivado Design Suite HL WebPACK Edition, which can be downloaded free of charge from [www.xilinx.com](http://www.xilinx.com).

TEWS offers a well-documented basic FPGA Example Application design. It includes a constraints file with all

necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TQMC600. It implements PCIe to register mapping and basic I/O. It comes as a Xilinx Vivado Design Suite project with source code and as a ready-to-download bit stream.

The TQMC600 is available as air cooled and conduction cooled variant.



Conduction Cooled QMC

### Technical Information

- Form Factor: Standard single QMC conforming to VITA 93.0
  - Board size: 78.25 mm x 26 mm
- PCI Express 2.1 compliant interface
- Artix-7 User programmable FPGA
  - Xilinx XC7A50T-2
  - PCIe endpoint in FPGA
- 128 Mbit SPI-EEPROM for FPGA configuration and User Data
- Digital I/O
  - 32 ESD-protected 5 V-tolerant TTL lines (-10R)
  - 16 differential EIA-422 / EIA-485 lines (-11R)
  - 16 differential M-LVDS lines (-12R)
  - Direction individually programmable
- Operating temperature -40 °C to +85 °C

### Order Information

#### RoHS Compliant

<b>TQMC600-10R-A</b>	32 TTL I/O, Artix-7 7A50T FPGA, air cooled
<b>TQMC600-10R-H</b>	32 TTL I/O, Artix-7 7A50T FPGA, conduction cooled
<b>TQMC600-11R-A</b>	16 differential EIA-422 / EIA-485 I/O, Artix-7 7A50T FPGA, air cooled
<b>TQMC600-11R-H</b>	16 differential EIA-422 / EIA-485 I/O, Artix-7 7A50T FPGA, conduction cooled
<b>TQMC600-12R-A</b>	16 differential M-LVDS I/O, Artix-7 7A50T FPGA, air cooled
<b>TQMC600-12R-H</b>	16 differential M-LVDS I/O, Artix-7 7A50T FPGA, conduction cooled

For the availability of non-RoHS compliant (lead solder) products please contact TEWS.

#### Software

<b>TDRV020-SW-25</b>	Integrity Software Support
<b>TDRV020-SW-42</b>	VxWorks Software Support
<b>TDRV020-SW-65</b>	Windows Software Support
<b>TDRV020-SW-82</b>	Linux Software Support
<b>TDRV020-SW-95</b>	QNX Software Support

For other operating systems please contact TEWS.

#### Related Products

<b>TPCE210</b>	2 Site QMC Carrier, PCIe x4, Gen2, low-profile, VHDCI-68 I/O
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