The Embedded I/O Company

TEWS TECHNOLOGIES

TQMC601

32 Isolated Digital Inputs

Version 1.0

User Manual

Issue 1.0.1

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TQMC601-10R-A

32 Isolated Digital Inputs, air cooled

Document History

Issue	Description	Date
1.0.0	Initial Issue	July 2026
1.0.1	• General Improvements • Updated IO Connector Product Number • Updated MTBF Value • Corrected Register Bit Access Types Symbols	August 2026

Table of Contents

List of Figures

List of Tables

1 Product Description

The TQMC601 is a standard single-width QMC module conforming to the VITA 93.0 standard for small form factor (SFF) mezzanine modules. It offers 32 isolated digital inputs that allow reading signals from a multitude of sensors or devices.

Each input can be operated with signalling voltages of 15 V to 60 V.

The individual inputs are separated in groups of 8 sharing a common input ground. These groups are potential free to each other. A high performance input circuit ensures a defined switching point and polarization protection against confusing the pole. All inputs have an electronic debounce circuit with a programmable debounce time.

All inputs can generate an interrupt. The signal edge handling is programmable.

The TQMC601 is available as air cooled and conduction cooled variant.

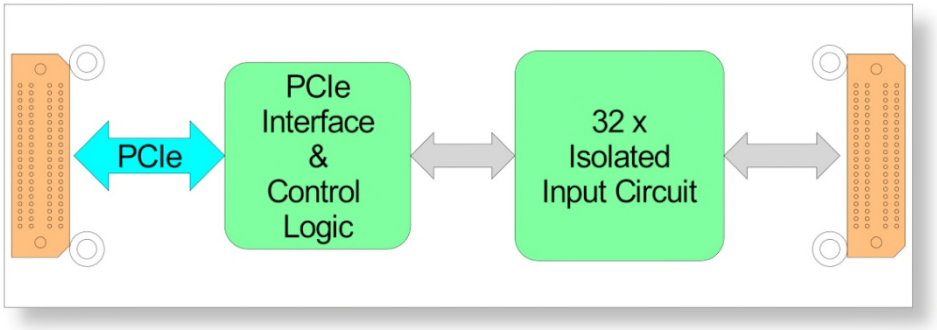


Figure 1-1 : Block Diagram

2 Technical Specification

General	
Mechanical Interface	Small Form Factor Mezzanine Card (QMC) air- or conduction-cooled conforming to VITA93.0 Standard Single-Width (26 mm x 78.25 mm)
Electrical Interface	PCIe Revision 2.1 Gen2 x1 conforming to ANSI/VITA 93.0

Main On Board Devices	
PCIe Interface Chip	AMD Artix™ 7
Input Receiver	ISO1212

I/O Interface	
Digital Inputs	32 Isolated Digital Inputs IEC 61131-2 Type 3 input-characteristic Inputs: 15-60 V (2.25 mA typ.)
Isolation per IPC-2221	566 V against system ground 30 V between IOPIPEs
I/O Connectors	QMC P12 I/O Connector: 80 Position Mezzanine 0.635 mm High-Density 4-Row Socket (Samtec ASP-239729-01)

Physical Data	
Power Requirements	300 mA typical @ +3.3 V DC
Temperature Range	Operating -40 °C to +85 °C Storage -40 °C to +85 °C
MTBF	1948000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	TQMC601-10R-A: 11 g

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with appropriate care!

3.2 Safety Instructions

This module shall only be installed into a system or be removed from a system while the system is powered-off!

This module is intended to be used with nominal voltages of up to 60 VDC on its input lines.

3.3 Forced Air Cooling

This module generates noticeable heat and requires adequate forced air cooling!
Temperature Control is required!

3.4 Isolated I/O Ground

Isolated ground signals on the I/O connector must be connected to the corresponding external ground!

3.5 QMC Installation

QMCs are protected against wrong insertion by a polarization feature incorporated in the connector.

QMCs are easily installed by placing them aligned with the Carrier's connectors and gently pressing them onto the Carrier.

The QMC can now be screwed to the Carrier as needed.

3.6 QMC Removal

When removing the QMC from the Carrier, care must also be taken to ensure that both plugs are disconnected simultaneously and in parallel. To do this, grasp both short sides of the PCB with both hands at the tabs and carefully lift the QMC.

- Remove the screws that secure the QMC on the carrier, if needed.
- Gently and simultaneously unplug both connectors of the QMC.

Be aware that there is a risk of damaging the QMC Module or Carrier during QMC Module extraction. Applying an unequal force to the two connectors while unplugging can cause a misalignment, which then can potentially result in damaging the connectors or boards.

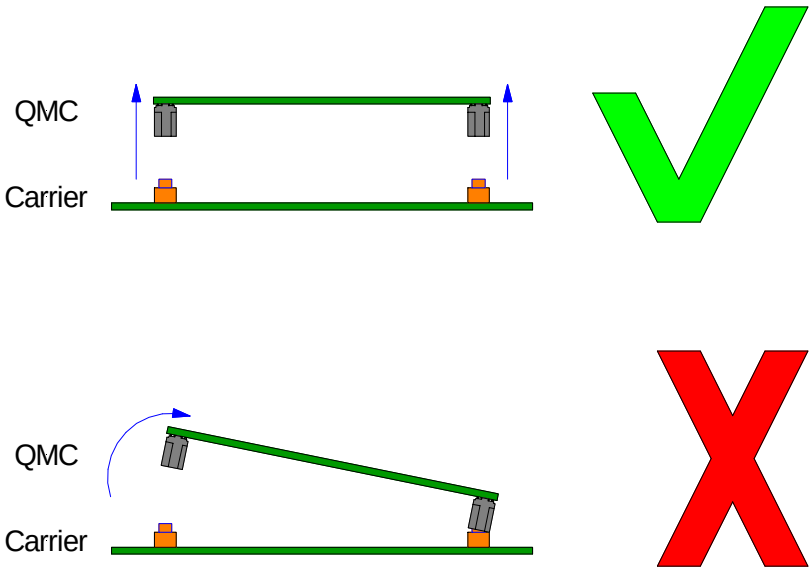


Figure 3-1 : QMC Removal

4 Terms and Definitions

4.1 Register Bit Access Types

Register Bit Access Type		Description
R	Read	The bit is readable by software (not writeable)
W	Write	The bit is writeable by software (not readable)
R/W	Read/Write	The bit is readable and writeable by software
R/W1C (R/C)	Read/Clear	The bit is readable by software The bit is set by firmware Software may clear the bit by writing a '1'
R/W1S (R/S)	Read/Set	The bit is readable by software Software may set this bit to '1' The bit is cleared by firmware

Table 4-1 : Register Bit Access Types

When reading reserved register bits, the read value is undefined.

For future software compatibility: For register write access, reserved bits shall be written '0'.

4.2 Signal Direction Types

Signal Direction Types as stated in Pin Assignment tables.

Signal Direction (Dir)	Description
I	TEWS card input Externally driven signal into the TEWS card
O	TEWS card output Signal driven out by TEWS card
I/O	Bidirectional Signal
OD	TEWS card Open Drain output Signal driven low or tri-stated by TEWS card

Table 4-2 : Signal Direction Types

4.3 Style Conventions

Hexadecimal values are shown with prefix 0x (i.e. 0x029E).

Binary values are shown with prefix 0b (i.e. 0b0110).

"Active Low" signals are shown with a # suffix (i.e. RESET#).

5 Addressing

5.1 PCI Device Identification

	Offset	Setting
Vendor ID	0x00	0x1498 (TEWS Technologies)
Device ID	0x02	0xC259 (TQMC601)
Revision ID	0x08	0x00
Class Code	0x09	0x118000 (Other Data Acquisition/Signal Processing Controllers)
Subsystem Vendor ID	0x2C	0x1498 (TEWS Technologies)
Subsystem ID	0x2E	0xC00A (TQMC601-10R)

Table 5-1 : PCI Device Identification

5.2 Other PCI Configuration Registers

	Offset	Setting
Cache Line Size	0x0C	Not supported
Latency Timer	0x0D	Not supported (PCI Master only)
Header Type	0x0E	0x00
Built-In Self-Test	0x0F	Not supported
Capabilities Pointer	0x34	0x00 (no capability list)
Interrupt Line	0x3C	Supported
Interrupt Pin	0x3D	0x01 (INTA#)
MIN_GNT	0x3E	Not supported (PCI Master only)
MAX_LAT	0x3F	Not supported (PCI Master only)

Table 5-2 : Other PCI Configuration Registers

5.2.1 PCI Base Address Registers

BAR	Offset	Space Mapping	Size (Byte)	Prefetch	Port Width (Bit)	Endian Mode	Description
0	0x10	MEM	512	No	32	Little	Register Space

Table 5-3 : PCI Base Address Registers

5.3 Register Space (BAR 0)

Offset to PCI BAR 0	Register Name	Size (Bit)
Input Functionality		
0x000	Digital Input Register	32
0x004	Reserved	32
0x008	Input Control Register	32
0x00C	Reserved	32
0x010	Rising Edge Interrupt Enable Register	32
0x014	Reserved	32
0x018	Falling Edge Interrupt Enable Register	32
0x01C	Reserved	32
0x020	Rising Edge Interrupt Status Register	32
0x024	Reserved	32
0x028	Falling Edge Interrupt Status Register	32
0x02C	Reserved	32
0x030	Debounce Time Register	32
0x034 : 0x19C	Reserved	32
Interrupt		
0x1A0	Interrupt Control Register	32
0x1A4:0x1A8	Reserved	32
0x1AC	Interrupt Status Register	32
0x1B0:0x1EC	Reserved	32
Extended		
0x1F0 : 0x1F8	Reserved	32
0x1FC	Firmware Version Register	32

Table 5-4 : Register Space Map

5.3.1 Digital Input Register

Bit	Symbol	Description	Access	Reset Value
31	DIN_31	Digital Input [x] Refer to Digital Input 0 for description	R	0
30	DIN_30		R	0
29	DIN_29		R	0
28	DIN_28		R	0
27	DIN_27		R	0
26	DIN_26		R	0
25	DIN_25		R	0
24	DIN_24		R	0
23	DIN_23		R	0
22	DIN_22		R	0
21	DIN_21		R	0
20	DIN_20		R	0
19	DIN_19		R	0
18	DIN_18		R	0
17	DIN_17		R	0
16	DIN_16		R	0
15	DIN_15		R	0
14	DIN_14		R	0
13	DIN_13		R	0
12	DIN_12		R	0
11	DIN_11		R	0
10	DIN_10		R	0
9	DIN_09		R	0
8	DIN_08		R	0
7	DIN_07		R	0
6	DIN_06		R	0
5	DIN_05		R	0
4	DIN_04		R	0
3	DIN_03		R	0
2	DIN_02		R	0
1	DIN_01		R	0
0	DIN_00	Digital Input 0 The bit Indicates the current (debounced) state of the input line.	R	0

Table 5-5 : Digital Input Register

5.3.2 Input Control Register

Bit	Symbol	Description	Access	Reset Value
31:1	-	Reserved	R	0
0	IDEB_EN	Input Debouncer Enable Control the state for the input synchronization circuit. 0b0 := disabled 0b1 := enabled *Setting effects all input lines in common (not selectively)*	R/W	0

Table 5-6 : Input Control Register

5.3.3 Rising Edge Interrupt Enable Register

Bit	Symbol	Description	Access	Reset Value
31	RE_IEN_DIN_31	Rising Edge Interrupt Enable for Digital Input [x] Refer to Rising Edge Interrupt Enable 0 for description	R/W	0
30	RE_IEN_DIN_30		R/W	0
29	RE_IEN_DIN_29		R/W	0
28	RE_IEN_DIN_28		R/W	0
27	RE_IEN_DIN_27		R/W	0
26	RE_IEN_DIN_26		R/W	0
25	RE_IEN_DIN_25		R/W	0
24	RE_IEN_DIN_24		R/W	0
23	RE_IEN_DIN_23		R/W	0
22	RE_IEN_DIN_22		R/W	0
21	RE_IEN_DIN_21		R/W	0
20	RE_IEN_DIN_20		R/W	0
19	RE_IEN_DIN_19		R/W	0
18	RE_IEN_DIN_18		R/W	0
17	RE_IEN_DIN_17		R/W	0
16	RE_IEN_DIN_16		R/W	0
15	RE_IEN_DIN_15		R/W	0
14	RE_IEN_DIN_14		R/W	0
13	RE_IEN_DIN_13		R/W	0

Bit	Symbol	Description	Access	Reset Value
12	RE_IEN_ DIN_12		R/W	0
11	RE_IEN_ DIN_11		R/W	0
10	RE_IEN_ DIN_10		R/W	0
9	RE_IEN_ DIN_09		R/W	0
8	RE_IEN_ DIN_08		R/W	0
7	RE_IEN_ DIN_07		R/W	0
6	RE_IEN_ DIN_06		R/W	0
5	RE_IEN_ DIN_05		R/W	0
4	RE_IEN_ DIN_04		R/W	0
3	RE_IEN_ Din_03		R/W	0
2	RE_IEN_ DIN_02		R/W	0
1	RE_IEN_ DIN_01		R/W	0
0	RE_IEN_ DIN_00	Rising Edge Interrupt Enable for Digital Input 0 Controls the line rising edge interrupt detection. 0b0 := disabled 0b1 := enabled	R/W	0

Table 5-7 : Rising Edge Interrupt Enable Register

5.3.4 Falling Edge Interrupt Enable Register

Bit	Symbol	Description	Access	Reset Value
31	FE_IEN_ DIN_31		R/W	0
30	FE_IEN_ DIN_30		R/W	0
29	FE_IEN_ DIN_29		R/W	0
28	FE_IEN_ DIN_28		R/W	0
27	FE_IEN_ DIN_27	Falling Edge Interrupt Enable for Digital Input [x] Refer to Falling Edge Interrupt Enable 0 for description	R/W	0
26	FE_IEN_ DIN_26		R/W	0
25	FE_IEN_ DIN_25		R/W	0
24	FE_IEN_ DIN_24		R/W	0
23	FE_IEN_ DIN_23		R/W	0

Bit	Symbol	Description	Access	Reset Value
22	FE_IEN_ DIN_22		R/W	0
21	FE_IEN_ DIN_21		R/W	0
20	FE_IEN_ DIN_20		R/W	0
19	FE_IEN_ DIN_19		R/W	0
18	FE_IEN_ DIN_18		R/W	0
17	FE_IEN_ DIN_17		R/W	0
16	FE_IEN_ DIN_16		R/W	0
15	FE_IEN_ DIN_15		R/W	0
14	FE_IEN_ DIN_14		R/W	0
13	FE_IEN_ DIN_13		R/W	0
12	FE_IEN_ DIN_12		R/W	0
11	FE_IEN_ DIN_11		R/W	0
10	FE_IEN_ DIN_10		R/W	0
9	FE_IEN_ DIN_09		R/W	0
8	FE_IEN_ DIN_08		R/W	0
7	FE_IEN_ DIN_07		R/W	0
6	FE_IEN_ DIN_06		R/W	0
5	FE_IEN_ DIN_05		R/W	0
4	FE_IEN_ DIN_04		R/W	0
3	FE_IEN_ DIN_03		R/W	0
2	FE_IEN_ DIN_02		R/W	0
1	FE_IEN_ DIN_01		R/W	0
0	FE_IEN_ DIN_00	Falling Edge Interrupt Enable for Digital Input 0 Controls the line falling edge interrupt detection. 0b0 := disabled 0b1 := enabled	R/W	0

Table 5-8 : Falling Edge Interrupt Enable Register

5.3.5 Rising Edge Interrupt Status Register

Bit	Symbol	Description	Access	Reset Value
31	RE_INT_DIN_31	Rising Edge Interrupt Status for Digital Input [x] Refer to Rising Edge Interrupt Status 0 for description	R/W1C	0
30	RE_INT_DIN_30		R/W1C	0
29	RE_INT_DIN_29		R/W1C	0
28	RE_INT_DIN_28		R/W1C	0
27	RE_INT_DIN_27		R/W1C	0
26	RE_INT_DIN_26		R/W1C	0
25	RE_INT_DIN_25		R/W1C	0
24	RE_INT_DIN_24		R/W1C	0
23	RE_INT_DIN_23		R/W1C	0
22	RE_INT_DIN_22		R/W1C	0
21	RE_INT_DIN_21		R/W1C	0
20	RE_INT_DIN_20		R/W1C	0
19	RE_INT_DIN_19		R/W1C	0
18	RE_INT_DIN_18		R/W1C	0
17	RE_INT_DIN_17		R/W1C	0
16	RE_INT_DIN_16		R/W1C	0
15	RE_INT_DIN_15		R/W1C	0
14	RE_INT_DIN_14		R/W1C	0
13	RE_INT_DIN_13		R/W1C	0
12	RE_INT_DIN_12		R/W1C	0
11	RE_INT_DIN_11		R/W1C	0
10	RE_INT_DIN_10		R/W1C	0
9	RE_INT_DIN_09		R/W1C	0
8	RE_INT_DIN_08		R/W1C	0
7	RE_INT_DIN_07		R/W1C	0

Bit	Symbol	Description	Access	Reset Value
6	RE_INT_ DIN_06		R/W1C	0
5	RE_INT_ DIN_05		R/W1C	0
4	RE_INT_ DIN_04		R/W1C	0
3	RE_INT_ Din_03		R/W1C	0
2	RE_INT_ DIN_02		R/W1C	0
1	RE_INT_ DIN_01		R/W1C	0
0	RE_INT_ DIN_00	Rising Edge Interrupt Status for Digital Input 0 Reflects the line rising edge interrupt status. 0b0 := not pending 0b1 := pending	R/W1C	0

Table 5-9 : Rising Edge Interrupt Status Register

5.3.6 Falling Edge Interrupt Status Register

Bit	Symbol	Description	Access	Reset Value
31	FE_INT_ DIN_31		R/W1C	0
30	FE_INT_ DIN_30		R/W1C	0
29	FE_INT_ DIN_29		R/W1C	0
28	FE_INT_ DIN_28		R/W1C	0
27	FE_INT_ DIN_27		R/W1C	0
26	FE_INT_ DIN_26		R/W1C	0
25	FE_INT_ DIN_25		R/W1C	0
24	FE_INT_ DIN_24	Falling Edge Interrupt Status for Digital Input [x] Refer to Falling Edge Interrupt Status 0 for description	R/W1C	0
23	FE_INT_ DIN_23		R/W1C	0
22	FE_INT_ DIN_22		R/W1C	0
21	FE_INT_ DIN_21		R/W1C	0
20	FE_INT_ DIN_20		R/W1C	0
19	FE_INT_ DIN_19		R/W1C	0
18	FE_INT_ DIN_18		R/W1C	0
17	FE_INT_ DIN_17		R/W1C	0

Bit	Symbol	Description	Access	Reset Value
16	FE_INT_ DIN_16		R/W1C	0
15	FE_INT_ DIN_15		R/W1C	0
14	FE_INT_ DIN_14		R/W1C	0
13	FE_INT_ DIN_13		R/W1C	0
12	FE_INT_ DIN_12		R/W1C	0
11	FE_INT_ DIN_11		R/W1C	0
10	FE_INT_ DIN_10		R/W1C	0
9	FE_INT_ DIN_09		R/W1C	0
8	FE_INT_ DIN_08		R/W1C	0
7	FE_INT_ DIN_07		R/W1C	0
6	FE_INT_ DIN_06		R/W1C	0
5	FE_INT_ DIN_05		R/W1C	0
4	FE_INT_ DIN_04		R/W1C	0
3	FE_INT_ DIN_03		R/W1C	0
2	FE_INT_ DIN_02		R/W1C	0
1	FE_INT_ DIN_01		R/W1C	0
0	FE_INT_ DIN_00	Falling Edge Interrupt Status for Digital Input 0 Reflects the line falling edge interrupt status. 0b0 := not pending 0b1 := pending	R/W1C	0

Table 5-10 : Falling Edge Interrupt Status Register

5.3.7 Input Debounce Time Register

Bit	Symbol	Description	Access	Reset Value
31:8	IDEB_ TMR_VAL	Input Debounce Time Value Sets the debounce time t_{db} of the input synchronization circuit using the following formula: $IDEB_{TMR_{VAL}} = \left(\frac{t_{db}(ns)}{8}\right) - 1$ Any debounce time in the range of 8ns to 134ms can be programmed in step of approx. 8ns. The debounce time is common for all 32 inputs. *Timing is based on PCIe clocking and may be affected by spread spectrum variations (up to +0.5%) if present.*	R/W	0
7:0	-	Reserved	R	0

Table 5-11 : Input Debounce Time Register

To make use of the debounce feature the Input Debounce Enable (IDEB_EN) must be enabled.

5.3.8 Interrupt Control Register

Bit	Symbol	Description	Access	Reset Value
31	INT_ACK_ MODE	Interrupt Acknowledge Mode 0b0 := Interrupts are cleared by write (R/W1C) 0b1 := Interrupts are cleared by read (R)	R/W	0
30:1	-	Reserved	R	0
0	GINT_EN	Global Interrupt Enable Master interrupt control (mask). 0b0 := disabled 0b1 := enabled *Setting effects all input lines in common (not selectively)*	R/W	0

Table 5-12 : Interrupt Control Register

5.3.9 Interrupt Status Register

Bit	Symbol	Description	Access	Reset Value
31	FE_INT_ STAT	Or-Wired Falling Edge Interrupt Status Register	R	0
30	RE_INT_ STAT	Or-Wired Rising Edge Interrupt Status Register	R	0
29:0	-	Reserved	R	0

Table 5-13 : Interrupt Status Register

6 Interrupts

6.1 Interrupt Sources

Data Input Edge Interrupt:

The firmware is capable of generating independent interrupts for rising and falling edge events per single data input line (DIN_[x]).

- Rising Edge Interrupt on Data Input [31:0]
- Falling Edge Interrupt on Data Input [31:0]

6.2 Interrupt Handling

Data Input Edge Interrupt:

There are interrupt status registers for rising (RE_INT_DIN_[x]) and falling interrupts (FE_INT_DIN_[x]). Bits within these registers can always be read and when set, cleared by high-active writing (R/W1C).

Interrupt clearing method is configurable (INT_ACK_MODE). Default is Clear-by-Write, Clear-on-Read is supported.

If an interrupt is enabled, either for rising edge (RE_IEN_DIN_[x]) or falling edge (FE_IEN_DIN_[x]), and a corresponding data input line transition is detected, the corresponding bit is set within the appropriate interrupt status register.

Disabling an already set (registered) interrupt event (RE_IEN_DIN_[x] or FE_IEN_DIN_[x]) does not clear the event.

Bits insides these registers are or-wired to generate a single internal interrupt request.

Global Interrupt Control/Status:

Internal interrupt requests are controlled (masked) by a global interrupt enable (GINT_EN).

If not enabled, host interrupts are suppressed. Deactivating a pending host interrupt does not clear any already set (registered) interrupt events nor prevents capturing those.

For handling reasons, there is an additional (global) Interrupt Status Register containing look-up bits for the Data Input Edge Interrupt Status Registers (RE_INT_DIN_[x] and FE_INT_DIN_[x]).

When either or both and the global interrupt enable are set, an active interrupt sourced by either or both of these registers is indicated.

Processing is not performed through the Interrupt Status Register. It is just used for indication purposes.

7 Input Interface Description

The TQMC601 has 32 digital inputs with IEC 61131-2 Type 3 input-characteristic. The standard signal level for these inputs is 24V DC. The switching level of the inputs is between 5 V and 11 V. Maximum allowed input voltage is 60 V.

7.1 Galvanic Isolation

All inputs are isolated by digital input isolators from the computer system and are also isolated against each other in groups of eight inputs.

Group	Ground	Input
I0	GND_I0	IN 0 IN 1 IN 2 IN 3 IN 4 IN 5 IN 6 IN 7
I1	GND_I1	IN 8 IN 9 IN 10 IN 11 IN 12 IN 13 IN 14 IN 15
I2	GND_I2	IN 16 IN 17 IN 18 IN 19 IN 20 IN 21 IN 22 IN 23
I3	GND_I3	IN 24 IN 25 IN 26 IN 27 IN 28 IN 29 IN 30 IN 31

Table 7-1 : Isolated Digital Inputs

7.2 Debounce Function

A programmable debounce function (input synchronization circuit) common for all inputs is implemented on the TQMC601. There is only one debounce time adjustable for all 32 digital inputs.

If the debounce function is enabled, an input pin must be stable for the programmed debounce time before the rising or falling edge is recognized as valid. So only after a correct identification the Digital Input Register is updated and an interrupt is generated.

To make use of the debounce feature the Input Debounce Enable (IDEB_EN) must be enabled.

7.3 Interrupt Logic

Interrupt generation can be individually programmed for each input transition. To enable the interrupt after a reset, the Global Interrupt Enable bit (GINT_EN) in the Interrupt Control Register must be set to the value '1'. Also the respective bit for rising or falling edge in the Rising Edge / Falling Edge Interrupt Enable Register must be set.

The Global Interrupt Enable bit and also all individually interrupt enable bits are disabled after power-on and reset.

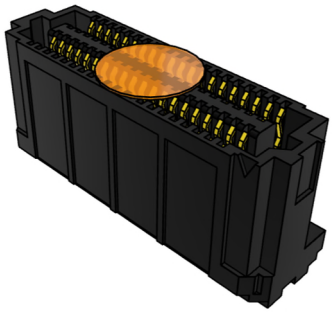
7.4 Thermal Considerations

The power dissipated inside the digital input devices on the TQMC601 is determined by the voltage at the input pin (up to 60 V) and the current drawn by the device (2.25 mA/Channel typ. for IEC 61131-2 Type 3). The maximum power dissipation could be therefore as high as: Pmax = 60 V * 2.25 mA * 32 = 4.32 W.

As a result, the module generates noticeable heat (especially at high input voltages) and requires adequate forced air cooling.

7.5 I/O Connector P12

Pin-Count	80 Pins
Connector Type	80 Position Mezzanine 0.635 mm High-Density 4-Row Socket
Source & Order Info	Samtec ASP-239729-01



7.5.1 IOPIPE 1

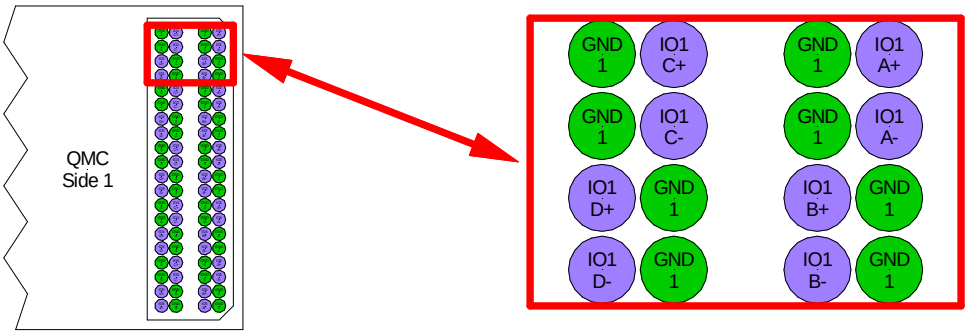


Figure 7-1 : P12 I/O Connector – IOPIPE 1

	Pin	Signal	Description
IOPIPE 1	IO1_A+	IN 0	Input Line 0
	IO1_A-	IN 1	Input Line 1
	IO1_B+	IN 2	Input Line 2
	IO1_B-	IN 3	Input Line 3
	IO1_C+	IN 4	Input Line 4
	IO1_C-	IN 5	Input Line 5
	IO1_D+	IN 6	Input Line 6
	IO1_D-	IN 7	Input Line 7
	GND1	GND IN 0 .. IN 7	IOPIPE1 Ground

Table 7-2 : P12 I/O Connector Pin Assignment – IOPIPE 1

7.5.2 IOPIPE 2

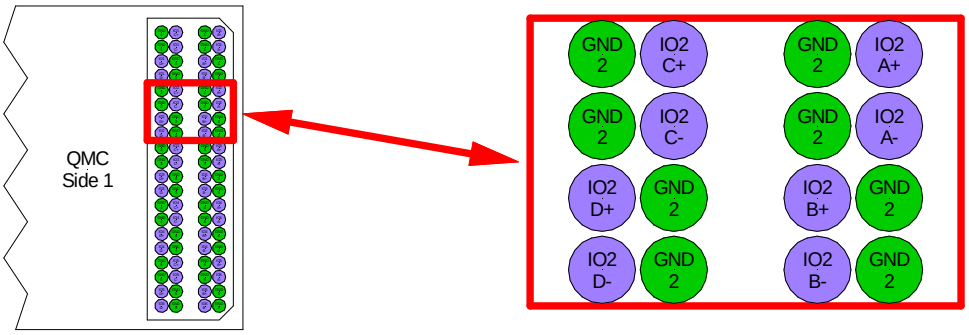


Figure 7-2 : P12 I/O Connector – IOPIPE 2

	Pin	Signal	Description
IOPIPE 2	IO2_A+	IN 8	Input Line 8
	IO2_A-	IN 9	Input Line 9
	IO2_B+	IN 10	Input Line 10
	IO2_B-	IN 11	Input Line 11
	IO2_C+	IN 12	Input Line 12
	IO2_C-	IN 13	Input Line 13
	IO2_D+	IN 14	Input Line 14
	IO2_D-	IN 15	Input Line 15
	GND2	GND IN 8 .. IN 15	IOPIPE2 Ground

Table 7-3 : P12 I/O Connector Pin Assignment – IOPIPE 2

7.5.3 IOPIPE 3

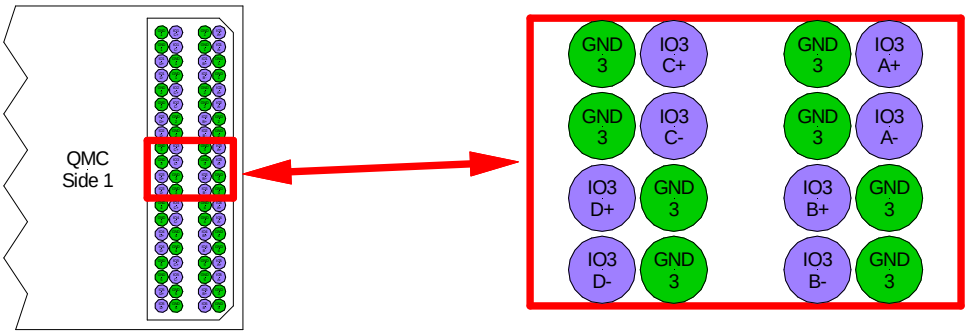


Figure 7-3 : P12 I/O Connector – IOPIPE 3

	Pin	Signal	Description
IOPIPE 3	IO3_A+	IN 16	Input Line 16
	IO3_A-	IN 17	Input Line 17
	IO3_B+	IN 18	Input Line 18
	IO3_B-	IN 19	Input Line 19
	IO3_C+	IN 20	Input Line 20
	IO3_C-	IN 21	Input Line 21
	IO3_D+	IN 22	Input Line 22
	IO3_D-	IN 23	Input Line 23
	GND3	GND IN 16 .. IN 23	IOPIPE3 Ground

Table 7-4 : P12 I/O Connector Pin Assignment – IOPIPE 3

7.5.4 IOPIPE 4

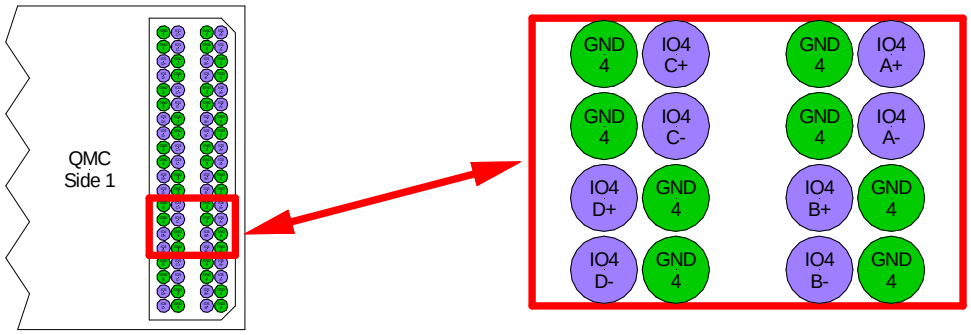


Figure 7-4 : P12 I/O Connector – IOPIPE 4

	Pin	Signal	Description
IOPIPE 4	IO4_A+	IN 24	Input Line 24
	IO4_A-	IN 25	Input Line 25
	IO4_B+	IN 26	Input Line 26
	IO4_B-	IN 27	Input Line 27
	IO4_C+	IN 28	Input Line 28
	IO4_C-	IN 29	Input Line 30
	IO4_D+	IN 30	Input Line 30
	IO4_D-	IN 31	Input Line 31
	GND4	GND IN 24 .. IN 31	IOPIPE4 Ground

Table 7-5 : P12 I/O Connector Pin Assignment – IOPIPE 4