

# TQMC604

## 32 Isolated Digital Outputs

Version 1.0

### User Manual

Issue 1.0.1

July 2026

---

## **TQMC604-10R-A**

32 Isolated Digital Outputs, air cooled

This document contains information, which is proprietary to TEWS Technologies GmbH. Any reproduction without written permission is forbidden.

TEWS Technologies GmbH has made any effort to ensure that this manual is accurate and complete. However TEWS Technologies GmbH reserves the right to change the product described in this document at any time without notice.

TEWS Technologies GmbH is not liable for any damage arising out of the application or use of the device described herein.

©2026 by TEWS Technologies GmbH

All trademarks mentioned are property of their respective owners.

## Document History

| Issue | Description                                                                                                                                                                                             | Date        |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|
| 1.0.0 | Initial Issue                                                                                                                                                                                           | July 2026   |
| 1.0.1 | <ul style="list-style-type: none"><li>• General Improvements</li><li>• Updated IO Connector Product Number</li><li>• Updated MTBF Value</li><li>• Corrected Register Bit Access Types Symbols</li></ul> | August 2026 |

# Table of Contents

|                                              |           |
|----------------------------------------------|-----------|
| <b>TQMC604</b>                               | <b>1</b>  |
| Document History                             | 3         |
| Table of Contents                            | 4         |
| List of Figures                              | 6         |
| List of Tables                               | 7         |
| <b>1 PRODUCT DESCRIPTION</b>                 | <b>8</b>  |
| <b>2 TECHNICAL SPECIFICATION</b>             | <b>9</b>  |
| <b>3 HANDLING AND OPERATION INSTRUCTIONS</b> | <b>10</b> |
| 3.1 ESD Protection                           | 10        |
| 3.2 Safety Instructions                      | 10        |
| 3.3 Forced Air Cooling                       | 10        |
| 3.4 Isolated I/O Ground                      | 10        |
| 3.5 QMC Installation                         | 11        |
| 3.6 QMC Removal                              | 11        |
| <b>4 TERMS AND DEFINITIONS</b>               | <b>12</b> |
| 4.1 Register Bit Access Types                | 12        |
| 4.2 Signal Direction Types                   | 12        |
| 4.3 Style Conventions                        | 12        |
| <b>5 ADDRESSING</b>                          | <b>13</b> |
| 5.1 PCI Device Identification                | 13        |
| 5.2 Other PCI Configuration Registers        | 13        |
| 5.2.1 PCI Base Address Registers             | 13        |
| 5.3 Register Space (BAR 0)                   | 14        |
| 5.3.1 Digital Output Register                | 15        |
| 5.3.2 Output Configuration Register 0        | 16        |
| 5.3.3 Output Configuration Register 1        | 17        |
| 5.3.4 Output Fault Status Register           | 18        |
| 5.3.5 Output Control Register                | 19        |
| 5.3.6 Watchdog Time Register                 | 19        |
| 5.3.7 Watchdog Output Safe-State Register    | 20        |
| 5.3.8 Watchdog Status Register               | 21        |
| 5.3.9 Interrupt Control Register             | 21        |
| 5.3.10 Interrupt Status Register             | 21        |
| <b>6 INTERRUPTS</b>                          | <b>22</b> |
| 6.1 Interrupt Sources                        | 22        |
| 6.2 Interrupt Handling                       | 22        |
| <b>7 INPUT INTERFACE DESCRIPTION</b>         | <b>23</b> |
| 7.1 Galvanic Isolation                       | 23        |
| 7.2 Output Configuration                     | 24        |
| 7.3 Fault Detection                          | 25        |
| 7.4 Output Watchdog                          | 25        |
| 7.5 Thermal Considerations                   | 25        |
| <b>8 I/O CONNECTOR P12</b>                   | <b>26</b> |
| 8.1.1 IOPIPE 1                               | 27        |
| 8.1.2 IOPIPE 2                               | 28        |
| 8.1.3 IOPIPE 3                               | 29        |
| 8.1.4 IOPIPE 4                               | 30        |

---

|              |                       |           |
|--------------|-----------------------|-----------|
| <b>8.1.5</b> | <b>IOPIPE 5 .....</b> | <b>31</b> |
|--------------|-----------------------|-----------|

## List of Figures

|                                                   |    |
|---------------------------------------------------|----|
| FIGURE 1-1 : BLOCK DIAGRAM.....                   | 8  |
| FIGURE 3-1 : QMC REMOVAL.....                     | 11 |
| FIGURE 7-1 : HIGH-SIDE DRIVER CONFIGURATION ..... | 24 |
| FIGURE 7-2 : LOW-SIDE DRIVER CONFIGURATION .....  | 24 |
| FIGURE 8-1 : P12 I/O CONNECTOR – IOPIPE 1 .....   | 27 |
| FIGURE 8-2 : P12 I/O CONNECTOR – IOPIPE 2 .....   | 28 |
| FIGURE 8-3 : P12 I/O CONNECTOR – IOPIPE 3 .....   | 29 |
| FIGURE 8-4 : P12 I/O CONNECTOR – IOPIPE 4 .....   | 30 |
| FIGURE 8-5 : P12 I/O CONNECTOR – IOPIPE 5 .....   | 31 |

## List of Tables

|                                                               |    |
|---------------------------------------------------------------|----|
| TABLE 2-1 : TECHNICAL SPECIFICATION.....                      | 9  |
| TABLE 4-1 : REGISTER BIT ACCESS TYPES .....                   | 12 |
| TABLE 4-2 : SIGNAL DIRECTION TYPES .....                      | 12 |
| TABLE 5-1 : PCI DEVICE IDENTIFICATION.....                    | 13 |
| TABLE 5-2 : OTHER PCI CONFIGURATION REGISTERS .....           | 13 |
| TABLE 5-3 : PCI BASE ADDRESS REGISTERS.....                   | 13 |
| TABLE 5-4 : REGISTER SPACE MAP .....                          | 14 |
| TABLE 5-5 : DIGITAL OUTPUT REGISTER.....                      | 15 |
| TABLE 5-6 : OUTPUT CONFIGURATION REGISTER 0 .....             | 16 |
| TABLE 5-7 : OUTPUT CONFIGURATION REGISTER 1 .....             | 17 |
| TABLE 5-8 : OUTPUT FAULT STATUS REGISTER.....                 | 18 |
| TABLE 5-9 : OUTPUT CONTROL REGISTER .....                     | 19 |
| TABLE 5-10 : WATCHDOG TIME REGISTER .....                     | 19 |
| TABLE 5-11 : WATCHDOG OUTPUT SAFE-STATE REGISTER.....         | 20 |
| TABLE 5-12 : WATCHDOG STATUS REGISTER.....                    | 21 |
| TABLE 5-13 : INTERRUPT CONTROL REGISTER .....                 | 21 |
| TABLE 5-14 : INTERRUPT STATUS REGISTER.....                   | 21 |
| TABLE 7-1 : ISOLATED DIGITAL OUTPUTS.....                     | 23 |
| TABLE 8-1 : P12 I/O CONNECTOR PIN ASSIGNMENT – IOPIPE 1 ..... | 27 |
| TABLE 8-2 : P12 I/O CONNECTOR PIN ASSIGNMENT – IOPIPE 2 ..... | 28 |
| TABLE 8-3 : P12 I/O CONNECTOR PIN ASSIGNMENT – IOPIPE 3 ..... | 29 |
| TABLE 8-4 : P12 I/O CONNECTOR PIN ASSIGNMENT – IOPIPE 4 ..... | 30 |
| TABLE 8-5 : P12 I/O CONNECTOR PIN ASSIGNMENT – IOPIPE 5 ..... | 31 |

# 1 Product Description

The TQMC604 is a standard single-width QMC module conforming to the VITA 93.0 standard for small form factor (SFF) mezzanine modules. It offers 32 digital outputs with galvanic isolation.

The output drivers work with 5 V up to 36 V supply and are capable of driving 0.15 A continuous per channel. All outputs resist short-circuits and are protected against reverse polarity, thermal overload and overvoltage events up to 65 V.

Outputs are isolated from the system and in groups of eight against each other. Each group of 8 outputs can be software configured as high-side or low-side switch.

A hardware watchdog clears all outputs in case of trigger failure.

The TQMC604 is available as air cooled and conduction cooled variant.

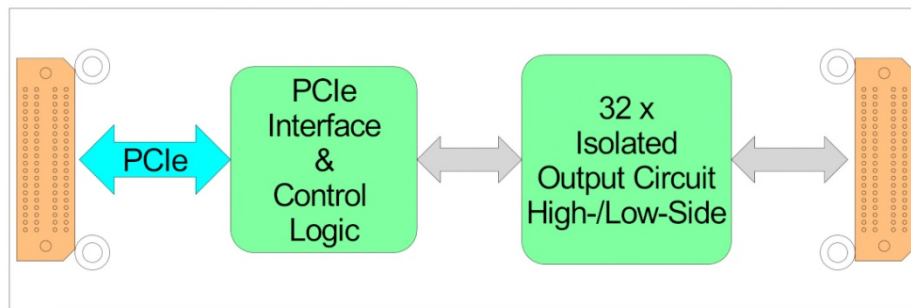


Figure 1-1 : Block Diagram

## 2 Technical Specification

| General                |                                                                                                                                                                                                                                                                                                                                                                    |
|------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Mechanical Interface   | Small Form Factor Mezzanine Card (QMC) air- or conduction-cooled conforming to VITA93.0<br>Standard Single-Width (26 mm x 78.25 mm)                                                                                                                                                                                                                                |
| Electrical Interface   | PCIe Revision 2.1 Gen2 x1 conforming to ANSI/VITA 93.0                                                                                                                                                                                                                                                                                                             |
| Main On Board Devices  |                                                                                                                                                                                                                                                                                                                                                                    |
| PCIe Interface Chip    | AMD Artix™ 7                                                                                                                                                                                                                                                                                                                                                       |
| Digital Isolator       | ISO7761F                                                                                                                                                                                                                                                                                                                                                           |
| Output Driver          | TIOS1023                                                                                                                                                                                                                                                                                                                                                           |
| I/O Interface          |                                                                                                                                                                                                                                                                                                                                                                    |
| Digital Outputs        | 32 Isolated Digital Outputs<br>Output supply Voltage: 5-36 V (0.15 A per output)                                                                                                                                                                                                                                                                                   |
| Isolation per IPC-2221 | 566 V against system ground<br>30 V between IOPIPEs                                                                                                                                                                                                                                                                                                                |
| I/O Connectors         | QMC P12 I/O Connector:<br>80 Position Mezzanine 0.635 mm High-Density 4-Row Socket (Samtec ASP-239729-01)                                                                                                                                                                                                                                                          |
| Physical Data          |                                                                                                                                                                                                                                                                                                                                                                    |
| Power Requirements     | System: 270 mA typical @ +3.3 V DC                                                                                                                                                                                                                                                                                                                                 |
| Temperature Range      | Operating -40 °C to +85 °C<br>Storage -40 °C to +85 °C                                                                                                                                                                                                                                                                                                             |
| MTBF                   | 1747000 h<br>MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G <sub>B</sub> 20°C.<br>The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation. |
| Humidity               | 5 – 95 % non-condensing                                                                                                                                                                                                                                                                                                                                            |
| Weight                 | TQMC604-10R-A: 12 g                                                                                                                                                                                                                                                                                                                                                |

Table 2-1 : Technical Specification

## 3 Handling and Operation Instructions

### 3.1 ESD Protection



This module is sensitive to static electricity.  
Packing, unpacking and all other module handling has to be done with appropriate care!

### 3.2 Safety Instructions



This module shall only be installed into a system or be removed from a system while the system is powered-off!

### 3.3 Forced Air Cooling



This module generates noticeable heat and requires adequate forced air cooling!  
Temperature Control is required!

### 3.4 Isolated I/O Ground



Isolated ground signals on the I/O connector must be connected to the corresponding external ground!

## 3.5 QMC Installation

QMCs are protected against wrong insertion by a polarization feature incorporated in the connector.

QMCs are easily installed by placing them aligned with the Carrier's connectors and gently pressing them onto the Carrier.

The QMC can now be screwed to the Carrier as needed.

## 3.6 QMC Removal

When removing the QMC from the Carrier, care must also be taken to ensure that both plugs are disconnected simultaneously and in parallel. To do this, grasp both short sides of the PCB with both hands at the tabs and carefully lift the QMC.

- Remove the screws that secure the QMC on the carrier, if needed.
- Gently and simultaneously unplug both connectors of the QMC.

Be aware that there is a risk of damaging the QMC Module or Carrier during QMC Module extraction. Applying an unequal force to the two connectors while unplugging can cause a misalignment, which then can potentially result in damaging the connectors or boards.

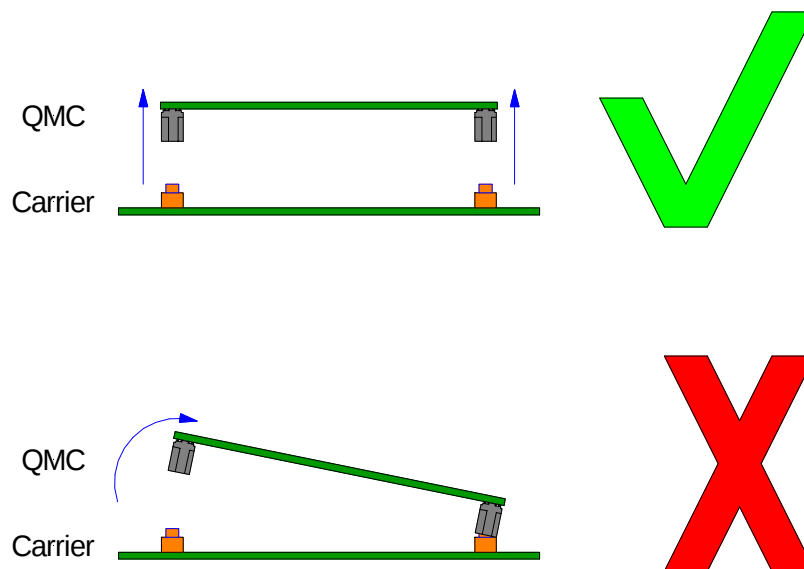


Figure 3-1 : QMC Removal

## 4 Terms and Definitions

### 4.1 Register Bit Access Types

| Register Bit Access Type |            | Description                                                                                                  |
|--------------------------|------------|--------------------------------------------------------------------------------------------------------------|
| R                        | Read       | The bit is readable by software (not writeable)                                                              |
| W                        | Write      | The bit is writeable by software (not readable)                                                              |
| R/W                      | Read/Write | The bit is readable and writeable by software                                                                |
| R/W1C<br>(R/C)           | Read/Clear | The bit is readable by software<br>The bit is set by firmware<br>Software may clear the bit by writing a '1' |
| R/W1S<br>(R/S)           | Read/Set   | The bit is readable by software<br>Software may set this bit to '1'<br>The bit is cleared by firmware        |

Table 4-1 : Register Bit Access Types

**When reading reserved register bits, the read value is undefined.**

**For future software compatibility: For register write access, reserved bits shall be written '0'.**

### 4.2 Signal Direction Types

Signal Direction Types as stated in Pin Assignment tables.

| Signal Direction (Dir) | Description                                                                 |
|------------------------|-----------------------------------------------------------------------------|
| I                      | TEWS card input<br>Externally driven signal into the TEWS card              |
| O                      | TEWS card output<br>Signal driven out by TEWS card                          |
| I/O                    | Bidirectional Signal                                                        |
| OD                     | TEWS card Open Drain output<br>Signal driven low or tri-stated by TEWS card |

Table 4-2 : Signal Direction Types

### 4.3 Style Conventions

Hexadecimal values are shown with prefix 0x (i.e. 0x029E).

Binary values are shown with prefix 0b (i.e. 0b0110).

"Active Low" signals are shown with a # suffix (i.e. RESET#).

## 5 Addressing

### 5.1 PCI Device Identification

|                     | Offset | Setting                                                         |
|---------------------|--------|-----------------------------------------------------------------|
| Vendor ID           | 0x00   | 0x1498 (TEWS Technologies)                                      |
| Device ID           | 0x02   | 0xC25C (TQMC604)                                                |
| Revision ID         | 0x08   | 0x00                                                            |
| Class Code          | 0x09   | 0x118000 (Other Data Acquisition/Signal Processing Controllers) |
| Subsystem Vendor ID | 0x2C   | 0x1498 (TEWS Technologies)                                      |
| Subsystem ID        | 0x2E   | 0xC00A (TQMC604-10R)                                            |

Table 5-1 : PCI Device Identification

### 5.2 Other PCI Configuration Registers

|                      | Offset | Setting                         |
|----------------------|--------|---------------------------------|
| Cache Line Size      | 0x0C   | Not supported                   |
| Latency Timer        | 0x0D   | Not supported (PCI Master only) |
| Header Type          | 0x0E   | 0x00                            |
| Built-In Self-Test   | 0x0F   | Not supported                   |
| Capabilities Pointer | 0x34   | 0x00 (no capability list)       |
| Interrupt Line       | 0x3C   | Supported                       |
| Interrupt Pin        | 0x3D   | 0x01 (INTA#)                    |
| MIN_GNT              | 0x3E   | Not supported (PCI Master only) |
| MAX_LAT              | 0x3F   | Not supported (PCI Master only) |

Table 5-2 : Other PCI Configuration Registers

#### 5.2.1 PCI Base Address Registers

| BAR | Offset | Space Mapping | Size (Byte) | Prefetch | Port Width (Bit) | Endian Mode | Description    |
|-----|--------|---------------|-------------|----------|------------------|-------------|----------------|
| 0   | 0x10   | MEM           | 512         | No       | 32               | Little      | Register Space |

Table 5-3 : PCI Base Address Registers

## 5.3 Register Space (BAR 0)

| Offset to PCI BAR 0         | Register Name                       | Size (Bit) |
|-----------------------------|-------------------------------------|------------|
| 0x000:0x0AC                 | Reserved                            | 32         |
| <b>Output Functionality</b> |                                     |            |
| 0x0B0                       | Digital Output Register             | 32         |
| 0x0B4                       | Reserved                            | 32         |
| 0x0B8                       | Output Configuration Register 0     | 32         |
| 0x0BC                       | Output Configuration Register 1     | 32         |
| 0x0C0                       | Reserved                            | 32         |
| 0x0C4                       | Reserved                            | 32         |
| 0x0C8                       | Output Fault Status Register        | 32         |
| 0x0CC                       | Reserved                            | 32         |
| 0x0D0                       | Output Control Register             | 32         |
| 0x0D4                       | Watchdog Time Register              | 32         |
| 0x0D8                       | Watchdog Output Safe-State Register | 32         |
| 0x0DC                       | Reserved                            | 32         |
| 0x0E0                       | Watchdog Status Register            | 32         |
| 0x0E4: 0x19C                | Reserved                            | 32         |
| <b>Interrupt</b>            |                                     |            |
| 0x1A0                       | Interrupt Control Register          | 32         |
| 0x1A4:0x1A8                 | Reserved                            | 32         |
| 0x1AC                       | Interrupt Status Register           | 32         |
| 0x1B0:0x1EC                 | Reserved                            | 32         |
| <b>Extended</b>             |                                     |            |
| 0x1F0 : 0x1F8               | Reserved                            | 32         |
| 0x1FC                       | Firmware Version Register           | 32         |

Table 5-4 : Register Space Map

### 5.3.1 Digital Output Register

| Bit | Symbol    | Description                                                                                                                                                                                                                                                                                                                                                                                                | Access | Reset Value |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
|-----|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------|--|--|--|-----------|----------|------|----------|-----|-----|-----|-----|---|-----|-----|-----|-----|---|-----|---|
| 31  | DOUT_31   | Digital Output [x]<br>Refer to Digital Output 0 for description                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 30  | DOUT_30   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 29  | DOUT_29   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 28  | DOUT_28   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 27  | DOUT_27   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 26  | DOUT_26   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 25  | DOUT_25   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 24  | DOUT_24   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 23  | DOUT_23   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 22  | DOUT_22   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 21  | DOUT_21   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 20  | DOUT_20   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 19  | DOUT_19   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 18  | DOUT_18   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 17  | DOUT_17   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 16  | DOUT_16   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 15  | DOUT_15   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 14  | DOUT_14   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 13  | DOUT_13   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 12  | DOUT_12   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 11  | DOUT_11   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 10  | DOUT_10   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 9   | DOUT_09   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 8   | DOUT_08   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 7   | DOUT_07   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 6   | DOUT_06   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 5   | DOUT_05   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 4   | DOUT_04   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 3   | DOUT_03   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 2   | DOUT_02   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 1   | DOUT_01   |                                                                                                                                                                                                                                                                                                                                                                                                            | R/W    | 0           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 0   | DOUT_00   | Digital Output 0<br>Controls the state of the output line.<br><table border="1"> <thead> <tr> <th rowspan="2"></th><th colspan="4">Mode</th></tr> <tr> <th>High-Side</th><th>Low-Side</th><th>Hi-Z</th><th>Reserved</th></tr> </thead> <tbody> <tr> <td>0b0</td><td>OFF</td><td>OFF</td><td>OFF</td><td>-</td></tr> <tr> <td>0b1</td><td>VCC</td><td>GND</td><td>OFF</td><td>-</td></tr> </tbody> </table> |        | Mode        |  |  |  | High-Side | Low-Side | Hi-Z | Reserved | 0b0 | OFF | OFF | OFF | - | 0b1 | VCC | GND | OFF | - | R/W | 0 |
|     | Mode      |                                                                                                                                                                                                                                                                                                                                                                                                            |        |             |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
|     | High-Side | Low-Side                                                                                                                                                                                                                                                                                                                                                                                                   | Hi-Z   | Reserved    |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 0b0 | OFF       | OFF                                                                                                                                                                                                                                                                                                                                                                                                        | OFF    | -           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 0b1 | VCC       | GND                                                                                                                                                                                                                                                                                                                                                                                                        | OFF    | -           |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |

Table 5-5 : Digital Output Register

### 5.3.2 Output Configuration Register 0

| Bit   | Symbol      | Description                                                                                                                                                                | Access | Reset Value |
|-------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------|
| 31:26 | -           | Reserved                                                                                                                                                                   | R      | 0           |
| 25:24 | DOUT_CFG_12 | Digital Output Configuration 12<br>Configures side-switching of digital output lines [15:12].<br>0b00 := low-side<br>0b01 := high-side<br>0b10 := Hi-Z<br>0b11 := reserved | R/W    | 2           |
| 23:18 | -           | Reserved                                                                                                                                                                   | R      | 0           |
| 17:16 | DOUT_CFG_08 | Digital Output Configuration 8<br>Configures side-switching of digital output lines [11:08].<br>0b00 := low-side<br>0b01 := high-side<br>0b10 := Hi-Z<br>0b11 := reserved  | R/W    | 2           |
| 15:10 | -           | Reserved                                                                                                                                                                   | R      | 0           |
| 9:8   | DOUT_CFG_04 | Digital Output Configuration 4<br>Configures side-switching of digital output lines [07:04].<br>0b00 := low-side<br>0b01 := high-side<br>0b10 := Hi-Z<br>0b11 := reserved  | R/W    | 2           |
| 7:2   | -           | Reserved                                                                                                                                                                   | R      | 0           |
| 1:0   | DOUT_CFG_00 | Digital Output Configuration 0<br>Configures side-switching of digital output lines [03:00].<br>0b00 := low-side<br>0b01 := high-side<br>0b10 := Hi-Z<br>0b11 := reserved  | R/W    | 2           |

Table 5-6 : Output Configuration Register 0

### 5.3.3 Output Configuration Register 1

| Bit   | Symbol      | Description                                                                                                                                                                | Access | Reset Value |
|-------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------|
| 31:26 | -           | Reserved                                                                                                                                                                   | R      | 0           |
| 25:24 | DOUT_CFG_28 | Digital Output Configuration 28<br>Configures side-switching of digital output lines [31:28].<br>0b00 := low-side<br>0b01 := high-side<br>0b10 := Hi-Z<br>0b11 := reserved | R/W    | 2           |
| 23:18 | -           | Reserved                                                                                                                                                                   | R      | 0           |
| 17:16 | DOUT_CFG_24 | Digital Output Configuration 24<br>Configures side-switching of digital output lines [27:24].<br>0b00 := low-side<br>0b01 := high-side<br>0b10 := Hi-Z<br>0b11 := reserved | R/W    | 2           |
| 15:10 | -           | Reserved                                                                                                                                                                   | R      | 0           |
| 9:8   | DOUT_CFG_20 | Digital Output Configuration 20<br>Configures side-switching of digital output lines [23:20].<br>0b00 := low-side<br>0b01 := high-side<br>0b10 := Hi-Z<br>0b11 := reserved | R/W    | 2           |
| 7:2   | -           | Reserved                                                                                                                                                                   | R      | 0           |
| 1:0   | DOUT_CFG_16 | Digital Output Configuration 16<br>Configures side-switching of digital output lines [19:16].<br>0b00 := low-side<br>0b01 := high-side<br>0b10 := Hi-Z<br>0b11 := reserved | R/W    | 2           |

Table 5-7 : Output Configuration Register 1

## 5.3.4 Output Fault Status Register

Refer to Chapter Functional Procedures for additional information.

| Bit | Symbol      | Description                                                                                                                                                                          | Access | Reset Value |
|-----|-------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------|
| 31  | DOUT_FLT_31 | Output Fault Status [x]<br>Refer to Output Fault Status [0] for description                                                                                                          | R/W1C  | 0           |
| 30  | DOUT_FLT_30 |                                                                                                                                                                                      | R/W1C  | 0           |
| 29  | DOUT_FLT_29 |                                                                                                                                                                                      | R/W1C  | 0           |
| 28  | DOUT_FLT_28 |                                                                                                                                                                                      | R/W1C  | 0           |
| 27  | DOUT_FLT_27 |                                                                                                                                                                                      | R/W1C  | 0           |
| 26  | DOUT_FLT_26 |                                                                                                                                                                                      | R/W1C  | 0           |
| 25  | DOUT_FLT_25 |                                                                                                                                                                                      | R/W1C  | 0           |
| 24  | DOUT_FLT_24 |                                                                                                                                                                                      | R/W1C  | 0           |
| 23  | DOUT_FLT_23 |                                                                                                                                                                                      | R/W1C  | 0           |
| 22  | DOUT_FLT_22 |                                                                                                                                                                                      | R/W1C  | 0           |
| 21  | DOUT_FLT_21 |                                                                                                                                                                                      | R/W1C  | 0           |
| 20  | DOUT_FLT_20 |                                                                                                                                                                                      | R/W1C  | 0           |
| 19  | DOUT_FLT_19 |                                                                                                                                                                                      | R/W1C  | 0           |
| 18  | DOUT_FLT_18 |                                                                                                                                                                                      | R/W1C  | 0           |
| 17  | DOUT_FLT_17 |                                                                                                                                                                                      | R/W1C  | 0           |
| 16  | DOUT_FLT_16 |                                                                                                                                                                                      | R/W1C  | 0           |
| 15  | DOUT_FLT_15 |                                                                                                                                                                                      | R/W1C  | 0           |
| 14  | DOUT_FLT_14 |                                                                                                                                                                                      | R/W1C  | 0           |
| 13  | DOUT_FLT_13 |                                                                                                                                                                                      | R/W1C  | 0           |
| 12  | DOUT_FLT_12 |                                                                                                                                                                                      | R/W1C  | 0           |
| 11  | DOUT_FLT_11 |                                                                                                                                                                                      | R/W1C  | 0           |
| 10  | DOUT_FLT_10 |                                                                                                                                                                                      | R/W1C  | 0           |
| 9   | DOUT_FLT_09 |                                                                                                                                                                                      | R/W1C  | 0           |
| 8   | DOUT_FLT_08 |                                                                                                                                                                                      | R/W1C  | 0           |
| 7   | DOUT_FLT_07 |                                                                                                                                                                                      | R/W1C  | 0           |
| 6   | DOUT_FLT_06 |                                                                                                                                                                                      | R/W1C  | 0           |
| 5   | DOUT_FLT_05 |                                                                                                                                                                                      | R/W1C  | 0           |
| 4   | DOUT_FLT_04 |                                                                                                                                                                                      | R/W1C  | 0           |
| 3   | DOUT_FLT_03 |                                                                                                                                                                                      | R/W1C  | 0           |
| 2   | DOUT_FLT_02 |                                                                                                                                                                                      | R/W1C  | 0           |
| 1   | DOUT_FLT_01 |                                                                                                                                                                                      | R/W1C  | 0           |
| 0   | DOUT_FLT_00 | Output Fault Status [0]<br>Indicates the current fault status of the output line<br>0b0 := normal operation<br>0b1 := fault detected<br>See chapter Fault Detection for more details | R/W1C  | 0           |

Table 5-8 : Output Fault Status Register

There is only one single fault status per output group (4 output lines). Hence, the bit DOUT\_FLT\_[x] indicates the current fault status of its own group. However, in case of a fault condition, only the affected output line will be turned off by its driver and not the whole group, as the output drivers work independently from each other.

### 5.3.5 Output Control Register

| Bit  | Symbol          | Description                                                                                          | Access | Reset Value |
|------|-----------------|------------------------------------------------------------------------------------------------------|--------|-------------|
| 31:5 | -               | Reserved                                                                                             | R      | 0           |
| 4    | WDOG_EN         | Watchdog Enable<br>Controls the watchdog timeout functionality.<br>0b0 := disabled<br>0b1 := enabled | R/W    | 0           |
| 3:1  | -               | Reserved                                                                                             | R      | 0           |
| 0    | FLT_STAT_INT_EN | Output Fault Status Interrupt Enable<br>0b0 := disabled<br>0b1 := enabled                            | R/W    | 0           |

Table 5-9 : Output Control Register

### 5.3.6 Watchdog Time Register

Refer to Chapter Functional Procedures for additional information.

| Bit   | Symbol   | Description                                                                                                                                                                                                                                                                                       | Access | Reset Value |
|-------|----------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------|
| 31:24 | -        | Reserved                                                                                                                                                                                                                                                                                          | R      | 0           |
| 23:8  | WDOG_TMR | Watchdog Timeout Value<br>Sets the maximum time between two (Read/Write) accesses.<br><br>$WDOG_{TMR} = T_{WDTO}(ms) - 1$<br><br>The default timeout is set to 120 ms.<br><br><i>Timing is based on PCIe clocking and may be affected by spread spectrum variations (up to +0.5%) if present.</i> | R/W    | 0x77        |
| 7:0   | -        | Reserved                                                                                                                                                                                                                                                                                          | R      | 0           |

Table 5-10 : Watchdog Time Register

## 5.3.7 Watchdog Output Safe-State Register

Refer to Chapter Functional Procedures for additional information.

| Bit | Symbol      | Description                                                                                                                                                                                                                                                                                                                                                                                                                                   | Access | Reset Value |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
|-----|-------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------|--|--|--|--|-----------|----------|------|----------|-----|-----|-----|-----|---|-----|-----|-----|-----|---|-----|---|
| 31  | WDOG_OSS_31 | Watchdog Output Safe-State [x]<br>Refer to Watchdog Output Safe-State 0 for description                                                                                                                                                                                                                                                                                                                                                       | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 30  | WDOG_OSS_30 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 29  | WDOG_OSS_29 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 28  | WDOG_OSS_28 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 27  | WDOG_OSS_27 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 26  | WDOG_OSS_26 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 25  | WDOG_OSS_25 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 24  | WDOG_OSS_24 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 23  | WDOG_OSS_23 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 22  | WDOG_OSS_22 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 21  | WDOG_OSS_21 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 20  | WDOG_OSS_20 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 19  | WDOG_OSS_19 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 18  | WDOG_OSS_18 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 17  | WDOG_OSS_17 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 16  | WDOG_OSS_16 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 15  | WDOG_OSS_15 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 14  | WDOG_OSS_14 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 13  | WDOG_OSS_13 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 12  | WDOG_OSS_12 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 11  | WDOG_OSS_11 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 10  | WDOG_OSS_10 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 9   | WDOG_OSS_09 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 8   | WDOG_OSS_08 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 7   | WDOG_OSS_07 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 6   | WDOG_OSS_06 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 5   | WDOG_OSS_05 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 4   | WDOG_OSS_04 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 3   | WDOG_OSS_03 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 2   | WDOG_OSS_02 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 1   | WDOG_OSS_01 |                                                                                                                                                                                                                                                                                                                                                                                                                                               | R/W    | 0           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 0   | WDOG_OSS_00 | Watchdog Output Safe-State 0<br>Sets the safe-state of the output line in case of a watchdog event. <table border="1"> <thead> <tr> <th></th><th colspan="4">Mode</th></tr> <tr> <th></th><th>High-Side</th><th>Low-Side</th><th>Hi-Z</th><th>Reserved</th></tr> </thead> <tbody> <tr> <td>0b0</td><td>OFF</td><td>OFF</td><td>OFF</td><td>-</td></tr> <tr> <td>0b1</td><td>VCC</td><td>GND</td><td>OFF</td><td>-</td></tr> </tbody> </table> |        | Mode        |  |  |  |  | High-Side | Low-Side | Hi-Z | Reserved | 0b0 | OFF | OFF | OFF | - | 0b1 | VCC | GND | OFF | - | R/W | 0 |
|     | Mode        |                                                                                                                                                                                                                                                                                                                                                                                                                                               |        |             |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
|     | High-Side   | Low-Side                                                                                                                                                                                                                                                                                                                                                                                                                                      | Hi-Z   | Reserved    |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 0b0 | OFF         | OFF                                                                                                                                                                                                                                                                                                                                                                                                                                           | OFF    | -           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |
| 0b1 | VCC         | GND                                                                                                                                                                                                                                                                                                                                                                                                                                           | OFF    | -           |  |  |  |  |           |          |      |          |     |     |     |     |   |     |     |     |     |   |     |   |

Table 5-11 : Watchdog Output Safe-State Register

### 5.3.8 Watchdog Status Register

Refer to Chapter Functional Procedures for additional information.

| Bit  | Symbol    | Description                                                                                                                                                                  | Access | Reset Value |
|------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|-------------|
| 31:5 | -         | Reserved                                                                                                                                                                     | R      | 0           |
| 4    | WDOG_STAT | Watchdog Status<br>Indicates the current watchdog status.<br>0b0 := normal operation<br>0b1 := asserted<br>All outputs switch to safe states until the assertion is cleared. | R/W1C  | 0           |
| 3:0  | -         | Reserved                                                                                                                                                                     | R      | 0           |

Table 5-12 : Watchdog Status Register

### 5.3.9 Interrupt Control Register

| Bit  | Symbol       | Description                                                                                                                 | Access | Reset Value |
|------|--------------|-----------------------------------------------------------------------------------------------------------------------------|--------|-------------|
| 31   | INT_ACK_MODE | Interrupt Acknowledge Mode<br>0b0 := Interrupts are cleared by write (R/W1C)<br>0b1 := Interrupts are cleared by read (R)   | R/W    | 0           |
| 30:1 | -            | Reserved                                                                                                                    | R      | 0           |
| 0    | GINT_EN      | Global Interrupt Enable<br>Master interrupt controls (masks) PCIe interrupt generation<br>0b0 := disabled<br>0b1 := enabled | R/W    | 0           |

Table 5-13 : Interrupt Control Register

### 5.3.10 Interrupt Status Register

| Bit  | Symbol       | Description                                                                                                        | Access | Reset Value |
|------|--------------|--------------------------------------------------------------------------------------------------------------------|--------|-------------|
| 31:1 | -            | Reserved                                                                                                           | R      | 0           |
| 0    | FLT_INT_STAT | Or-Wired Fault Status Interrupt<br>Indicates that one or more of the output fault status events have been detected | R/W1C  | 0           |

Table 5-14 : Interrupt Status Register

## 6 Interrupts

### 6.1 Interrupt Sources

#### **Output Fault Status Interrupt:**

The TQMC604 is capable of generating an interrupt in case of an output fault condition (DOUT\_FLT\_[x] is set in the Output Fault Status Register).

### 6.2 Interrupt Handling

#### **Output Fault Status Interrupt:**

The single output fault status (DOUT\_FLT\_[x]) have been or-wired to generate a single interrupt request.

The single fault interrupt status (FLT\_INT\_STAT) has been integrated into the Interrupt Status Register. The bit can always be read and when set, cleared by high-active writing (R/W1C).

Interrupt clearing method is configurable (INT\_ACK\_MODE). Default is Clear-by-Write, Clear-on-Read is supported.

If the output fault status interrupt (FLT\_STAT\_INT\_EN) is enabled in the Output Control Register and a fault condition occurs (DOUT\_FLT\_[x] - Output Fault Status Register - is switching to asserted), the corresponding bit is set within the interrupt status register.

Disabling an already set (registered) interrupt will clear the event.

#### **Global Interrupt Control/Status:**

Internal interrupt requests are controlled (masked) by a global interrupt enable (GINT\_EN).

If not enabled, host interrupts are suppressed. Deactivating a pending host interrupt does not clear any already set (registered) interrupt events nor prevents capturing those.

When the fault status interrupt and the global interrupt enable are set, an active interrupt will be indicated.

## 7 Input Interface Description

### 7.1 Galvanic Isolation

The TQMC604 has 32 digital outputs. All outputs are isolated through digital isolators from the system and are also isolated against each other in groups of eight outputs.

| Group | Supply | Ground | Output                                                                       |
|-------|--------|--------|------------------------------------------------------------------------------|
| O0    | VS_0   | GND_0  | OUT 0<br>OUT 1<br>OUT 2<br>OUT 3<br>OUT 4<br>OUT 5<br>OUT 6<br>OUT 7         |
| O1    | VS_1   | GND_1  | OUT 8<br>OUT 9<br>OUT 10<br>OUT 11<br>OUT 12<br>OUT 13<br>OUT 14<br>OUT 15   |
| O2    | VS_2   | GND_2  | OUT 16<br>OUT 17<br>OUT 18<br>OUT 19<br>OUT 20<br>OUT 21<br>OUT 22<br>OUT 23 |
| O3    | VS_3   | GND_3  | OUT 24<br>OUT 25<br>OUT 26<br>OUT 27<br>OUT 28<br>OUT 29<br>OUT 30<br>OUT 31 |

Table 7-1 : Isolated Digital Outputs

## 7.2 Output Configuration

The output drivers on the TQMC604 work with 5 V up to 36 V supply and are capable of driving 0.15 A continuous per output. All outputs resist short-circuits and are protected against reverse polarity, thermal overload and overvoltage events up to 65 V.

The outputs can be software configured as high-side or low-side switch in groups of four.

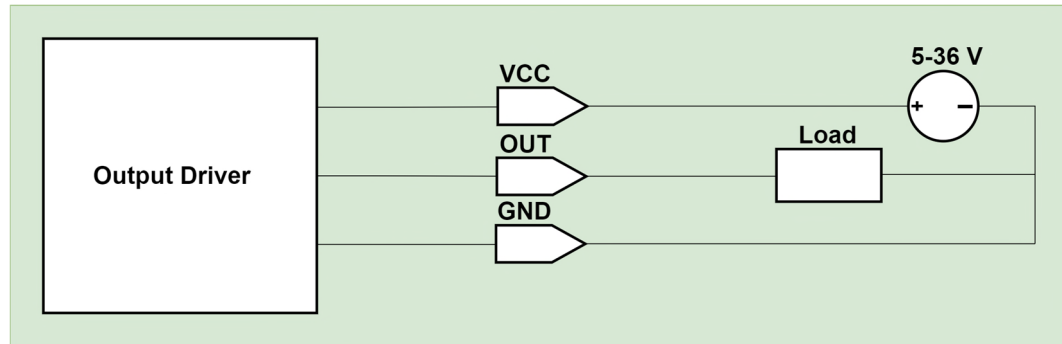


Figure 7-1 : High-Side Driver Configuration

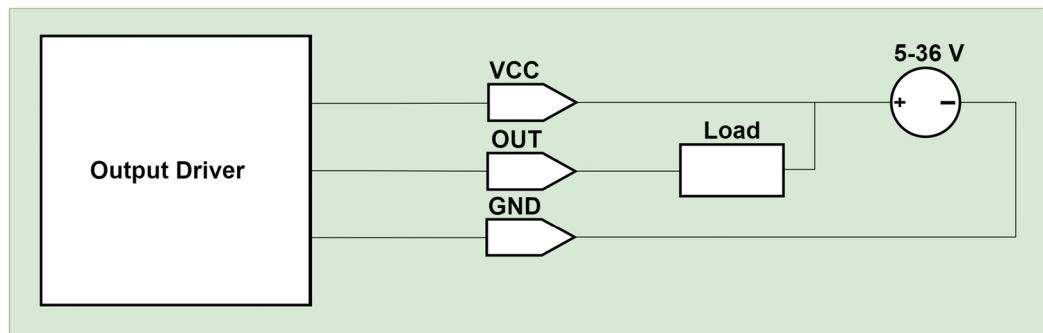


Figure 7-2 : Low-Side Driver Configuration

Writing '0' to bit DOUT\_[x] in the Digital Output Register disables the corresponding output driver and sets the output line at Hi-Z.

When disabled and in high-side configuration (DOUT\_CFG\_[x] = 0b01), the output is weakly pulled low with typical 50  $\mu$ A.

While disabled and in any other configuration (DOUT\_CFG\_[x] = 0b00), the output is weakly pulled high with typical 50  $\mu$ A.

To prevent any undesired effect, the switching configuration set in the Output Configuration Registers should match the load configuration as shown in the figures above.

## 7.3 Fault Detection

The bit DOUT\_FLT\_[x] in the Output Fault Status Register will be set to '1' if either of the following conditions has been detected by any of the group's outputs:

- Overcurrent
- Overtemperature
- Supply Voltage Drop

In case of a fault condition, the affected output(s) will automatically be turned off by the output driver(s). The affected output(s) remain disabled until the fault conditions are cleared.

**The bit DOUT\_FLT\_[x] indicates the current fault status of an output group (4 output lines). However, in case of a fault condition, only the affected output lines will be turned off and not the whole group.**

## 7.4 Output Watchdog

Writing '1' to bit 4 (WDOG\_EN) in the Output Control Register enables the hardware watchdog function. The status of the watchdog is indicated at bit 4 (WDOG\_STAT) of the Watchdog Status Register.

Any software accesses (read or write) to the Digital Output Register will retrigger the watchdog. The maximum time between two accesses is adjustable and set by the bits (WDOG\_TMR) in the Watchdog Time Register. If the time expires without a software access all outputs fall back to the set safe-state in the Watchdog Output Safe-State Register. At the same time the watchdog status will change from '0' to '1'. This prevents a write access to the Digital Output Register. The content of this register is however not affected by that.

Writing '1' to the watchdog status (bit 4 WDOG\_STAT) clears this bit and also unlocks the Digital Output Register. After unlocking the Digital Output Register the output stays in the set safe-state till the next register write access.

**The maximum time between two software accesses is set by default to 120 ms in the Watchdog Time Register. This time is based on PCIe clocking and may be slightly affected by spread spectrum variations (up to +0.5%) if present.**

## 7.5 Thermal Considerations

The power dissipated inside the output drivers on the TQMC604 is determined by the power consumption of the integrated LDO ( $P_{D_{LDO}}$ ) and also the current that flows through the driver on-resistance  $R_{ON}$  ( $P_{D_{OP}}$ ).

The integrated LDO is used to power the digital isolators, that isolates the system from the output interface.

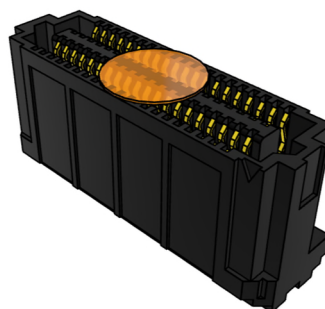
$R_{on}$  refers to the internal resistance of the output driver when it is fully conducting in the high- or low-side configuration.

The total power dissipation of the 32 output drivers could reach 7 W assuming the maximum drivers supply (36 V) and the maximum available load current (0.15 A).

As a result, the module generates noticeable heat (especially at high supply voltages and high load currents) and requires adequate forced air cooling.

## 8 I/O Connector P12

|                                |                                                          |
|--------------------------------|----------------------------------------------------------|
| <b>Pin-Count</b>               | 80 Pins                                                  |
| <b>Connector Type</b>          | 80 Position Mezzanine 0.635 mm High-Density 4-Row Socket |
| <b>Source &amp; Order Info</b> | Samtec ASP-239729-01                                     |



### 8.1.1 IOPIPE 1

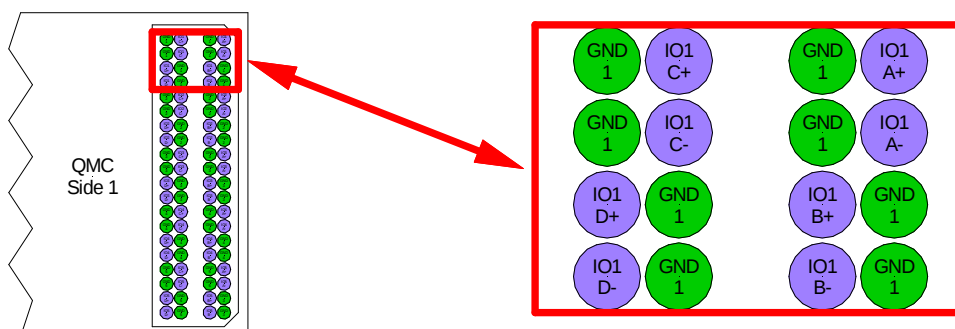


Figure 8-1 : P12 I/O Connector – IOPIPE 1

|          | Pin    | Signal                   | Description                   |
|----------|--------|--------------------------|-------------------------------|
| IOPIPE 1 | IO1_A+ | VS_0                     | Supply for Output Lines 0-7   |
|          | IO1_A- | VS_0                     | Supply for Output Lines 0-7   |
|          | IO1_B+ | VS_1                     | Supply for Output Lines 8-15  |
|          | IO1_B- | VS_1                     | Supply for Output Lines 8-15  |
|          | IO1_C+ | VS_2                     | Supply for Output Lines 16-23 |
|          | IO1_C- | VS_2                     | Supply for Output Lines 16-23 |
|          | IO1_D+ | VS_3                     | Supply for Output Lines 24-31 |
|          | IO1_D- | VS_3                     | Supply for Output Lines 24-31 |
|          | GND1   | Not connected on TQMC604 | -                             |

Table 8-1 : P12 I/O Connector Pin Assignment – IOPIPE 1

## 8.1.2 IOPIPE 2

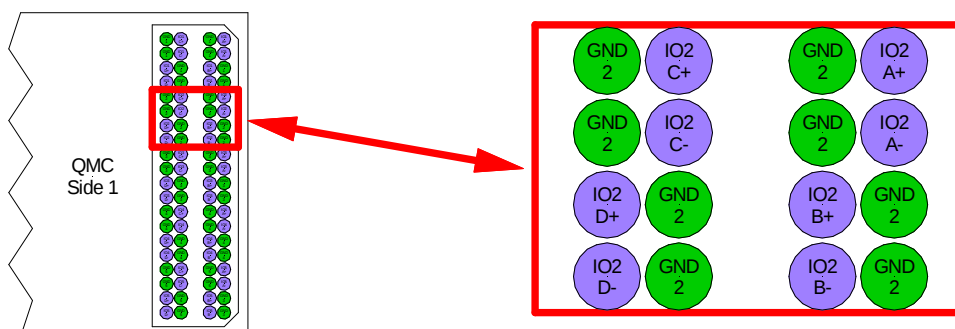


Figure 8-2 : P12 I/O Connector – IOPIPE 2

|          | Pin    | Signal                 | Description                           |
|----------|--------|------------------------|---------------------------------------|
| IOPIPE 2 | IO2_A+ | OUT 0                  | Output Line 0                         |
|          | IO2_A- | OUT 1                  | Output Line 1                         |
|          | IO2_B+ | OUT 2                  | Output Line 2                         |
|          | IO2_B- | OUT 3                  | Output Line 3                         |
|          | IO2_C+ | OUT 4                  | Output Line 4                         |
|          | IO2_C- | OUT 5                  | Output Line 5                         |
|          | IO2_D+ | OUT 6                  | Output Line 6                         |
|          | IO2_D- | OUT 7                  | Output Line 7                         |
|          | GND2   | GND for OUT 0 .. OUT 7 | Current return for Output Lines [0:7] |

Table 8-2 : P12 I/O Connector Pin Assignment – IOPIPE 2

### 8.1.3 IOPIPE 3

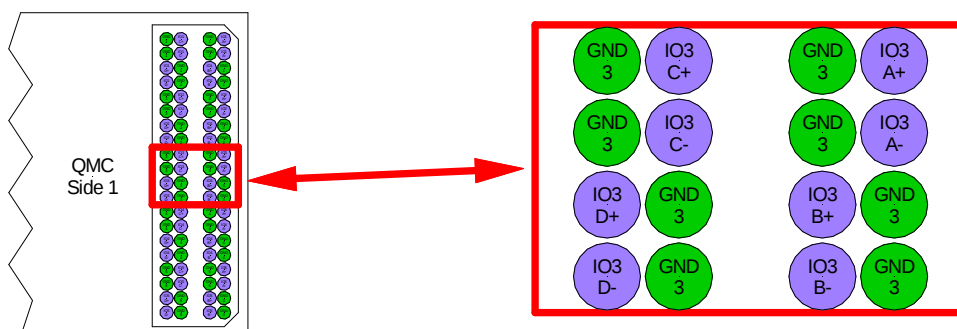


Figure 8-3 : P12 I/O Connector – IOPIPE 3

|          | Pin    | Signal                  | Description                            |
|----------|--------|-------------------------|----------------------------------------|
| IOPIPE 3 | IO3_A+ | OUT 8                   | Output Line 8                          |
|          | IO3_A- | OUT 9                   | Output Line 9                          |
|          | IO3_B+ | OUT 10                  | Output Line 10                         |
|          | IO3_B- | OUT 11                  | Output Line 11                         |
|          | IO3_C+ | OUT 12                  | Output Line 12                         |
|          | IO3_C- | OUT 13                  | Output Line 13                         |
|          | IO3_D+ | OUT 14                  | Output Line 14                         |
|          | IO3_D- | OUT 15                  | Output Line 15                         |
|          | GND3   | GND for OUT 8 .. OUT 15 | Current return for Output Lines [8:15] |

Table 8-3 : P12 I/O Connector Pin Assignment – IOPIPE 3

### 8.1.4 IOPIPE 4

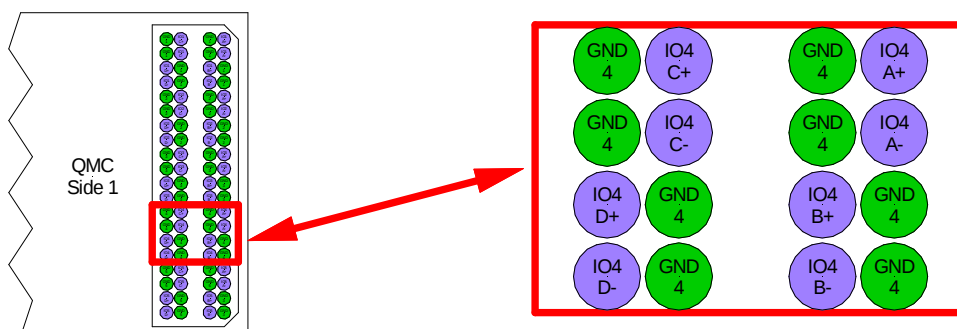


Figure 8-4 : P12 I/O Connector – IOPIPE 4

|          | Pin    | Signal                   | Description                             |
|----------|--------|--------------------------|-----------------------------------------|
| IOPIPE 4 | IO4_A+ | OUT 16                   | Output Line 16                          |
|          | IO4_A- | OUT 17                   | Output Line 17                          |
|          | IO4_B+ | OUT 18                   | Output Line 18                          |
|          | IO4_B- | OUT 19                   | Output Line 19                          |
|          | IO4_C+ | OUT 20                   | Output Line 20                          |
|          | IO4_C- | OUT 21                   | Output Line 21                          |
|          | IO4_D+ | OUT 22                   | Output Line 22                          |
|          | IO4_D- | OUT 23                   | Output Line 23                          |
|          | GND4   | GND for OUT 16 .. OUT 23 | Current return for Output Lines [16:23] |

Table 8-4 : P12 I/O Connector Pin Assignment – IOPIPE 4

### 8.1.5 IOPIPE 5

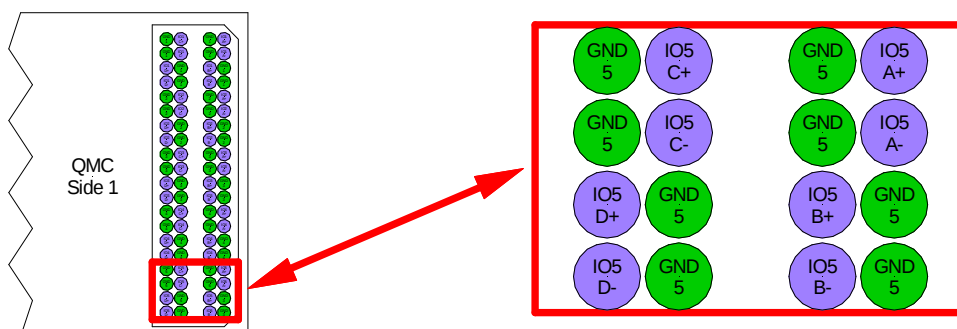


Figure 8-5 : P12 I/O Connector – IOPIPE 5

|          | Pin    | Signal                   | Description                             |
|----------|--------|--------------------------|-----------------------------------------|
| IOPIPE 5 | IO5_A+ | OUT 24                   | Output Line 24                          |
|          | IO5_A- | OUT 25                   | Output Line 25                          |
|          | IO5_B+ | OUT 26                   | Output Line 26                          |
|          | IO5_B- | OUT 27                   | Output Line 27                          |
|          | IO5_C+ | OUT 28                   | Output Line 28                          |
|          | IO5_C- | OUT 29                   | Output Line 29                          |
|          | IO5_D+ | OUT 30                   | Output Line 30                          |
|          | IO5_D- | OUT 31                   | Output Line 31                          |
|          | GND5   | GND for OUT 24 .. OUT 31 | Current return for Output Lines [24:31] |

Table 8-5 : P12 I/O Connector Pin Assignment – IOPIPE 5