The Embedded I/O Company

TEWS TECHNOLOGIES

TVME8240A

Single Board Computer

with IndustryPack® Interface

Version 2.0

User Manual

Issue 2.0.2

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TVME8240A

Single Board Computer with IndustryPack Interface

Available Board Options :

TMVE8240A-11

MPC8245 300 MHz, 64 MB SDRAM,
2 + 8 MB Flash, Fast Ethernet,
Front Panel I/O

TMVE8240A-21

MPC8245 300 MHz, 256 MB SDRAM,
2 + 32 MB Flash, Fast Ethernet,
Front Panel I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
-	Preliminary Issue for TVME8240A V2.0 Major board version change. Product ID changed to TVME820A. MPC8245 CPU, 2x 82551 Ethernet Controller, 32 KB NVRAM, VME Bus Error Interrupt, extended Boot Flash, readable switch, remote control & status, extended SDRAM and Flash options	March 2007
1.0	Status Register 2 (Readable Switch Description), Status Register 1 (Fuse Alarm Description), Control Register 2 (RS422 Mode Description. Added note) , IP Control Register (Added control bit).	July 2007
1.1	Added new board options -21, -22 (extended SDRAM and Flash Memory). Added LED output driver type note in the remote header section. Supported Flash type 39VF64xx changed to 39VF64xxB.	May 2008
2.0.2	New Notation for User Manual and Engineering Documentation. SCSI Board Options removed (former SCSI Board Options -12 and -22 set to EOL since the SCSI controller used is obsolete).	December 2008

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1 Introduction

The TVME8240A is a VME single slot Single Board Computer (SBC) using the Motorola MPC8245 Embedded PowerPC Processor.

The TVME8240A provides four single IndustryPack (IP) slots supporting single and double-sized IP modules running at 8 MHz or 32 MHz. There is a front-I/O ribbon cable connector for each IP Slot.

1.1 Features

Processor	MPC8245 Embedded PowerPC Processor (300 MHz / Timer, DMA, I2C, Interrupt Controller)
Flash Memory	2 Mbyte 8 bit wide Boot Flash (4 Mbyte max option) TVME8240A-11: 8 Mbyte 64 bit wide Application Flash TVME8240A-21: 32 Mbyte 64 bit wide Application Flash
System Memory	TVME8240A-11: 64 Mbyte 64 bit wide Synchronous DRAM (100 MHz) TVME8240A-21: 256 Mbyte 64 bit wide Synchronous DRAM (100 MHz)
LAN Interface	Intel 82551 Fast Ethernet Controller for 100Base-TX Port RJ45 front-I/O Intel 82551 Fast Ethernet Controller for 100Base-TX Port VME P2 back-I/O
IndustryPack Interface	Four single-sized / Two double-sized / Two single-sized + one double-sized Industry Pack modules supported 8 MHz / 32 MHz selectable for each IP slot Front-I/O ribbon cable connector for each IP slot
PCI Expansion Capability	IP-Span (4 additional IP slots) or PMC-Span (2 additional PMC slots) support (occupying a second VME bus slot)
NVRAM & RTC	32 Kbyte (M48T37 device)
Dual-UART + Asynchronous Serial Interface	One RS232 port on DB9 front-I/O (full modem) and VME P2 back-I/O One RS232 (4 signal) / RS422 (2 signal) port on DB9 front-I/O and VME P2 back-I/O. Software programmable
Miscellaneous	RESET switch on front panel ABORT switch on front panel Front panel status indicators Remote Header for remote LED status and switch control
Form Factor	Standard 6U VME

Figure 1-1 : Features TVME8240A

1.2 Block Diagram

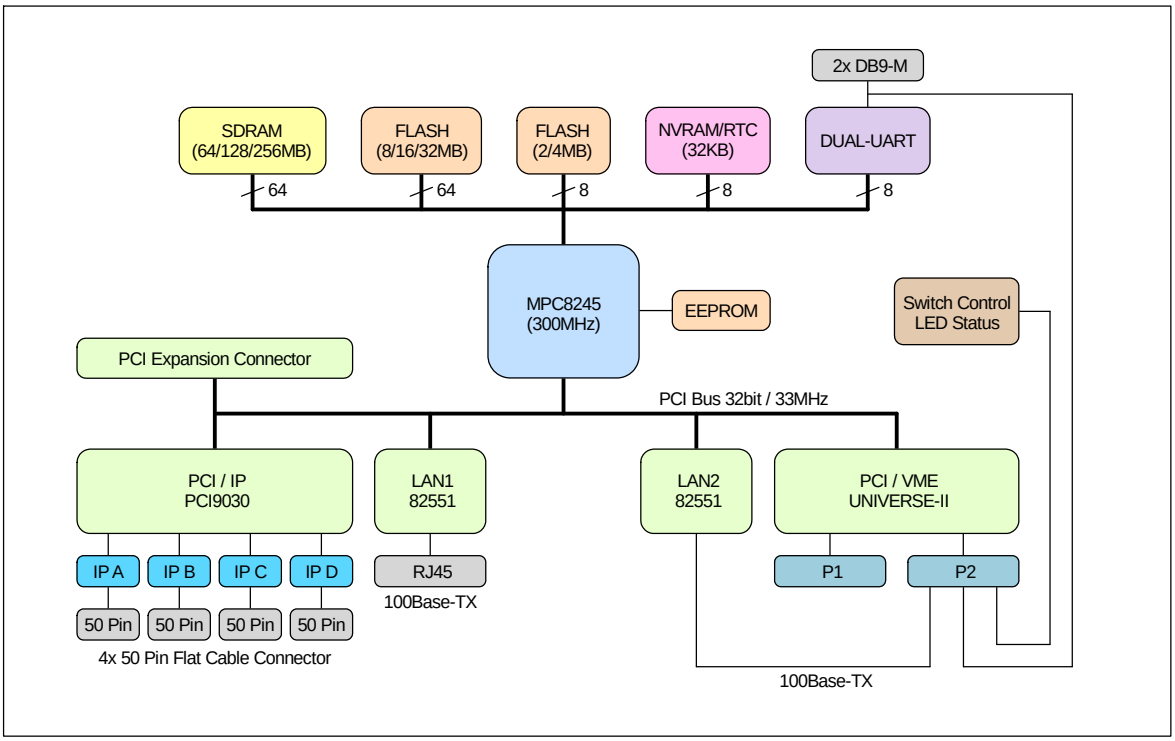


Figure 1-2 : TVME8240A Block Diagram

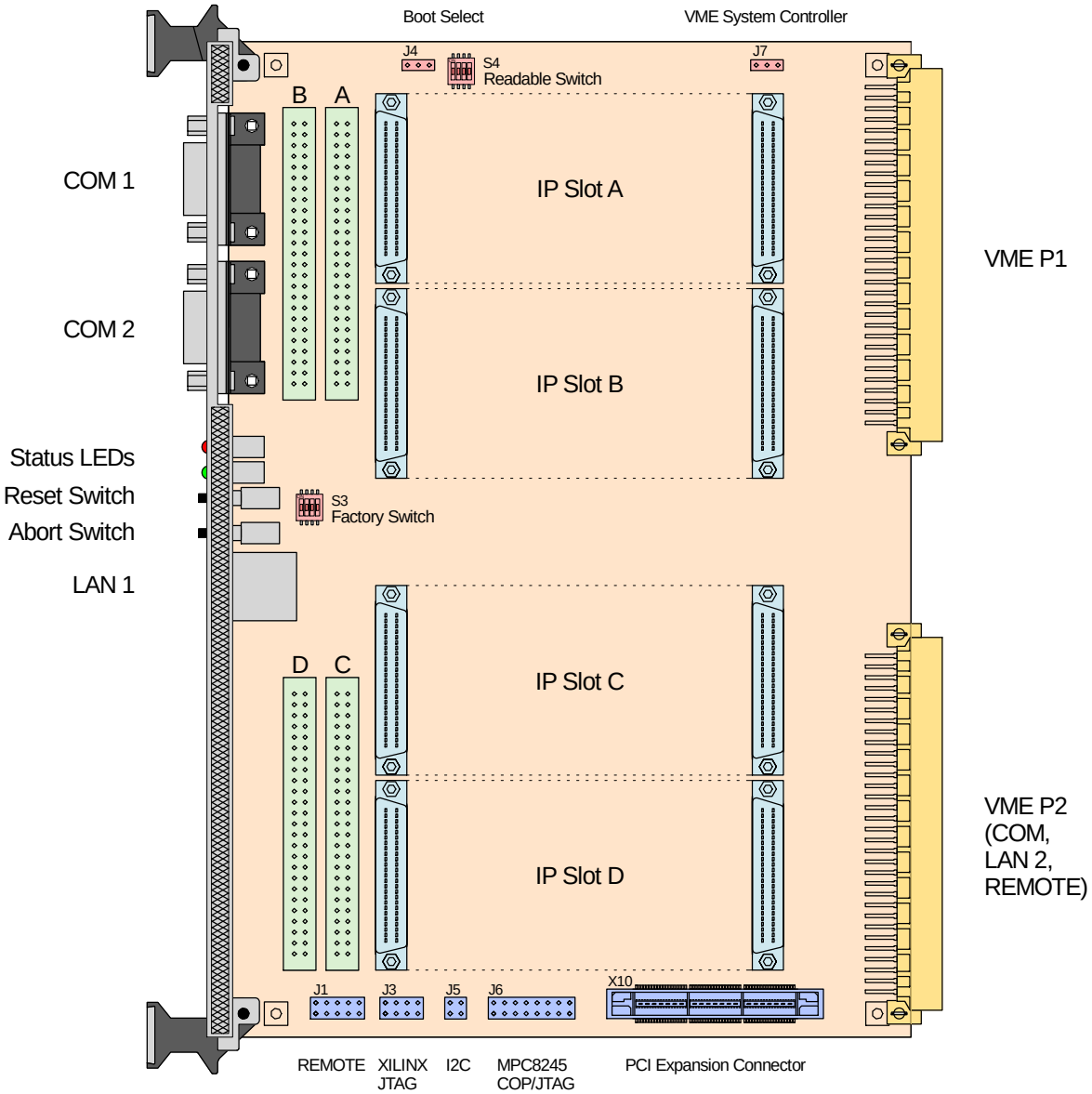


Figure 1-3 : TVME8240A Board View

2 Description

2.1 Processor

The TVME8240A uses the Motorola MPC8245 Embedded PowerPC processor.

2.2 Local Memory Bus

The TVME8240A uses the MPC8245 integrated memory controller for accessing the local memory bus devices.

The TVME8240A provides the following devices on the local memory bus:

- Application Flash Memory (64 bit wide / 8 Mbyte default, 32 Mbyte max option)
- Boot Flash Memory (8 bit wide / 2 Mbyte default, 4 Mbyte max option)
- SDRAM memory (64 bit wide / 64 Mbyte default, 256 Mbyte max option)
- NVRAM (8 bit wide, 32 Kbyte) / Real-Time Clock / Watchdog
- 16550 compatible Dual-UART (8 bit wide)
- Utility Registers (8 bit wide)

2.2.1 Flash Memory

The TVME8240A provides two banks of Flash memory:

- Bank 0 provides a 2M x 8 bit = 2 Mbyte, 8 bit wide Boot Flash Memory (base option), used for board initialization code and debug monitor.
- Bank 1 provides four x16 bit Flash devices, making a total of 8 or 32 Mbyte (depending on board option), 64 bit wide Application Flash Memory.

2.2.2 SDRAM Memory

The TVME8240A-11 provides four 8 M x 16 bit SDRAM devices, building a total of 64 Mbyte, 64 bit wide SDRAM memory.

The TVME8240A-21 provides four 32 M x 16 bit SDRAM devices, building a total of 256 Mbyte, 64 bit wide SDRAM memory.

2.2.3 NVRAM / Real-Time Clock

The TVME8240A provides an ST M48T37 compatible device to provide 32 Kbyte of non-volatile static RAM and real-time clock.

The M48T37 device consists of two parts:

- A 44-pin SO device which implements the Real Time Clock and Watchdog functions plus 32 Kbyte SRAM and sockets for the Snaphat battery.
- A Snaphat battery that is plugged on top of the device.

Please refer to the M48T37 manual for details.

2.2.4 16550 compatible Dual UART

The TVME8240A provides the Exar XR16C2850 16550 compatible Dual-UART with a 1.8432 MHz clock-oscillator source and two asynchronous serial ports.

Please refer to the XR16C2850 manual for details.

2.2.5 Utility Registers

The TVME8240A provides some additional registers for board control and status functions.

Please refer to the address map section of this manual for details.

2.3 PCI Bus

The TVME8240A implements a 32 bit, 33 MHz PCI bus.

The TVME8240A provides the following devices on the PCI bus:

- MPC8245 (PowerPC CPU, Local Memory Controller, Local PCI Bridge, PCI Arbiter, System Clock Generation, Interrupt Controller)
- Universe-II (VME/PCI Bridge)
- 82551 (10/100Base-TX Ethernet LAN Controller) [RJ45 front-I/O]
- 82551 (10/100Base-TX Ethernet LAN Controller) [VME P2 back-I/O]
- PCI9030 (PCI Local Target Chip) (IndustryPack Interface)
- Optional PCI Devices on PCI Expansion Connector (e.g. TEWS TECHNOLOGIES' TVME230 IP-Span or Motorola PMC-Span-002)

Please see the PCI Bus Summary Section for more details.

2.4 VME Bus Interface

The TVME8240A features the Universe-II VME / PCI Bridge (Tundra).

The Universe-II VME/PCI Bridge provides a 32 bit address / 32 bit data VME interface.

Please refer to the Universe-II manuals for details.

2.5 LAN Interface

The TVME8240A provides two 82551 10/100Base-TX Fast Ethernet LAN Controller (Intel).

One 82551 Fast Ethernet Controller is used for the 10/100Base-TX Ethernet interface available on an 8P RJ45 connector at the front panel.

The second 82551 Fast Ethernet Controller is used for the 10/100Base-TX Ethernet interface available at the VME P2 connector.

Please refer to the 82551 manual for details.

2.6 IP Bus Interface

The TVME8240A features the PCI9030 PCI Target Chip (PLX Technologies) for addressing the IndustryPack Interface on the PCI bus. A Xilinx FPGA is used for implementing the IndustryPack interface logic.

Four single-sized IP slots (A–D) are provided. Double-sized IP modules (8/16bit) are supported on combined IP slots A/B or C/D. The clock rate for each IP slot is programmable (8 MHz or 32 MHz).

Please refer to the IP interface section for details.

2.7 PCI Expansion Interface

The TVME8240A features a 114-pin PCI expansion connector for using existing PCI Expansion Boards with VME form factor (e.g. TEWS TECHNOLOGIES' TVME230 IP-Span or Motorola PMC-Span 002).

2.8 Asynchronous Serial Interface

The TVME8240A provides two asynchronous serial interface ports controlled by the on board Dual-UART.

Port 1 is a RS232 port, available on a DB9 connector at the front panel (full modem) and on the VME P2 connector (no RI and DSR signals on VME P2).

Port 2 is a software programmable RS232 / RS422 port, available on a DB9 connector at the front panel and on the VME P2 connector. The RS232 port is a 4 signal interface (RX, TX, RTS, CTS), the RS422 port is a 2 differential signal interface (RX+, RX-, TX+, TX-).

2.9 Interrupt Controller

The TVME8240A uses the MPC8245 integrated Programmable Interrupt Controller (PIC) in the serial mode.

Please see the MPC8245 section for details.

2.10 Status Indicators

The TVME8240A provides four status indicators visible at the front panel. The four status indicators are also available on the 10-pin Remote Header and on the VME P2 connector.

Function	Label	Color	Description
VME Bus System Controller	SYS	Green	Indicates if the TVME8240A is the VME Bus System Controller
Board Activity	ACT	Green	Indicates Local Memory Bus or PCI Bus activity
Board Failure	FAIL	Red	Software controlled failure indication
Active Fuse	FUSE	Red	Indicates triggered fuses for IP Interface power supply

Figure 2-1 : Status Indicators

All status indicators are ON during a board reset.

2.11 Reset Switch

The TVME8240A provides a momentary Reset switch (RST) accessible at the front panel.

The Reset switch can be used to generate a board hardware reset.

The Reset switch function can also be controlled via Remote Header or VME P2 connector pins.

2.12 Abort Switch

The TVME8240A provides a momentary Abort switch accessible on the front panel.

The Abort switch can be used to generate a CPU interrupt.

The Abort switch function can also be controlled via Remote Header or VME P2 connector pins.

2.13 Remote Header

The TVME8240A features a 10-pin Remote Header providing Reset and Abort switch control inputs plus status indicator outputs. These signals are also available on the VME P2 connector.

Please see the Board I/O section for details.

3 Address Maps

The TVME8240A uses the MPC8245 address map B in host mode.

The following address maps reflect MPC8245 configuration register settings done by board initialization software.

3.1 Address Map - Processor View

Processor Address		Size (Byte)	Description
Start	End		
0x0000_0000	TOP_DRAM	DRAM_SIZE	SDRAM Memory (64 bit wide) 64 Mbyte: TOP_DRAM = 0x03FF_FFFF 256 Mbyte: TOP_DRAM = 0x0FFF_FFFF
TOP_DRAM + 1	0x3FFF_FFFF	1 G – DRAM_SIZE	Reserved
0x4000_0000	0x6FFF_FFFF	1 G – 256 M	Reserved
0x7000_0000	TOP_FLASH	FLASH_SIZE	Application Flash (64 bit wide) 8 Mbyte: TOP_FLASH = 0x707F_FFFF 32 Mbyte: TOP_FLASH = 0x71FF_FFFF
TOP_ FLASH + 1	0x7FFF_FFFF	256 M – FLASH_SIZE	Reserved
0x8000_0000	0xFCEF_FFFF	2 G – 49 M	PCI MEM Space
0xFCF0_0000	0xFCFF_FFFF	1 M	MPC8245 EUMB
0xFD00_0000	0xFDFF_FFFF	16 M	PCI MEM Space (0-based)
0xFE00_0000	0xFE00_FFFF	64 K	PCI I/O Space (0-based)
0xFE01_0000	0xFE7F_FFFF	8 M – 64 K	Reserved
0xFE80_0000	0xFEBF_FFFF	4 M	PCI I/O Space (0-based)
0xFEC0_0000	0xFEDF_FFFF	2 M	Configuration Address Register
0xFEE0_0000	0xFEEF_FFFF	1 M	Configuration Data Register
0xFEF0_0000	0xFEFF_FFFF	1 M	PCI Interrupt Acknowledge
0xFF00_0000	0xFF7F_FFFF	8 M	Application Flash (lower 8 Mbyte) (64 bit wide)
0xFF80_0000	0xFFBF_FFFF	4 M	Peripheral Devices (8 bit wide)
0xFFC0_0000	0xFFDF_FFFF	2 M	Reserved for Boot Flash Extension
0xFFE0_0000	0xFFFF_FFFF	2 M	Boot Flash (8 bit wide)

Figure 3-1 : Address Map – Processor View

Device	Read	Write
SDRAM	All	All
Application Flash	All	64 bit Only
Peripheral Devices	8 bit Only	8 bit Only
Boot Flash	All	8 bit Only

Figure 3-2 : Supported Transfer Sizes

Processor Address		Translated PCI Address		PCI Space
Start	End	Start	End	
0x8000_0000	0xFCEF_FFFF	0x8000_0000	0xFCEF_FFFF	MEM
0xFD00_0000	0xFDFF_FFFF	0x0000_0000	0x00FF_FFFF	MEM
0xFE00_0000	0xFE00_FFFF	0x0000_0000	0x0000_FFFF	I/O
0xFE80_0000	0xFEBF_FFFF	0x0000_0080	0x00BF_FFFF	I/O

Figure 3-3 : PCI Address Translation

3.2 Address Map – PCI Memory Master View

PCI Memory Address		Size (Byte)	Description
Start	End		
0x0000_0000	TOP_DRAM	DRAM_SIZE	SDRAM Memory (64 bit wide) 64 Mbyte : TOP_DRAM = 0x03FF_FFFF 256 Mbyte: TOP_DRAM = 0x0FFF_FFFF
TOP_DRAM + 1	0x3FFF_FFFF	1 G – DRAM_SIZE	Reserved
0x4000_0000	0x6FFF_FFFF	1 G – 256 M	Reserved
0x7000_0000	TOP_FLASH	FLASH_SIZE	Application Flash (64 bit wide) 8 Mbyte: TOP_FLASH = 0x007F_FFFF 32 Mbyte: TOP_FLASH = 0x71FF_FFFF
TOP_ FLASH + 1	0x7FFF_FFFF	256 M – FLASH_SIZE	Reserved
0x8000_0000	0xFCEF_FFFF	2 G – 49 M	PCI Memory Space
0xFCF0_0000	0xFCF0_0FFF	4 K	PCI accessible MPC8245 EUMB
0xFCF0_1000	0xFCFF_FFFF	1 M – 4 K	Reserved
0xFD00_0000	0xFDFF_FFFF	16 M	SDRAM Memory (0-Based)
0xFE00_0000	0xFEFF_FFFF	16 M	Reserved
0xFF00_0000	0xFF7F_FFFF	8 M	Application Flash (lower 8 Mbyte) (64 bit wide)
0xFF80_0000	0xFFBF_FFFF	4 M	Peripheral Devices (8 bit wide)

0xFFC0_0000	0xFFDF_FFFF	2 M	Boot Flash Extension (option)
0xFFE0_0000	0xFFFF_FFFF	2 M	Boot Flash (8 bit wide)

Figure 3-4 : Address Map – PCI Memory Master View

On the TVME8240A the MPC8245 responds as a target to PCI Memory cycles for accessing SDRAM, PCI accessible MPC8245 EUMB, Application Flash, Peripheral Devices and Boot Flash.

3.3 Address Map – PCI I/O Master View

PCI I/O Address		Size (Byte)	Description
Start	End		
0x0000_0000	0x0000_FFFF	64 K	PCI I/O Space
0x0001_0000	0x007F_FFFF	8 M – 64 K	Reserved
0x0080_0000	0x00BF_FFFF	4 M	PCI I/O Space
0x00C0_0000	0xFFFF_FFFF	4 G – 12 M	Reserved

Figure 3-5 : Address Map – PCI I/O Master View

The MPC8245 does not responding as a target to PCI I/O cycles.

3.4 Address Map – Peripheral Devices Detail

Address		Size (Byte)	Description
Start	End		
0xFF80_0000	0xFF80_7FFF	32 K	NVRAM / RTC
0xFF80_8000	0xFF8F_FFFF	1 M – 32 K	Reserved
0xFF90_0000	0xFF90_0007	8	UTILITY REG
0xFF90_0008	0xFF9F_FFFF	1 M – 8	Reserved
0xFFA0_0000	0xFFA0_0007	8	UART CH 1
0xFFA0_0008	0xFFAF_FFFF	1M – 8	Reserved
0xFFB0_0000	0xFFB0_0007	8	UART CH 2
0xFFB0_0008	0xFFBF_FFFF	1 M – 8	Reserved

Figure 3-6 : Address Map – Peripheral Devices Detail

For read or write accesses to the Peripheral Devices 8 bit (byte) transfer sizes must be used.

For the NVRAM / RTC register map please refer to the M48T37 device documentation.

For the UART register map please refer to the XR16C2850 documentation.

3.5 Address Map – Utility Register Detail

Address	Size (Byte)	Register Name
0xFF90_0000	1	CONTROL
0xFF90_0001	1	STATUS
0xFF90_0002	1	CONTROL 2
0xFF90_0003	1	STATUS 2
0xFF90_0004	1	FPGA_FLASH_PROG

Figure 3-7 : Address Map – Utility Register Detail

3.5.1 Control Register (0xFF90_0000)

Bit	Name	Access	Reset	Function
7 (MSB)	BOARD_RST	R/W	0	0: Normal Board Operation 1: Assert Board Reset
6	I2C_EEP_WE	R/W	0	0: I2C EEPROM Writes Disabled 1: I2C EEPROM Writes Enabled
5	APP_FLASH_WE	R/W	0	0: Application Flash Writes Disabled 1: Application Flash Writes Enabled
4	BOOT_FLASH_WE	R/W	0	0: Boot Flash Writes Disabled 1: Boot Flash Writes Enabled
3	APP_FLASH_RST	R/W	0	0: Do Not Reset Application Flash 1: Reset Application Flash (Does only apply for Spansion™ Flash Types)
2	BOOT_FLASH_RST	R/W	0	0: Do Not Reset Boot Flash 1: Reset Boot Flash (Does only apply for Spansion™ Flash Types)
1	VBERR_INT_EN	R/W	0	0: Disable VME Bus Error Interrupt 1: Enable VME Bus Error Interrupt
0 (LSB)	FUSE_INT_EN	R/W	0	0: Disable Fuse Interrupt 1: Enable Fuse Interrupt

Figure 3-8 : Control Register

A board reset is also performed at power-up.

A board reset will perform a general board hardware reset, re-configuration of the IP FPGA, PCI reset and CPU reset.

If the TVME8240A is the VME bus system controller, a board reset will also trigger a VME bus system reset.

3.5.2 Status Register (0xFF90_0001)

Bit	Name	Access	Reset	Function
7 (MSB)	BOOT_JMP	R	-	0: Run Bug Monitor 1: Run Flash Application
6	PCI_EXP_PRSNT	R	-	0: PCI Expansion Board Not Present 1: PCI Expansion Board Present
5	ABORT_SW	R	-	0: Abort Switch Not Active 1: Abort Switch Active
4	FPGA_DONE	R	-	0: IP FPGA Configuration Not Done 1: IP FPGA Configuration Done
3	APP_FLASH_BSY	R	-	0: Application Flash Is Not Busy 1: Application Flash Is Busy (Does only apply for Spansion™ Flash Types)
2	BOOT_FLASH_BSY	R	-	0: Boot Flash Is Not Busy 1: Boot Flash Is Busy (Does only apply for Spansion™ Flash Types)
1	VME_BERR	R/C	-	Reads: 0: No VME Bus Error Event 1: VME Bus Error Event occurred Writes: Write as '1' to clear VME Bus Error Status and/or to clear VME Bus Error Interrupt Status. This status bit is capable of generating an interrupt if enabled in the Control Register.
0 (LSB)	FUSE_ALRM	R/C	-	Reads: 0: All on board Fuses OK 1: At least one on board Fuse has triggered Writes: Write as '1' to clear Fuse Alarm Status and/or to clear Fuse Alarm Interrupt. Clearing has no effect if any Fuse is still triggered. This status bit is capable of generating an interrupt if enabled in the Control Register.

Figure 3-9 : Status Register

Board initialization software should verify successful IP FPGA configuration.

3.5.3 Control Register 2 (0xFF90_0002)

Bit	Name	Access	Reset	Function
7 (MSB)	FAIL_LED	R/W	0	0: Set Fail LED OFF 1: Set Fail LED ON
6	COM2_RS422	R/W	0	0: COM2 RS232 Mode 1: COM2 RS422 Mode (see note below)
5	Reserved	-	-	Write as '0' Undefined for Reads
4	Reserved	-	-	Write as '0' Undefined for Reads
3	Reserved	-	-	Write as '0' Undefined for Reads
2	Reserved	-	-	Write as '0' Undefined for Reads
1	Reserved	-	-	Write as '0' Undefined for Reads
0 (LSB)	Reserved	-	-	Write as '0'. Undefined for Reads

Figure 3-10: Control Register 2

For RS422 Mode on Serial Channel 2 the UART MCR[1] bit (0xFFB0_0004) must be clear.

3.5.4 Status Register 2 (0xFF90_0003)

Bit	Name	Access	Reset	Function
7 (MSB)	SW_1	R	-	0: Readable Switch Pos. 1 is OFF 1: Readable Switch Pos. 1 is ON
6	SW_2	R	-	0: Readable Switch Pos. 2 is OFF 1: Readable Switch Pos. 2 is ON
5	SW_3	R	-	0: Readable Switch Pos. 3 is OFF 1: Readable Switch Pos. 3 is ON
4	SW_4	R	-	0: Readable Switch Pos. 4 is OFF 1: Readable Switch Pos. 4 is ON
3	PROG_MODE	R	-	0: Normal Operating Mode 1: Programming/Test Mode
2	Reserved	-	-	Write as '0' Undefined for Reads
1	Reserved	-	-	Write as '0' Undefined for Reads
0 (LSB)	Reserved	-	-	Write as '0'. Undefined for Reads

Figure 3-11: Status Register 2

3.5.5 FPGA Flash Programming Register (0xFF90_0004)

Bit	Name	Access	Reset	Function
7 (MSB)	TCK_OUT	R/W	0	0: Set TCK signal low 1: Set TCK signal high
6	TMS_OUT	R/W	1	0: Set TMS signal low 1: Set TMS signal high
5	TDI_OUT	R/W	0	0: Set TDI signal low 1: Set TDI signal high
4	TDO_IN	R	-	0: TDO signal is low 1: TDO signal is high
3	Reserved	-	-	Write as '0' Undefined for Reads
2	Reserved	-	-	Write as '0' Undefined for Reads
1	Reserved	-	-	Write as '0' Undefined for Reads
0 (LSB)	Reserved	-	-	Write as '0'. Undefined for Reads

Figure 3-12: FPGA Flash Programming Register

This register should only be used in case of an IP FPGA logic update. It should not be used during normal operation.

4 MPC8245

The TVME8240A uses the MPC8245 in host mode with address map B in extended addressing mode.

The MPC8245 processor and peripheral logic are configured to operate in big endian mode.

4.1 MPC8245 Configuration Register

Setting up the MPC8245 Configuration Registers is scope of the board initialization software.

4.1.1 Configuration Register Access

The MPC8245 Configuration Registers are accessed in two steps:

1. A 32 bit register address 0x8000_00nn is written to the CONFIG_ADDR port at 0xFEC0_0000, where nn is the (word-aligned) register offset.

2. Data is accessed at the CONFIG_DATA port at 0xFEE0_000m, where m is the offset within the word-aligned address (depending on transfer size).

Data can be accessed multiple times at the CONFIG_DATA port until the CONFIG_ADDR port value is changed.

All of the MPC8245 Configuration Registers are intrinsically little endian. Therefore all of the following Configuration Register settings are shown in little endian order.

Since on the TVME8240A the MPC8245 processor and peripheral logic operates in big endian mode, software must either use byte reversed load / store instructions or byte-swap the values for the CONFIG_ADDR and CONFIG_DATA port access.

E.g. for reading the Device ID Register (offset 0x02) one should write 0x0000_0080 (0x00 is the word-aligned offset for 0x02) to 0xFEC0_0000 and read the half-word 0x0600 at 0xFEE0_0002.

E.g. for setting the Output Driver Control Register (offset 0x73) one should write 0x7000_0080 (0x70 is the word-aligned offset for 0x73) to 0xFEC0_0000 and write the register byte value to 0xFEE0_0003.

E.g. for setting the EUMBBAR Register (offset 0x78) to 0xFCF0_0000 one should write 0x78000080 to 0xFEC0_0000 and write the word 0x0000F0FC to 0xFEE0_0000.

4.1.2 Configuration Register Settings

Register Offset	Register Description	Size (Byte)	Access Type	Setting
0x00	Vendor ID	2	R	0x1057
0x02	Device ID	2	R	0x0006
0x04	PCI Command Register	2	R/W	0x0106
0x06	PCI Status Register	2	R/C	*status*
0x08	Revision ID	1	R	*revision*
0x09	Standard Programming Interface	1	R	0x00
0x0A	Subclass Code	1	R	0x00
0x0B	Class Code	1	R	0x06
0x0C	Cache Line Size	1	R/W	*reset_default*
0x0D	Latency Timer	1	R/W	*reset_default*
0x0E	Header Type	1	R	0x00
0x0F	BIST Control	1	R	0x00
0x10	Local Memory Base Address Register 0	4	R/W	*reset_default*
0x14	Peripheral Control Status Register Base Address Register	4	R/W	*reset_default*
0x18	Local Memory Base Address Register 1	4	R/W	*reset_default*
0x2C	Subsystem Vendor ID	2	R/W	0x0000
0x2E	Subsystem ID	2	R/W	0x0000
0x30	Expansion ROM Base Address	4	R	0x0000_0000
0x3C	Interrupt Line	1	R/W	*reset_default*
0x3D	Interrupt Pin	1	R	0x01
0x3E	MIN GNT	1	R	0x00
0x3F	MAX LAT	1	R	0x00
0x40	Bus Number	1	R/W	*reset_default*
0x41	Subordinate Bus Number	1	R/W	*reset_default*
0x44	PCI General Control Register	2	R/W	0x0000
0x46	PCI Arbiter Control Register	2	R/W	0x8400
0x70	Power Management Configuration Register 1	2	R/W	0xC001
0x72	Power Management Configuration Register 2	1	R/W	0x20
0x73	Output Driver Control Register	1	R/W	0xDD
0x74	Clock Driver Control Register	2	R/W	0x0000
0x76	Misc. I/O Control Register 1	1	R/W	0x00
0x77	Misc. I/O Control Register 2	1	R/W	0x20

Register Offset	Register Description	Size (Byte)	Access Type	Setting
0x78	Embedded Utilities Memory Block Base Address (EUMBBAR)	4	R/W	0xFCF0_0000
0x80, 0x84	Memory Starting Address Registers	4	R/W	0x0000_0000, 0x0000_0000
0x88, 0x8C	Extended Memory Starting Address Registers	4	R/W	0x0101_0100, 0x0101_0101
0x90, 0x94	Memory Ending Address Registers	4	R/W	64 Mbyte Opt. : 0xFFFF_FF3F, 0xFFFF_FFFF 128 Mbyte Opt. : 0xFFFF_FF7F, 0xFFFF_FFFF 256 Mbyte Opt. : 0xFFFF_FFFF, 0xFFFF_FFFF
0x98, 0x9C	Extended Memory Ending Address Registers	4	R/W	0x0101_0100, 0x0101_0101
0xA0	Memory Bank Enable Register	1	R/W	0x01
0xA3	Page Mode Register	1	R/W	0x00
0xA8	Processor Interface Configuration Register 1	4	R/W	0x0014_1B98
0xAC	Processor Interface Configuration Register 2	4	R/W	0x2000_0000
0xB8	ECC Single Bit Error Counter Register	1	R/W	*status*
0xB9	ECC Single Bit Error Trigger Register	1	R/W	*reset_default*
0xC0	Error Enabling Register 1	1	R/W	*reset_default*
0xC1	Error Detection Register 1	1	R/C	*status*
0xC3	Processor Internal Bus Error Status Register	1	R/C	*status*
0xC4	Error Enabling Register 2	1	R/W	*reset_default*
0xC5	Error Detection Register 2	1	R/C	*status*
0xC7	PCI Bus Error Status Register	1	R/C	*status*
0xC8	Processor/PCI Error Address Register	4	R	*status*
0xD0	Extended ROM Configuration Register 1	4	R/W	0x35FF_8000
0xD4	Extended ROM Configuration Register 2	4	R/W	0xB5FF_8000
0xD8	Extended ROM Configuration Register 3	4	R/W	*reset_default*
0xDC	Extended ROM Configuration Register 4	4	R/W	8 Mbyte Opt.: 0x0000_000B 16 Mbyte Opt.: 0x0000_000C 32 Mbyte Opt.: 0x0000_000D

Register Offset	Register Description	Size (Byte)	Access Type	Setting
0xE0	Address Map B Options Register (AMBOR)	1	R/W	0xC0
0xE1	PCI/Memory Buffer Configuration Register	1	R/W	0x00
0xE2	PLL Configuration Register	1	R	*reset_default*
0xE3	DLL Tap Count Register	1	R	*reset_default*
0xF0	Memory Control Configuration Register 1 (MCCR1)	4	R/W	64 Mbyte Opt. : 0x15E8_0000 128/256 Mbyte Opt. : 0x15E8_0002
0xF4	Memory Control Configuration Register 2 (MCCR2)	4	R/W	64 Mbyte Opt. : 0x5220_1800 128/256 Mbyte Opt. : 0x5220_0BC0
0xF8	Memory Control Configuration Register 3 (MCCR3)	4	R/W	0x0700_0000
0xFC	Memory Control Configuration Register 4 (MCCR4)	4	R/W	0x2530_2220

Figure 4-1 : MPC8245 Configuration Register Settings

Board initialization software notes:

The MEMGO bit in the MCCR1 register (offset 0xF0) must not be set until all other memory configuration parameters have been appropriately configured.

The DLL_RESET bit in the AMBOR register (offset 0xE0) must be explicitly set and then cleared by software during initialization.

4.2 MPC8245 Interrupt Controller

The TVME8240A uses the MPC8245 PIC in serial mode as the board interrupt controller.

The following table shows the available interrupt sources and the serial interrupt mapping.

Serial Interrupt No.	Edge / Level	Polarity	Interrupt Source
0	Level	Low	PLD Interrupt (VME Bus Error, Fuse Alarm)
1	Edge	Low	ABORT Switch
2	Level	Low	82551 (LAN 1) (front-I/O)
3	Level	Low	Reserved
4	Level	Low	PCI9030 (IP Interface)
5	Level	Low	Universe-II LINT0
6	Level	Low	Universe-II LINT1
7	Level	Low	Universe-II LINT2
8	Level	Low	Universe-II LINT3
9	Level	Low	PCI Expansion INTA
10	Level	Low	PCI Expansion INTB
11	Level	Low	PCI Expansion INTC
12	Level	Low	PCI Expansion INTD
13	Level	Low	M48T37 (Real-Time Clock / Watchdog)
14	Level	Low	82551 (LAN 2) (back-I/O)
15	Level	Low	16C2850 (Dual-UART)

Figure 4-2 : PIC Serial Interrupt Assignment

4.2.1 PIC Register Access

The PIC Registers are part of the MPC8245 Embedded Utility Memory Block (EUMB).

The EUMB base address is set in the EUMBBAR Register.

On the TVME8240A the EUMB base address is set to 0xFCF0_0000.

4.2.2 PIC Register Settings

4.2.2.1 Global Configuration Register (GCR)

Offset from EUMBBAR: 0x4_1020

The mode bit in the GCR must be set for PIC mixed mode operation.

4.2.2.2 PIC Interrupt Configuration Register (EICR)

Offset from EUMBBAR: 0x4_1030

The EICR clock ratio field should be set to 0x2 for optimized interrupt performance.

The EICR SIE bit must be set to enable Serial Interrupt Mode.

4.2.2.3 Serial Interrupt Vector / Priority Registers (SVPR)

The polarity and sense bits in the SVPRs must be configured accordingly to the PIC Serial Interrupt Assignment table.

Please refer to chapter “Interrupt Controller” for the PIC serial interrupt assignment.

4.2.2.4 PIC Register Programming

The PIC Programming Guidelines from the MPC8245 manual should be followed.

4.3 I2C EEPROM

The TVME8240A provides an on board I2C EEPROM for board specific data.

EEPROM Offset	Description	Content
0x00	Check sum	see note below
0x01	Number Of Valid Bytes Following	e.g. 0x06
0x02	Board Type (High Byte)	0x2030 for TVME8240A
0x03	Board Type (Low Byte)	
0x04	Board Option (High Byte)	e.g. 0x000B for TVME8240A-11
0x05	Board Option (Low Byte)	
0x06	Board Version (Major)	V <major>.<minor> e.g. 0x0200 = V2.0
0x07	Board Version (Minor)	
0x08 ... 0x0F	Factory Reserved	
0x10 ... 0xFF	Reserved	

Figure 4-3 : I2C EEPROM Content

The address of the on board I2C EEPROM is 0b000.

Writes to the on board I2C EEPROM must be enabled in the Utility Control Register.

The check sum is the 2's-complement of the lower byte of the sum of all used locations of the I2C EEPROM, except the check sum byte.

5 Flash Programming

5.1 Boot Flash Memory

Boot Flash Overview		
Size	2/4 Mbyte (option)	
Address Range	2 Mbyte	0xFFE0_0000 - 0xFFFF_FFFF
	4 Mbyte	0xFFC0_0000 - 0xFFFF_FFFF
Port Width	8 bit	
Purpose	Board Initialization Code, Debug Monitor, Factory Reserved	
System Reset Vector	0xFFF0_0100	

Figure 5-1 : Boot Flash Overview

For writes to the Boot Flash only byte (8 bit) transfer sizes must be used.

Writes to the Boot Flash must be enabled in the Utility Control Register.

5.1.1 SST 39VF168x Flash Types

5.1.1.1 Supported SST Boot Flash Types

SST Flash Type	Size	Address Range	Sector Organization	Device ID
39VF1681	2 Mbyte	0xFFE0_0000 - 0xFFFF_FFFF	512 Uniform Sectors (4 Kbyte each) or 32 Uniform Blocks (64 Kbyte each)	0xC8
39VF1682				0xC9

Note: The SST Manufacturer ID for the SST Boot Flash is 0xBF. Manufacturer ID and Device ID are readable using the Auto-Select command.

Figure 5-2 : Supported SST Boot Flash Types

5.1.1.2 SST Boot Flash Command Cycles

Command Sequence	Cycles	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	Base+ 0x000	0xF0										
Auto-Select	4	Base+ 0xAAA	0xAA	Base+ 0x555	0x55	Base+ 0xAAA	0x90	Base+ 0x000	MID				
								Base+ 0x001	DID				
Program	4	Base+ 0xAAA	0xAA	Base+ 0x555	0x55	Base+ 0xAAA	0xA0	PA	PD				
Chip Erase	6	Base+ 0xAAA	0xAA	Base+ 0x555	0x55	Base+ 0xAAA	0x80	Base+ 0xAAA	0xAA	Base+ 0x555	0x55	Base+ 0xAAA	0x10
Block Erase	6	Base+ 0xAAA	0xAA	Base+ 0x555	0x55	Base+ 0xAAA	0x80	Base+ 0xAAA	0xAA	Base+ 0x555	0x55	BA	0x30
Sector Erase	6	Base+ 0xAAA	0xAA	Base+ 0x555	0x55	Base+ 0xAAA	0x80	Base+ 0xAAA	0xAA	Base+ 0x555	0x55	SA	0x50

Note: All cycles shown are write cycles, except the fourth cycle of the Auto-Select command, which is a read cycle.

MID = Manufacturer ID, DID = Device ID, PA = Program Address, PD = Program Data, BA = Block Address, SA = Sector Address.

For Write Commands, after the 4th cycle, the program should poll address PA until read data = PD.

For Erase Commands, after the 6th cycle, the program should poll for read data = 0xFF at the Flash base address for Chip Erase or at the given sector/block address for Sector/Block Erase.

Figure 5-3 : SST Boot Flash Command Cycles

5.1.1.3 SST Boot Flash Sector Maps

The SST 39VF1681/1682 Flash provides 512 Uniform Sectors (4 Kbyte each) or 32 Uniform Blocks (64 Kbyte each):

Sector	Sector Size (Byte)	Sector Address Range
SA0	4 K	0xFFE0_0000 - 0xFFE0_0FFF
SA1	4 K	0xFFE0_1000 - 0xFFE0_1FFF
SA2	4 K	0xFFE0_2000 - 0xFFE0_2FFF
…	…	…
SA510	4 K	0xFFFF_E000 - 0xFFFF_EFFF
SA511	4 K	0xFFFF_F000 - 0xFFFF_FFFF

Figure 5-4 : SST39VF168x Boot Flash Sector Map

Block	Block Size (Byte)	Block Address Range
BA0	64 K	0xFFE0_0000 - 0xFFE0_FFFF
BA1	64 K	0xFFE1_0000 - 0xFFE1_FFFF
BA2	64 K	0xFFE2_0000 - 0xFFE2_FFFF
…	…	…
BA31	64 K	0xFFFE_0000 - 0xFFFE_FFFF
BA31	64 K	0xFFFF_0000 - 0xFFFF_FFFF

Figure 5-5 : SST39VF168x Boot Flash Block Map

5.1.2 Spansion 29GL0xxA Flash Types

If used as Boot Flash device, the Spansion S29GL0xxA Flash device is used in Byte-Mode.

The Spansion S29GL0xxA Flash device requires to wait 4us after the last write of a command sequence, before any status information (i.e. any data) is read from the Flash device. Otherwise the read data could indicate wrong status information.

5.1.2.1 Supported Spansion Boot Flash Types

Spansion Flash Type	Size	Address Range	Sector Organization
S29GL016A-R1	2 Mbyte	0xFFE0_0000 - 0xFFFF_FFFF	31 sectors (64 Kbyte each) plus 8 Top Boot Sectors (8 Kbyte each)
S29GL016A-R2			31 sectors (64 Kbyte each) plus 8 Bottom Boot Sectors (8 Kbyte each)
S29GL032A-R3	4 Mbyte	0xFFC0_0000 - 0xFFFF_FFFF	63 sectors (64 Kbyte each) plus 8 Top Boot Sectors (8 Kbyte each)
S29GL032A-R4			63 sectors (64 Kbyte each) plus 8 Bottom Boot Sectors (8 Kbyte each)

Figure 5-6 : Supported Spansion Boot Flash Types

5.1.2.2 Spansion Boot Flash Command Cycles

Command Sequence	Cycles	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	Base+ 0x000	0xF0										
Auto-Select	4	Base+ 0xAAA	0xAA	Base+ 0x555	0x55	Base+ 0xAAA	0x90	See below for reading Manufacturer and Device Identifier					
Write to Buffer	5 + x	Base+ 0xAAA	0xAA	Base+ 0x555	0x55	SA	0x25	SA	DC	PA	PD	WBL	PD
Program Buffer	1	SA	0x29										
Write to Buffer Abort Reset	3	Base+ 0xAAA	0xAA	Base+ 0x555	0x55	Base+ 0xAAA	0xF0						
Chip Erase	6	Base+ 0xAAA	0xAA	Base+ 0x555	0x55	Base+ 0xAAA	0x80	Base+ 0xAAA	0xAA	Base+ 0x555	0x55	Base+ 0xAAA	0x10
Sector Erase	6	Base+ 0xAAA	0xAA	Base+ 0x555	0x55	Base+ 0xAAA	0x80	Base+ 0xAAA	0xAA	Base+ 0x555	0x55	SA	0x30

Note: All cycles shown are write cycles, except the 4th, 5th & 6th cycle of the Auto-Select command, which are read cycles.
SA = Sector Address, DC = Data Count (Number of Write Buffer Locations to load minus 1),
PA = Program Address (Address must belong to the specified Sector), PD = Program Data,
WBL = Additional Write Buffer Location (Address must be within same Write Buffer Page as PA. Each Write-Buffer-Page has a 32 Byte address boundary).

Figure 5-7 : Spansion Boot Flash Command Cycles

5.1.2.3 Spansion Boot Flash Identifier

ID Read Cycle	Address	Data
All listed S29GL0xxA-Rx		
Manufacturer ID	Base + 0x000	0x01
S29GL016A-R1		
Device ID Cycle 1	Base + 0x002	0xC4
S29GL016A-R2		
Device ID Cycle 1	Base + 0x002	0x49
S29GL032A-R3		
Device ID Cycle 1	Base + 0x002	0x7E
Device ID Cycle 2	Base + 0x01C	0x1A
Device ID Cycle 3	Base + 0x01E	0x01
S29GL032A-R4		
Device ID Cycle 1	Base + 0x002	0x7E
Device ID Cycle 2	Base + 0x01C	0x1A
Device ID Cycle 3	Base + 0x01E	0x00

Note: All cycles shown are read cycles for the Auto-Select command.

Figure 5-8 : Spansion Boot Flash Identifier

5.1.2.4 Spansion Flash Write Buffer Programming

The Spansion S29GL0xxA Flash devices in x8-Mode must use Write-Buffer programming.

The first two cycles of the Write-to-Buffer command are general unlock cycles.

The 3rd cycle writes the Write-Buffer-Load command to the sector address in which the programming occurs.

The 4th cycle writes the number of data units to write (e.g. number of Bytes to write), minus one, to the sector address in which the programming occurs.

The 5th cycle writes the first address / data pair to the write buffer. The actual write buffer page is selected by the 32 Byte address boundary used. **Write buffer programming must not cross write buffer page or Flash sector boundaries.**

Once the specified number of write buffer locations is loaded, the Program Buffer command must be used.

Data Polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ5 and DQ1 should be monitored to determine the device status during write buffer programming.

Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

5.1.2.5 Spansion Flash Flowcharts

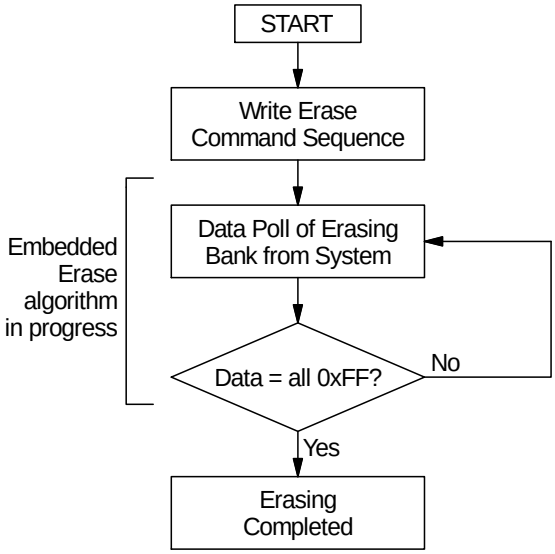
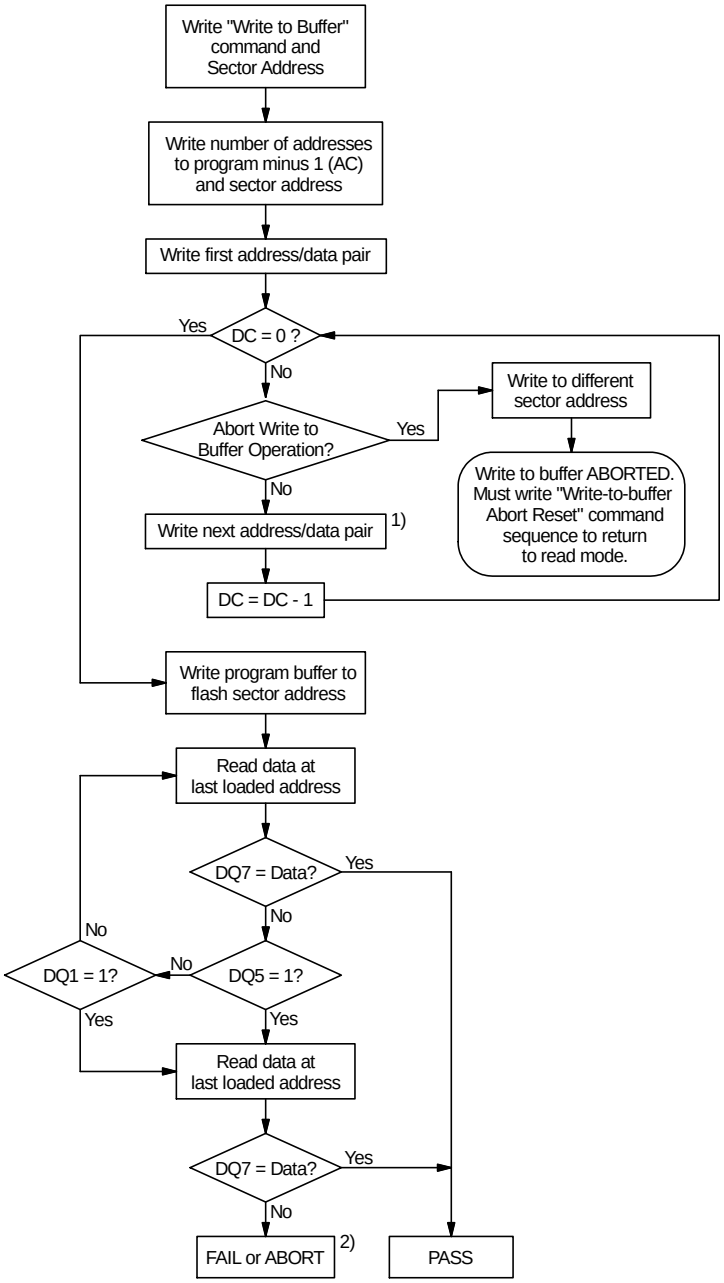


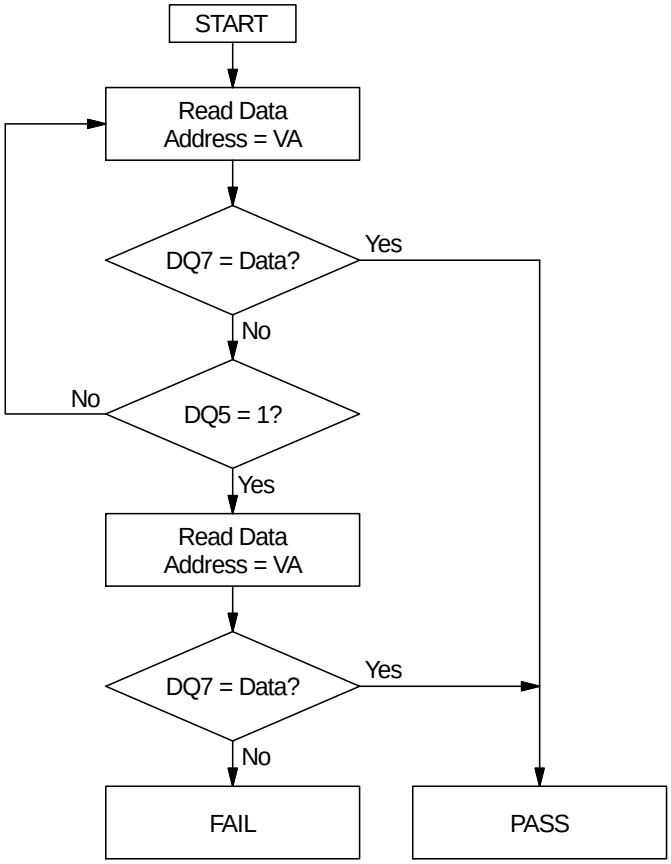
Figure 5-9 : Spansion Flash Erase Operation



1) When Sector Address is specified, any address in the selected sector is acceptable. However, when loading Write-Buffer address locations with data, all addresses must fall within the selected Write-Buffer Page.

2) If this flowchart location was reached because of DQ5 = 1, then the device FAILED. If this flowchart location was reached because of DQ1 = 1, then the Write-to-Buffer operation was ABORTED. In either case, the proper reset command must be written before the device can begin any next operation. If DQ1 = 1, write the Write-Buffer-Programming-Abort-Reset command. If DQ5 = 1, write the Reset command.

Figure 5-10 : Spansion Flash Write Buffer Programming



VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.

Figure 5-11 : Spansion Flash Data Polling

5.1.2.6 Spansion Boot Flash Sector Maps

The **Spansion S29GL016A-R1** Flash provides 31 sectors (64 Kbyte each) plus 8 Top Boot Sectors (8 Kbyte each):

Sector	Sector Size (Byte)	Sector Address Range
SA0	64K	0xFFE0_0000 - 0xFFE0_FFFF
SA1	64K	0xFFE1_0000 - 0xFFE1_FFFF
SA2	64K	0xFFE2_0000 - 0xFFE2_FFFF
…	…	…
SA28	64K	0xFFFC_0000 - 0xFFFC_FFFF
SA29	64K	0xFFFD_0000 - 0xFFFD_FFFF
SA30	64K	0xFFFE_0000 - 0xFFFE_FFFF
SA31	8K	0xFFFF_0000 - 0xFFFF_1FFF
SA32	8K	0xFFFF_2000 - 0xFFFF_3FFF
SA33	8K	0xFFFF_4000 - 0xFFFF_5FFF
SA34	8K	0xFFFF_6000 - 0xFFFF_7FFF
SA35	8K	0xFFFF_8000 - 0xFFFF_9FFF
SA36	8K	0xFFFF_A000 - 0xFFFF_BFFF
SA37	8K	0xFFFF_C000 - 0xFFFF_DFFF
SA38	8K	0xFFFF_E000 - 0xFFFF_FFFF

Figure 5-12 : S29GL016A-R1 Boot Flash Sector Map

The **Spansion S29GL016A-R2** Flash provides 31 sectors (64 Kbyte each) plus 8 Bottom Boot Sectors (8 Kbyte each):

Sector	Sector Size (Byte)	Sector Address Range
SA0	8K	0xFFE0_0000 - 0xFFE0_1FFF
SA1	8K	0xFFE0_2000 - 0xFFE0_3FFF
SA2	8K	0xFFE0_4000 - 0xFFE0_5FFF
SA3	8K	0xFFE0_6000 - 0xFFE0_7FFF
SA4	8K	0xFFE0_8000 - 0xFFE0_9FFF
SA5	8K	0xFFE0_A000 - 0xFFE0_BFFF
SA6	8K	0xFFE0_C000 - 0xFFE0_DFFF
SA7	8K	0xFFE0_E000 - 0xFFE0_FFFF
SA8	64K	0xFFE1_0000 - 0xFFE1_FFFF
SA9	64K	0xFFE2_0000 - 0xFFE2_FFFF
SA10	64K	0xFFE3_0000 - 0xFFE3_FFFF
…	…	…

SA36	64K	0xFFFD_0000 - 0xFFFD_FFFF
SA37	64K	0xFFFE_0000 - 0xFFFE_FFFF
SA38	64K	0xFFFF_0000 - 0xFFFF_FFFF

Figure 5-13 : S29GL016A-R2 Boot Flash Sector Map

The **Spansion S29GL032A-R3** Flash provides 63 sectors (64 Kbyte each) plus 8 Top Boot Sectors (8 Kbyte each):

Sector	Sector Size (Byte)	Sector Address Range
SA0	64K	0xFFC0_0000 - 0xFFC0_FFFF
SA1	64K	0xFFC1_0000 - 0xFFC1_FFFF
SA2	64K	0xFFC2_0000 - 0xFFC2_FFFF
…	…	…
SA60	64K	0xFFFC_0000 - 0xFFFC_FFFF
SA61	64K	0xFFFD_0000 - 0xFFFD_FFFF
SA62	64K	0xFFFE_0000 - 0xFFFE_FFFF
SA63	8K	0xFFFF_0000 - 0xFFFF_1FFF
SA64	8K	0xFFFF_2000 - 0xFFFF_3FFF
SA65	8K	0xFFFF_4000 - 0xFFFF_5FFF
SA66	8K	0xFFFF_6000 - 0xFFFF_7FFF
SA67	8K	0xFFFF_8000 - 0xFFFF_9FFF
SA68	8K	0xFFFF_A000 - 0xFFFF_BFFF
SA69	8K	0xFFFF_C000 - 0xFFFF_DFFF
SA70	8K	0xFFFF_E000 - 0xFFFF_FFFF

Figure 5-14 : S29GL032A-R3 Boot Flash Sector Map

The Spansion **S29GL032A-R4** Flash provides 63 sectors (64 Kbyte each) plus 8 Bottom Boot Sectors (8 Kbyte each):

Sector	Sector Size (Byte)	Sector Address Range
SA0	8K	0xFFC0_0000 - 0xFFC0_1FFF
SA1	8K	0xFFC0_2000 - 0xFFC0_3FFF
SA2	8K	0xFFC0_4000 - 0xFFC0_5FFF
SA3	8K	0xFFC0_6000 - 0xFFC0_7FFF
SA4	8K	0xFFC0_8000 - 0xFFC0_9FFF
SA5	8K	0xFFC0_A000 - 0xFFC0_BFFF
SA6	8K	0xFFC0_C000 - 0xFFC0_DFFF
SA7	8K	0xFFC0_E000 - 0xFFC0_FFFF
SA8	64K	0xFFC1_0000 - 0xFFC1_FFFF

SA9	64K	0xFFC2_0000 - 0xFFC2_FFFF
SA10	64K	0xFFC3_0000 - 0xFFC3_FFFF
...	...	...
SA68	64K	0xFFFD_0000 - 0xFFFD_FFFF
SA69	64K	0xFFFE_0000 - 0xFFFE_FFFF
SA70	64K	0xFFFF_0000 - 0xFFFF_FFFF

Figure 5-15 : S29GL032A-R4 Boot Flash Sector Map

5.2 Application Flash Memory

Application Flash Overview		
Total Size	8/16/32 Mbyte (option)	
Address Range	8 Mbyte	0x7000_0000 - 0x707F_FFFF
	16 Mbyte	0x7000_0000 - 0x70FF_FFFF
	32 Mbyte	0x7000_0000 - 0x71FF_FFFF
Organization	4 Devices, each 1/2/4 M x 16 bit (option)	
Port Width	64 bit	
Purpose	User Application	

Figure 5-16 : Application Flash Overview

For writes to the Application Flash double-word (64 bit) transfer sizes must be used.

Writes to the Application Flash must be enabled in the Utility Control Register.

5.2.1 SST 39VFxxxx Flash Types

5.2.1.1 Supported SST Application Flash Types

SST Flash Type	Size	Address Range	Sector Organization	Device ID
4 x 39VF1601	4 x 2 Mbyte	0x7000_0000 - 0x707F_FFFF	512 Uniform Sectors (4 x 4 Kbyte each) or 32 Uniform Blocks (4 x 64 Kbyte each)	0x234B_234B_234B_234B
4 x 39VF1602				0x234A_234A_234A_234A
4 x 39VF3201	4 x 4 Mbyte	0x7000_0000 - 0x70FF_FFFF	1024 Uniform Sectors (4 x 4 Kbyte each) or 64 Uniform Blocks (4 x 64 Kbyte each)	0x235B_235B_235B_235B
4 x 39VF3202				0x235A_235A_235A_235A
4 x 39VF6401B	4 x 8 Mbyte	0x7000_0000 - 0x71FF_FFFF	2048 Uniform Sectors (4 x 4 Kbyte each) or 128 Uniform Blocks (4 x 64 Kbyte each)	0x236D_236D_236D_236D
4 x 39VF6402B				0x236C_236C_236C_236C

Note:
The 64 bit Application Flash Bank is build by using four parallel x16 Flash devices.
The SST Manufacturer ID read for the Application Flash is 0x00BF_00BF_00BF_00BF.
Manufacturer ID and Device ID are readable using the Auto-Select command.

Figure 5-17 : Supported SST Application Flash Types

5.2.1.2 SST 39VF16xx/39VF32xx Application Flash Command Cycles

Command Sequence	Cycles	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	Base + 0x0_0000	0x00F0_00F0 _00F0_00F0										
Auto Select	4	Base + 0x2_AAA8	0x00AA_00AA _00AA_00AA	Base + 0x1_5550	0x0055_0055 _0055_0055	Base + 0x2_AAA8	0x0090_0090 _0090_0090	Base + 0x0	MID				
								Base + 0x8	DID				
Write	4	Base + 0x2_AAA8	0x00AA_00AA _00AA_00AA	Base + 0x1_5550	0x0055_0055 _0055_0055	Base + 0x2_AAA8	0x00A0_00A0 _00A0_00A0	PA	PD				
Chip Erase	6	Base + 0x2_AAA8	0x00AA_00AA _00AA_00AA	Base + 0x1_5550	0x0055_0055 _0055_0055	Base + 0x2_AAA8	0x0080_0080 _0080_0080	Base + 0x2_AAA8	0x00AA_00AA _00AA_00AA	Base + 0x1_5550	0x0055_0055 _0055_0055	Base + 0x2_AAA8	0x0010_0010 _0010_0010
Block Erase	6	Base + 0x2_AAA8	0x00AA_00AA _00AA_00AA	Base + 0x1_5550	0x0055_0055 _0055_0055	Base + 0x2_AAA8	0x0080_0080 _0080_0080	Base + 0x2_AAA8	0x00AA_00AA _00AA_00AA	Base + 0x1_5550	0x0055_0055 0055_0055	BA	0x0050_0050 _0050_0050
Sector Erase	6	Base + 0x2_AAA8	0x00AA_00AA _00AA_00AA	Base + 0x1_5550	0x0055_0055 _0055_0055	Base + 0x2_AAA8	0x0080_0080 _0080_0080	Base + 0x2_AAA8	0x00AA_00AA _00AA_00AA	Base + 0x1_5550	0x0055_0055 0055_0055	SA	0x0030_0030 _0030_0030

Note:

All cycles shown are write cycles except the fourth cycle of the Auto-Select command, which is a read cycle.

MID = Manufacturer ID, DID = Device ID, PA = Program Address, PD = Program Data, BA = Block Address, SA = Sector Address.

For Write Commands, after the 4th cycle, the program should poll address PA until read data = PD.

For Erase Commands, after the 6th cycle, the program should poll for read data = 0xFFFF_FFFF_FFFF_FFFF at the Flash base address for Chip Erase or at the given sector/block address for Sector/Block Erase.

Figure 5-18 : SST 39VF16xx/39VF32xx Application Flash Command Cycles

5.2.1.3 SST 39VF64xxB Application Flash Command Cycles

Command Sequence	Cycles	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	Base + 0x0_0000	0x00F0_00F0_00F0_00F0										
Auto Select	4	Base + 0x2_AAA8	0x00AA_00AA_00AA_00AA	Base + 0x1_5550	0x0055_0055_0055_0055	Base + 0x2_AAA8	0x0090_0090_0090_0090	Base + 0x0	MID				
								Base + 0x8	DID				
Write	4	Base + 0x2_AAA8	0x00AA_00AA_00AA_00AA	Base + 0x1_5550	0x0055_0055_0055_0055	Base + 0x2_AAA8	0x00A0_00A0_00A0_00A0	PA	PD				
Chip Erase	6	Base + 0x2_AAA8	0x00AA_00AA_00AA_00AA	Base + 0x1_5550	0x0055_0055_0055_0055	Base + 0x2_AAA8	0x0080_0080_0080_0080	Base + 0x2_AAA8	0x00AA_00AA_00AA_00AA	Base + 0x1_5550	0x0055_0055_0055_0055	Base + 0x2_AAA8	0x0010_0010_0010_0010
Block Erase	6	Base + 0x2_AAA8	0x00AA_00AA_00AA_00AA	Base + 0x1_5550	0x0055_0055_0055_0055	Base + 0x2_AAA8	0x0080_0080_0080_0080	Base + 0x2_AAA8	0x00AA_00AA_00AA_00AA	Base + 0x1_5550	0x0055_0055_0055_0055	BA	0x0030_0030_0030_0030
Sector Erase	6	Base + 0x2_AAA8	0x00AA_00AA_00AA_00AA	Base + 0x1_5550	0x0055_0055_0055_0055	Base + 0x2_AAA8	0x0080_0080_0080_0080	Base + 0x2_AAA8	0x00AA_00AA_00AA_00AA	Base + 0x1_5550	0x0055_0055_0055_0055	SA	0x0050_0050_0050_0050

Note:

All cycles shown are write cycles except the fourth cycle of the Auto-Select command, which is a read cycle.

MID = Manufacturer ID, DID = Device ID, PA = Program Address, PD = Program Data, BA = Block Address, SA = Sector Address.

For Write Commands, after the 4th cycle, the program should poll address PA until read data = PD.

For Erase Commands, after the 6th cycle, the program should poll for read data = 0xFFFF_FFFF_FFFF_FFFF at the Flash base address for Chip Erase or at the given sector/block address for Sector/Block Erase.

Figure 5-19 : SST 39VF64xxB Application Flash Command Cycles

5.2.1.4 SST Application Flash Sector Maps

The four **SST39VF1601/1602** Flash devices provide a total of 512 sectors (16 Kbyte each) or 32 blocks (256 Kbyte each).

Sector	Sector Size (Byte)	Sector Address Range
SA0	4 x 4 K	0x7000_0000 - 0x7000_3FFF
SA1	4 x 4 K	0x7000_4000 - 0x7000_7FFF
SA2	4 x 4 K	0x7000_8000 - 0x7000_BFFF
SA3	4 x 4 K	0x7000_C000 - 0x7000_FFFF
…	…	…
SA508	4 x 4 K	0x707F_0000 - 0x707F_3FFF
SA509	4 x 4 K	0x707F_4000 - 0x707F_7FFF
SA510	4 x 4 K	0x707F_8000 - 0x707F_BFFF
SA511	4 x 4 K	0x707F_C000 - 0x707F_FFFF

Figure 5-20 : SST39VF160x Sector Map

Block	Sector Size (Byte)	Block Address Range
BA0	4 x 64 K	0x7000_0000 - 0x7003_FFFF
BA1	4 x 64 K	0x7004_0000 - 0x7007_FFFF
BA2	4 x 64 K	0x7008_0000 - 0x700B_FFFF
BA3	4 x 64 K	0x700C_0000 - 0x700F_FFFF
…	…	…
BA28	4 x 64 K	0x7070_0000 - 0x7073_FFFF
BA29	4 x 64 K	0x7074_0000 - 0x7077_FFFF
BA30	4 x 64 K	0x7078_0000 - 0x707B_FFFF
BA31	4 x 64 K	0x707C_0000 - 0x707F_FFFF

Figure 5-21 : SST39VF160x Block Map

The four **SST39VF3201/3202** Flash devices provide a total of 1024 sectors (16 Kbyte each) or 64 blocks (256 Kbyte each).

Sector	Sector Size (Byte)	Sector Address Range
SA0	4 x 4 K	0x7000_0000 - 0x7000_3FFF
SA1	4 x 4 K	0x7000_4000 - 0x7000_7FFF

SA2	4 x 4 K	0x7000_8000 - 0x7000_BFFF
SA3	4 x 4 K	0x7000_C000 - 0x7000_FFFF
…	…	…
SA1020	4 x 4 K	0x70FF_0000 - 0x70FF_3FFF
SA1021	4 x 4 K	0x70FF_4000 - 0x70FF_7FFF
SA1022	4 x 4 K	0x70FF_8000 - 0x70FF_BFFF
SA1023	4 x 4 K	0x70FF_C000 - 0x70FF_FFFF

Figure 5-22 : SST39VF320x Sector Map

Block	Sector Size (Byte)	Block Address Range
BA0	4 x 64 K	0x7000_0000 - 0x7003_FFFF
BA1	4 x 64 K	0x7004_0000 - 0x7007_FFFF
BA2	4 x 64 K	0x7008_0000 - 0x700B_FFFF
BA3	4 x 64 K	0x700C_0000 - 0x700F_FFFF
…	…	…
BA60	4 x 64 K	0x70F0_0000 - 0x70F3_FFFF
BA61	4 x 64 K	0x70F4_0000 - 0x70F7_FFFF
BA62	4 x 64 K	0x70F8_0000 - 0x70FB_FFFF
BA63	4 x 64 K	0x70FC_0000 - 0x70FF_FFFF

Figure 5-23 : SST39VF320x Block Map

The four **SST39VF6401B/6402B** Flash devices provide a total of 2048 sectors (16 Kbyte each) or 128 blocks (256 Kbyte each).

Sector	Sector Size (Byte)	Sector Address Range
SA0	4 x 4 K	0x7000_0000 - 0x7000_3FFF
SA1	4 x 4 K	0x7000_4000 - 0x7000_7FFF
SA2	4 x 4 K	0x7000_8000 - 0x7000_BFFF
SA3	4 x 4 K	0x7000_C000 - 0x7000_FFFF
…	…	…
SA2044	4 x 4 K	0x71FF_0000 - 0x71FF_3FFF
SA2045	4 x 4 K	0x71FF_4000 - 0x71FF_7FFF
SA2046	4 x 4 K	0x71FF_8000 - 0x71FF_BFFF
SA2047	4 x 4 K	0x71FF_C000 - 0x71FF_FFFF

Figure 5-24 : SST39VF640xB Sector Map

Block	Sector Size (Byte)	Block Address Range
BA0	4 x 64 K	0x7000_0000 - 0x7003_FFFF
BA1	4 x 64 K	0x7004_0000 - 0x7007_FFFF
BA2	4 x 64 K	0x7008_0000 - 0x700B_FFFF
BA3	4 x 64 K	0x700C_0000 - 0x700F_FFFF
…	…	…
BA124	4 x 64 K	0x71F0_0000 - 0x71F3_FFFF
BA125	4 x 64 K	0x71F4_0000 - 0x71F7_FFFF
BA126	4 x 64 K	0x71F8_0000 - 0x71FB_FFFF
BA127	4 x 64 K	0x71FC_0000 - 0x71FF_FFFF

Figure 5-25 : SST39VF640xB Block Map

5.2.2 Spansion 29GL0xxA Flash Types

The Spansion S29GL0xxA Flash device requires to wait 4us after the last write of a command sequence, before any status information (i.e. any data) is read from the Flash device. Otherwise the read data could indicate wrong status information.

5.2.2.1 Supported Application Flash Types

Spansion Flash Type	Size	Address Range	Sector Organization
4 x S29GL016A-R1	4 x 2 Mbyte	0x7000_0000 - 0x707F_FFFF	31 sectors (4 x 64 Kbyte each) plus 8 Top Boot Sectors (4 x 8 Kbyte each)
4 x S29GL016A-R2			31 sectors (4 x 64 Kbyte each) plus 8 Bottom Boot Sectors (4 x 8 Kbyte each)
4 x S29GL032A-R3	4 x 4 Mbyte	0x7000_0000 - 0x70FF_FFFF	63 sectors (4 x 64 Kbyte each) plus 8 Top Boot Sectors (4 x 8 Kbyte each)
4 x S29GL032A-R4			63 sectors (4 x 64 Kbyte each) plus 8 Bottom Boot Sectors (4 x 8 Kbyte each)
4 x S29GL064A-R3	4 x 8 Mbyte	0x7000_0000 - 0x71FF_FFFF	127 sectors (4 x 64 Kbyte each) plus 8 Top Boot Sectors (4 x 8 Kbyte each)
4 x S29GL064A-R4			127 sectors (4 x 64 Kbyte each) plus 8 Bottom Boot Sectors (4 x 8 Kbyte each)

Note: The 64 bit Application Flash Bank is build by using four parallel x16 Flash devices.

Figure 5-26 : Supported Spansion Application Flash Types

5.2.2.2 Spansion Application Flash Command Cycles

Command Sequence	Cycles	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Reset	1	Base + 0x0000	0x00F0_00F0_00F0_00F0										
Auto Select	4	Base + 0x2AA8	0x00AA_00AA_00AA_00AA	Base + 0x1550	0x0055_0055_0055_0055	Base + 0x2AA8	0x0090_0090_0090_0090	See below for reading Manufacturer and Device Identifier					
Program	4	Base + 0x2AA8	0x00AA_00AA_00AA_00AA	Base + 0x1550	0x0055_0055_0055_0055	Base + 0x2AA8	0x00A0_00A0_00A0_00A0	PA	PD				
Write to Buffer		Base + 0x2AA8	0x00AA_00AA_00AA_00AA	Base + 0x1550	0x0055_0055_0055_0055	SA	0x0025_0025_0025_0025	SA	DC	PA	PD	WBL	PD
Program Buffer to Flash	1	SA	0x0029_0029_0029_0029										
Chip Erase	6	Base + 0x2AA8	0x00AA_00AA_00AA_00AA	Base + 0x1550	0x0055_0055_0055_0055	Base + 0x2AA8	0x0080_0080_0080_0080	Base + 0x2AA8	0x00AA_00AA_00AA_00AA	Base + 0x1550	0x0055_0055_0055_0055	Base + 0x2AA8	0x0010_0010_0010_0010
Sector Erase	6	Base + 0x2AA8	0x00AA_00AA_00AA_00AA	Base + 0x1550	0x0055_0055_0055_0055	Base + 0x2AA8	0x0080_0080_0080_0080	Base + 0x2AA8	0x00AA_00AA_00AA_00AA	Base + 0x1550	0x0055_0055_0055_0055	SA	0x0030_0030_0030_0030

Note: All cycles shown are write cycles except the 4th, 5th & 6th cycle of the Auto-Select command, which are read cycles.
SA = Sector Address, DC = Data Count (Number of Write Buffer Locations to load minus 1),
PA = Program Address (Address must belong to the specified Sector), PD = Program Data,
WBL = Additional Write Buffer Location (Address must be within same Write Buffer Page as PA. Each Write-Buffer-Page has a 32 byte address boundary).

Figure 5-27 : Spansion Application Flash Command Cycles

5.2.2.3 Spansion Application Flash Identifier

ID Read Cycle	Address	Data
All listed S29GL0xxA-Rx		
Manufacturer ID	Base + 0x000	0x0001_0001_0001_0001
S29GL016A-R1		
Device ID Cycle 1	Base + 0x008	0x22C4_22C4_22C4_22C4
S29GL016A-R2		
Device ID Cycle 1	Base + 0x008	0x2249_2249_2249_2249
S29GL032A-R3		
Device ID Cycle 1	Base + 0x008	0x227E_227E_227E_227E
Device ID Cycle 2	Base + 0x070	0x221A_221A_221A_221A
Device ID Cycle 3	Base + 0x 078	0x2201_2201_2201_2201
S29GL032A-R4		
Device ID Cycle 1	Base + 0x008	0x227E_227E_227E_227E
Device ID Cycle 2	Base + 0x 070	0x221A_221A_221A_221A
Device ID Cycle 3	Base + 0x 078	0x2200_2200_2200_2200
S29GL064A-R3		
Device ID Cycle 1	Base + 0x008	0x227E_227E_227E_227E
Device ID Cycle 2	Base + 0x 070	0x2210_2210_2210_2210
Device ID Cycle 3	Base + 0x 078	0x2201_2201_2201_2201
S29GL064A-R4		
Device ID Cycle 1	Base + 0x008	0x227E_227E_227E_227E
Device ID Cycle 2	Base + 0x 070	0x2210_2210_2210_2210
Device ID Cycle 3	Base + 0x 078	0x2200_2200_2200_2200

Notes: All cycles shown are read cycles for the Auto-Select command.

Figure 5-28 : Spansion Application Flash Identifier

5.2.2.4 Spansion Application Flash Write Buffer Programming

The Spansion S29GL0xxA Flash devices in x16-Mode may use Write-Buffer programming or direct programming.

For Write-Buffer Programming please see the write buffer programming description in the Spansion Boot Flash section.

5.2.2.5 Spansion Application Flash Flowcharts

Basically the same flowcharts as shown in the Spansion Boot Flash section do apply.

However, since the 64 bit Application Flash bank is build by using four parallel x16 Flash devices, any check shown for DQx means that for the Application Flash four datalines must be checked.

8 bit Flash Port Status	64 bit Flash Port Status
DQ7	DQ7, DQ23, DQ39, DQ55
DQ5	DQ5, DQ21, DQ37, DQ53
DQ1	DQ1, DQ17, DQ33, DQ49

Figure 5-29 : Spansion Application Flash Status Bits

5.2.2.6 Spansion Application Flash Sector Maps

The four **Spansion S29GL016A-R1** Flash devices provide 31 sectors (4 x 64 Kbyte each) plus 8 Top Boot Sectors (4 x 8 Kbyte each):

Sector	Sector Size (Byte)	Sector Address Range
SA0	4 x 64K	0x7000_0000 - 0x7003_FFFF
SA1	4 x 64K	0x7004_0000 - 0x7007_FFFF
SA2	4 x 64K	0x7008_0000 - 0x700B_FFFF
SA3	4 x 64K	0x700C_0000 - 0x700F_FFFF
…	…	…
SA28	4 x 64K	0x7070_0000 - 0x7073_FFFF
SA29	4 x 64K	0x7074_0000 - 0x7077_FFFF
SA30	4 x 64K	0x7078_0000 - 0x707B_FFFF
SA31	4 x 8K	0x707C_0000 - 0x707C_BFFF
SA32	4 x 8K	0x707C_C000 - 0x707C_FFFF
SA33	4 x 8K	0x707D_0000 - 0x707D_BFFF
SA34	4 x 8K	0x707D_C000 - 0x707D_FFFF
SA35	4 x 8K	0x707E_0000 - 0x707E_BFFF
SA36	4 x 8K	0x707E_C000 - 0x707E_FFFF
SA37	4 x 8K	0x707F_0000 - 0x707F_BFFF
SA38	4 x 8K	0x707F_C000 - 0x707F_FFFF

Figure 5-30 : S29GL016A-R1 Application Flash Sector Map

The four **Spansion S29GL016A-R2** Flash devices provide 31 sectors (4 x 64 Kbyte each) plus 8 Bottom Boot Sectors (4 x 8 Kbyte each):

Sector	Sector Size (Byte)	Sector Address Range
SA0	4 x 8K	0x7000_0000 - 0x7000_BFFF
SA1	4 x 8K	0x7000_C000 - 0x7000_FFFF
SA2	4 x 8K	0x7001_0000 - 0x7001_BFFF
SA3	4 x 8K	0x7001_C000 - 0x7001_FFFF
SA4	4 x 8K	0x7002_0000 - 0x7002_BFFF
SA5	4 x 8K	0x7002_C000 - 0x7002_FFFF
SA6	4 x 8K	0x7003_0000 - 0x7003_BFFF
SA7	4 x 8K	0x7003_C000 - 0x7003_FFFF
SA8	4 x 64K	0x7004_0000 - 0x7007_FFFF
SA9	4 x 64K	0x7008_0000 - 0x700B_FFFF
SA10	4 x 64K	0x700C_0000 - 0x700F_FFFF
…	…	
SA35	4 x 64K	0x7070_0000 - 0x7073_FFFF
SA36	4 x 64K	0x7074_0000 - 0x7077_FFFF
SA37	4 x 64K	0x7078_0000 - 0x707B_FFFF
SA38	4 x 64K	0x707C_0000 - 0x707F_FFFF

Figure 5-31 : S29GL016A-R2 Application Flash Sector Map

The four **Spansion S29GL032A-R3** Flash devices provide 63 sectors (4 x 64 Kbyte each) plus 8 Top Boot Sectors (4 x 8 Kbyte each):

Sector	Sector Size (Byte)	Sector Address Range
SA0	4 x 64K	0x7000_0000 - 0x7003_FFFF
SA1	4 x 64K	0x7004_0000 - 0x7007_FFFF
SA2	4 x 64K	0x7008_0000 - 0x700B_FFFF
SA3	4 x 64K	0x700C_0000 - 0x700F_FFFF
…	…	…
SA60	4 x 64K	0x70F0_0000 - 0x70F3_FFFF
SA61	4 x 64K	0x70F4_0000 - 0x70F7_FFFF
SA62	4 x 64K	0x70F8_0000 - 0x70FB_FFFF
SA63	4 x 8K	0x70FC_0000 - 0x70FC_BFFF
SA63	4 x 8K	0x70FC_C000 - 0x70FC_FFFF
SA64	4 x 8K	0x70FD_0000 - 0x70FD_BFFF
SA65	4 x 8K	0x70FD_C000 - 0x70FD_FFFF
SA66	4 x 8K	0x70FE_0000 - 0x70FE_BFFF

SA67	4 x 8K	0x70FE_C000 - 0x70FE_FFFF
SA68	4 x 8K	0x70FF_0000 - 0x70FF_BFFF
SA70	4 x 8K	0x70FF_C000 - 0x70FF_FFFF

Figure 5-32 : S29GL032A-R3 Application Flash Sector Map

The four Spansion **S29GL032A-R4** Flash devices provide 63 sectors (4 x 64 Kbyte each) plus 8 Bottom Boot Sectors (4 x 8 Kbyte each):

Sector	Sector Size (Byte)	Sector Address Range
SA0	4 x 8K	0x7000_0000 - 0x7000_BFFF
SA1	4 x 8K	0x7000_C000 - 0x7000_FFFF
SA2	4 x 8K	0x7001_0000 - 0x7001_BFFF
SA3	4 x 8K	0x7001_C000 - 0x7001_FFFF
SA4	4 x 8K	0x7002_0000 - 0x7002_BFFF
SA5	4 x 8K	0x7002_C000 - 0x7002_FFFF
SA6	4 x 8K	0x7003_0000 - 0x7003_BFFF
SA7	4 x 8K	0x7003_C000 - 0x7003_FFFF
SA8	4 x 64K	0x7004_0000 - 0x7007_FFFF
SA9	4 x 64K	0x7008_0000 - 0x700B_FFFF
SA10	4 x 64K	0x700C_0000 - 0x700F_FFFF
…	…	
SA67	4 x 64K	0x70F0_0000 - 0x70F3_FFFF
SA68	4 x 64K	0x70F4_0000 - 0x70F7_FFFF
SA69	4 x 64K	0x70F8_0000 - 0x70FB_FFFF
SA70	4 x 64K	0x70FC_0000 - 0x70FF_FFFF

Figure 5-33 : S29GL032A-R4 Application Flash Sector Map

The four **Spansion S29GL064A-R3** Flash devices provide 127 sectors (4 x 64 Kbyte each) plus 8 Top Boot Sectors (4 x 8 Kbyte each):

Sector	Sector Size (Byte)	Sector Address Range
SA0	4 x 64K	0x7000_0000 - 0x7003_FFFF
SA1	4 x 64K	0x7004_0000 - 0x7007_FFFF
SA2	4 x 64K	0x7008_0000 - 0x700B_FFFF
SA3	4 x 64K	0x700C_0000 - 0x700F_FFFF
…	…	…
SA60	4 x 64K	0x70F0_0000 - 0x70F3_FFFF
SA61	4 x 64K	0x70F4_0000 - 0x70F7_FFFF
SA126	4 x 64K	0x70F8_0000 - 0x70FB_FFFF

SA127	4 x 8K	0x71FC_0000 - 0x71FC_BFFF
SA128	4 x 8K	0x71FC_C000 - 0x71FC_FFFF
SA129	4 x 8K	0x71FD_0000 - 0x71FD_BFFF
SA130	4 x 8K	0x71FD_C000 - 0x71FD_FFFF
SA131	4 x 8K	0x71FE_0000 - 0x71FE_BFFF
SA132	4 x 8K	0x71FE_C000 - 0x71FE_FFFF
SA133	4 x 8K	0x71FF_0000 - 0x71FF_BFFF
SA134	4 x 8K	0x71FF_C000 - 0x71FF_FFFF

Figure 5-34 : S29GL064A-R3 Application Flash Sector Map

The four Spansion **S29GL064A-R4** Flash devices provide 127 sectors (4 x 64 Kbyte each) plus 8 Bottom Boot Sectors (4 x 8 Kbyte each):

Sector	Sector Size (Byte)	Sector Address Range
SA0	4 x 8K	0x7000_0000 - 0x7000_BFFF
SA1	4 x 8K	0x7000_C000 - 0x7000_FFFF
SA2	4 x 8K	0x7001_0000 - 0x7001_BFFF
SA3	4 x 8K	0x7001_C000 - 0x7001_FFFF
SA4	4 x 8K	0x7002_0000 - 0x7002_BFFF
SA5	4 x 8K	0x7002_C000 - 0x7002_FFFF
SA6	4 x 8K	0x7003_0000 - 0x7003_BFFF
SA7	4 x 8K	0x7003_C000 - 0x7003_FFFF
SA8	4 x 64K	0x7004_0000 - 0x7007_FFFF
SA9	4 x 64K	0x7008_0000 - 0x700B_FFFF
SA10	4 x 64K	0x700C_0000 - 0x700F_FFFF
…	…	
SA131	4 x 64K	0x71F0_0000 - 0x71F3_FFFF
SA132	4 x 64K	0x71F4_0000 - 0x71F7_FFFF
SA133	4 x 64K	0x71F8_0000 - 0x71FB_FFFF
SA134	4 x 64K	0x71FC_0000 - 0x71FF_FFFF

Figure 5-35 : S29GL064A-R4 Application Flash Sector Map

6 VME Bus Interface

The Tundra Universe-II VME/PCI bridge is used as the TVME8240A VME PCI bridge.

The Universe-II is accessible on both the VME bus and the TVME8240A PCI bus.

Please refer to the Universe-II manual for a detailed description of the Universe-II VME/PCI bridge.

6.1 Universe-II PCI Header

The Universe-II PCI device number is 13.

Register Offset	PCI Configuration Register				Setting
	31 ... 24	23 ... 16	15 ... 8	7 ... 0	
0x00	Device ID (Universe)		Vendor ID (Tundra)		0x0000_10E3
0x04	Status		Command		0x0200_0007
0x08	Class Code			Revision ID	0x0680_0001
0x0C	Reserved	Header	Latency	Cache Line	0x0000_0000
0x10	PCI Base Address 0 (Configuration Register I/O Mapped)				0xFFFF_F001(1) (4 Kbyte)
0x14	PCI Base Address 1 (Configuration Register Memory Mapped)				0xFFFF_F000(1) (4 Kbyte)
0x18	PCI Unimplemented				0x0000_0000
0x1C	PCI Unimplemented				0x0000_0000
0x20	PCI Unimplemented				0x0000_0000
0x24	PCI Unimplemented				0x0000_0000
0x28	PCI Reserved				0x0000_0000
0x2C	PCI Reserved				0x0000_0000
0x30	PCI Unimplemented				0x0000_0000
0x34	PCI Reserved				0x0000_0000
0x38	PCI Reserved				0x0000_0000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	0x0003_0100

(1) Read back value after writing all 1's.

Figure 6-1 : Universe-II PCI Header

6.2 Universe-II Power-Up Options

The TVME8240A uses the default Universe-II power-up option configuration.

Please see the Universe-II user manual for details.

6.3 Universe-II Reset Signals

The Universe-II PWRRST# input is controlled by on board power-up reset logic.

The Universe-II RST# input is connected to the PCI reset signal.

The Universe-II LRST# output is used to assert a general board reset in case of a VME bus system reset.

The Universe-II VMERST# input is used to assert a VME bus system reset in case of a general board reset.

The Universe-II VRSYSRST# and VXSYSRST# signals are mapped to the VME bus SYSRST# signal.

If the Universe-II is the VME bus system controller, a general board reset will also assert a VME bus system reset.

If the Universe-II is not the VME bus system controller, a VME bus system reset will also assert a general board reset.

6.4 Universe-II Interrupts

6.4.1 Universe Interrupt Pins

The Universe-II LINT#[0:3] interrupt pins are used as outputs and are mapped to the serial interrupt stream of the MPC8245 PIC.

The Universe-II LINT#[4:7] interrupt pins are not used.

6.4.2 VME Bus Error Interrupt

The TVME8240A provides a dedicated interrupt source for VME bus error events occurring while the Universe-II acts as VME Bus Master.

The Universe-II does only provide a limited functionality for mapping a VME bus error event to the Universe-II LINT# interrupt pins. To overcome this limitation additional on board logic directly monitors the Universe-II VR_BERR (VME BERR#) input while the TVME8240A is the VME Bus Master.

The TVME8240A VME bus error interrupt is handled via the Utility Registers in the Peripheral Devices address space. Please see the Address Map section for details.

6.5 Universe-II VME Bus Modes

On the TVME8240A the Universe-II supports VME bus A32/24/16 master and slave address modes and D32/16/8 master and slave data transfer modes.

Please see the Universe-II user manual for details.

7 Ethernet Interface

The TVME8240A V2.0 provides two Intel 82551 Fast Ethernet Controllers. There is one 10Base-T/100Base-TX interface available on a RJ45 connector at the front panel and a second 10Base-T/100Base-TX interface available on the VME P2 connector for back-I/O.

The 82551 are accessible on the TVME8400 PCI bus (PCI device no. 14 and 17).

The 82551 are reset by a PCI reset.

The 82551 INT# interrupt outputs are mapped to serial channel no. 2 and 14 of the MPC8245 PIC.

Please refer to the Intel 82551 manual for a detailed description of the 82551 Fast Ethernet Controller.

7.1 82551 PCI Header

Offset	PCI Configuration Register				Setting
	31 - 24	23 - 16	15 - 08	07 - 00	
0x00	Device ID		Vendor ID		0x1209_8086
0x04	Status		Command		0x0290_0007
0x08	Class Code			Revision ID	0x0200_00xx
0x0C	BIST	Header	Latency	Cache Line	0x0000_xx00
0x10	PCI Base Address 0 (Memory Mapped Configuration Register)				0xFFFF_F000(1) (4 Kbyte)
0x14	PCI Base Address 0 (I/O Mapped Configuration Register)				0xFFFF_FF81(1) (64 Byte)
0x18	PCI Base Address 0 (Memory Mapped Flash Space)				0xFFFE_0000(1) (128 Kbyte)
0x1C	Reserved				0x0000_0000
0x20	Reserved				0x0000_0000
0x24	Reserved				0x0000_0000
0x28	Reserved				0x0000_0000
0x2C	Subsystem ID		Subsystem Vendor ID		0x0000_0000
0x30	Expansion ROM PCI Base Address				0x0000_0000
0x34	Reserved			Cap. Pointer	0x0000_00DC
0x38	Reserved				0x0000_0000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	0xxx08_0100
0xDC	Power Management Cap.		Next Cap.	Cap. ID	0x7E22_0001
0xE0	Reserved	Data	Power Management CSR		0x4B00_4000

(1) Read back Value after writing all 1's.

Figure 7-1 : 82551 PCI Header

7.2 82551 Configuration EEPROM

EEPROM Address (16 bit Address)	Description		Value
	Bits 15 - 8	Bits 07 - 00	
0x00	Ethernet Address Byte [1:0]		0x0100
0x01	Ethernet Address Byte [3:2]		0xXX06
0x02	Ethernet Address Byte [5:4]		0xZZYY
0x03	Compatibility Byte[1:0]		0x0B87
0x04	Reserved		0x0000
0x05	Controller Type	Connectors	0x0201
0x06	Primary PHY Record		0x4701
0x07	Secondary PHY Record		0x0000
0x08	PWA Byte [1:0]		0x0000
0x09	PWA Byte [3:2]		0x0000
0x0A	EEPROM-ID		0x5FE0
0x0B	Subsystem-ID		0x0000
0x0C	Subsystem-Vendor-ID		0x0000
0x0D – 0x22	Reserved		0x0000
0x23	Device-ID		0x1209
0x24 – 0x2F	Reserved		0x0000
0x30	Boot Agent Main Setup Options		0x900C
0x31	Boot Agent Configuration Customization Options		0x0000
0x32	Boot Agent Configuration Customization Options		0x0000
0x33	IBA Capabilities		0x0001
0x34 – 0x3E	Reserved		0x0000
0x3F	EEPROM Checksum		

Figure 7-2 : Intel 82551 Configuration EEPROM Settings

7.3 Media Capabilities

- IEEE 802.3 10Base-T / 100Base-TX interface, available at a RJ45 front panel connector
- IEEE 802.3 10Base-T / 100Base-TX interface, available at the VME P2 connector

8 IP Bus Interface

The TVME8240A IP interface space is accessible in the PCI Memory space.

The PCI9030 PCI Target Chip from PLX Technology is used as the PCI target device for accessing the IP interface.

A Xilinx FPGA is used on the PCI9030 local bus to implement the IP interface control and register functions.

8.1 PCI9030 PCI Target Chip

The PCI9030 provides four local spaces 0:3 that are used by the TVME8240A IP interface.

Basic PCI9030 register configuration is loaded from a serial EEPROM after power-up or board reset.

Programming of the PCI9030 PCI and local configuration registers and the PCI9030 Configuration EEPROM is scope of the board initialization software.

8.1.1 PCI9030 PCI Header

The PCI9030 PCI device number is 16.

Register Offset	PCI Configuration Register				Setting
	31 … 24	23 … 16	15 … 8	7 … 0	
0x00	Device ID (PCI9030)		Vendor ID (PLX Technology)		0x9030_10B5
0x04	Status		Command		0x0280_0003
0x08	Class Code			Revision ID	0x0680_0000
0x0C	Not Supported	Header	Not Supported	Cache Line	0x0000_0000
0x10	PCI Base Address 0 (PCIBAR0) (PCI9030 Local Configuration Register Memory Mapped)				0xFFFF_FF80 (128 Byte)
0x14	PCI Base Address 1 (PCIBAR1) (PCI9030 Local Configuration Register I/O Mapped)				0xFFFF_FF81[1] (128 Byte)
0x18	PCI Base Address 2 (PCIBAR2) (Local Space 0)				0xFFFF_FF00[1] (256 Byte)
0x1C	PCI Base Address 3 (PCIBAR3) (Local Space 1)				0xFFFF_FC00[1] (1 Kbyte)
0x20	PCI Base Address 4 (PCIBAR4) (Local Space 2)				0xFE00_0000[1] (32 Mbyte)
0x24	PCI Base Address 5 (PCIBAR5) (Local Space 3)				0xFF00_0000[1] (16 Mbyte)
0x28	Not Supported				0x0000_0000
0x2C	Subsystem ID (TVME8240A)		Subsystem Vendor ID (TEWS TECHNOLOGIES)		0x2030_1498
0x30	PCI Expansion ROM Base Address				0x0000_0000
0x34	Reserved			Cap. Pointer	0x0000_0040
0x38	Reserved				0x0000_0000
0x3C	Not Supported	Not Supported	Interrupt Pin	Interrupt Line	0x0000_0100
0x40	PM Capabilities		PM NxtCap	PM CapID	0x4801_4801
0x44	PM Data	PM CSR EXT	PM CSR		0x0000_0000
0x48	Reserved	HS CSR	HS NxtCap	HS CapID	0x0000_4C06
0x4C	VPD Address		VPD NxtCap	VPD CapID	0x0000_0003
0x50	VPD Data				0x0000_0000

[1] Read back Value after writing all 1's.

Figure 8-1 : PCI9030 PCI Header

8.1.2 Local Configuration Register

The PCI base address for the PCI9030 Local Configuration Registers can be obtained from the PCIBAR0 (PCI Memory mapped) register at offset 0x10 or from the PCIBAR1 (PCI I/O mapped) register at offset 0x14 in the PCI9030 PCI configuration register space.

Register Offset	Local Configuration Register	Name	Setting
0x00	Local Space 0 Range	LAS0RR	0x0FFF_FF00
0x04	Local Space 1 Range	LAS1RR	0x0FFF_FC00
0x08	Local Space 2 Range	LAS2RR	0x0E00_0000
0x0C	Local Space 3 Range	LAS3RR	0x0F00_0000
0x10	Expansion ROM Range	EROMRR	0x0000_0000
0x14	Local Space 0 Remap	LAS0BA	0x0800_0001
0x18	Local Space 1 Remap	LAS1BA	0x0400_0001
0x1C	Local Space 2 Remap	LAS2BA	0x0000_0001
0x20	Local Space 3 Remap	LAS3BA	0x0200_0001
0x24	Expansion ROM Remap	EROMBA	0x0000_0000
0x28	Local Space 0 Descriptor	LAS0BRD	0xD541_60A0
0x2C	Local Space 1 Descriptor	LAS1BRD	0x1541_20A2
0x30	Local Space 2 Descriptor	LAS2BRD	0x1541_20A2
0x34	Local Space 3 Descriptor	LAS3BRD	0x1501_20A2
0x38	Expansion ROM Descriptor	EROMBRD	0x0000_0000
0x3C	Local Chip Select 0	CS0BASE	0x0800_0081
0x40	Local Chip Select 1	CS1BASE	0x0400_0201
0x44	Local Chip Select 2	CS2BASE	0x0100_0001
0x48	Local Chip Select 3	CS3BASE	0x0280_0001
0x4C	Serial EEPROM / Interrupt Control & Status	PROT_AREA / INTCSR	0x0030_0049
0x50	Miscellaneous	CNTRL	0x007A_4000
0x54	General Purpose I/O	GPIOC	0x0224_9252

Figure 8-2 : PCI9030 Local Configuration Register

Shown values are register values after serial EEPROM configuration.

8.1.3 PCI9030 Configuration EEPROM

Basic PCI9030 register configuration is loaded from an on board serial EEPROM at power-up or board reset.

EEPROM Offset	Register Offset	Register Description	Register Bits Affected	Value
0x00	PCI 0x02	Device ID	PCIIDR[31:16]	0x9030
0x02	PCI 0x00	Vendor ID	PCIIDR[15:0]	0x10B5
0x04	PCI 0x06	PCI Status	PCISR[15:0]	0x0280
0x06	PCI 0x04	PCI Command	Reserved	0x0000
0x08	PCI 0x0A	Class Code	PCICCR[15:0]	0x0680
0x0A	PCI 0x08	Class Code / Revision	PCICR[7:0] / PCIREV[7:0]	0x0000
0x0C	PCI 0x2E	Subsystem ID	PCISID[15:0]	0x2030
0x0E	PCI 0x2C	Subsystem Vendor ID	PCISVID[15:0]	0x1498
0x10	PCI 0x36	MSB New Capability Pointer	Reserved	0x0000
0x12	PCI 0x34	LSB New Capability Pointer	CAP_PTR[7:0]	0x0040
0x14	PCI 0x3E	Max_Lat, Max_Gnt	Reserved	0x0000
0x16	PCI 0x3C	Interrupt Pin	PCIIPR[7:0] / Reserved	0x0100
0x18	PCI 0x42	MSW Power Management Capabilities	PMC[14:11, 5, 3:0]	0x4801
0x1A	PCI 0x40	LSW Power Management Capabilities	PM_NEXT[7:0] / PMCAPID[7:0]	0x4801
0x1C	PCI 0x46	MSW Power Management Data / PMCSR Bridge Support Ext.	Reserved	0x0000
0x1E	PCI 0x44	LSW Power Management Control / Status	PMCSR[14:8]	0x0000
0x20	PCI 0x4A	MSW Hot Swap Control / Status	Reserved	0x0000
0x22	PCI 0x48	LSW Hot Swap Next Capability Pointer / Hot Swap Control	HS_NEXT[7:0] / HS_CNTL[7:0]	0x4C06
0x24	PCI 0x4E	PCI Vital Product Data Address	Reserved	0x0000
0x26	PCI 0x4C	PCI Vital Product Data Next Capability Pointer / PCI Vital Product Data Control	PVPD_NEXT[]7:0] / PVPD_CNTL[7:0]	0x0003
0x28	Local 0x02	MSW Local Space 0 Range	LAS0RR[31:16]	0x0FFF
0x2A	Local 0x00	LSW Local Space 0 Range	LAS0RR[15:0]	0xFF00
0x2C	Local 0x06	MSW Local Space 1 Range	LAS1RR[31:16]	0x0FFF
0x2E	Local 0x04	LSW Local Space 1 Range	LAS1RR[15:0]	0xFC00
0x30	Local 0x0A	MSW Local Space 2 Range	LAS2RR[31:16]	0x0E00
0x32	Local 0x08	LSW Local Space 2 Range	LAS2RR[15:0]	0x0000
0x34	Local 0x0E	MSW Local Space 3 Range	LAS3RR[31:16]	0x0F00
0x36	Local 0x0C	LSW Local Space 3 Range	LAS3RR[15:0]	0x0000
0x38	Local 0x12	MSW Local Exp. ROM Range	EROMRR[31:16]	0x0000
0x3A	Local 0x10	LSW Local Exp. ROM Range	EROMRR[15:0]	0x0000
0x3C	Local 0x16	MSW Local Space 0 Remap	LAS0BA[31:16]	0x0800
0x3E	Local 0x14	LSW Local Space 0 Remap	LAS0BA[15:0]	0x0001
0x40	Local 0x1A	MSW Local Space 1 Remap	LAS1BA[31:16]	0x0400

EEPROM Offset	Register Offset	Register Description	Register Bits Affected	Value
0x42	Local 0x18	LSW Local Space 1 Remap	LAS1BA[31:16]	0x0001
0x44	Local 0x1E	MSW Local Space 2 Remap	LAS2BA[31:16]	0x0000
0x46	Local 0x1C	LSW Local Space 2 Remap	LAS2BA[31:16]	0x0001
0x48	Local 0x22	MSW Local Space 3 Remap	LAS3BA[31:16]	0x0200
0x4A	Local 0x20	LSW Local Space 3 Remap	LAS3BA[31:16]	0x0001
0x4C	Local 0x26	MSW Local Exp. ROM Remap	EROMBA[31:16]	0x0000
0x4E	Local 0x24	LSW Local Exp. ROM Remap	EROMBA[15:0]	0x0000
0x50	Local 0x2A	MSW Local Space 0 Descriptor	LAS0BRD[31:0]	0xD541
0x52	Local 0x28	LSW Local Space 0 Descriptor	LAS0BRD[15:0]	0x60A0
0x54	Local 0x2E	MSW Local Space 1 Descriptor	LAS1BRD[31:0]	0x1541
0x56	Local 0x2C	LSW Local Space 1 Descriptor	LAS1BRD[15:0]	0x20A2
0x58	Local 0x32	MSW Local Space 2 Descriptor	LAS2BRD[31:0]	0x1541
0x5A	Local 0x30	LSW Local Space 2 Descriptor	LAS2BRD[15:0]	0x20A2
0x5C	Local 0x36	MSW Local Space 3 Descriptor	LAS3BRD[31:0]	0x1501
0x5E	Local 0x34	LSW Local Space 3 Descriptor	LAS3BRD[15:0]	0x20A2
0x60	Local 0x3A	MSW Local Exp. ROM Descriptor	EROMBRD[31:16]	0x0000
0x62	Local 0x38	LSW Local Exp. ROM Descriptor	EROMBRD[15:0]	0x0000
0x64	Local 0x3E	MSW Local Chip Select 0	CS0BASE[31:16]	0x0800
0x66	Local 0x3C	LSW Local Chip Select 0	CS0BASE[15:0]	0x0081
0x68	Local 0x42	MSW Local Chip Select 1	CS1BASE[31:16]	0x0400
0x6A	Local 0x40	LSW Local Chip Select 1	CS1BASE[15:0]	0x0201
0x6C	Local 0x46	MSW Local Chip Select 2	CS2BASE[31:16]	0x0100
0x6E	Local 0x44	LSW Local Chip Select 2	CS2BASE[15:0]	0x0001
0x70	Local 0x4A	MSW Local Chip Select 3	CS3BASE[31:16]	0x0280
0x72	Local 0x48	LSW Local Chip Select 3	CS3BASE[15:0]	0x0001
0x74	Local 0x4E	Serial EEPROM Write Protect	PROT_AREA[7:0]	0x0030
0x76	Local 0x4C	LSW Interrupt Control / Status	INTCSR[15:0]	0x0049
0x78	Local 0x52	MSW Miscellaneous	CNTRL[31:16]	0x007A
0x7A	Local 0x50	LSW Miscellaneous	CNTRL[15:0]	0x4000
0x7C	Local 0x56	MSW General Purpose I/O Control	GPIOC[31:16]	0x0224
0x7E	Local 0x54	LSW General Purpose I/O Control	GPIOC[15:0]	0x9252
0x80	Local 0x72	MSW Power Management Data Select		0x0000
0x82	Local 0x70	LSW Power Management Data Select		0x0000
0x84	Local 0x76	MSW Power Management Data Scale		0x0000
0x86	Local 0x74	LSW Power Management Data Scale		0x0000

Figure 8-3 : PCI9030 Configuration EEPROM Settings

EEPROM Address	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x9030	0x10B5	0x0280	0x0000	0x0680	0x0000	0x2030	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x4801	0x0000	0x0000
0x20	0x0000	0x4C06	0x0000	0x0003	0x0FFF	0xFF00	0x0FFF	0xFC00
0x30	0x0E00	0x0000	0x0F00	0x0000	0x0000	0x0000	0x0800	0x0001
0x40	0x0400	0x0001	0x0000	0x0001	0x0200	0x0001	0x0000	0x0000
0x50	0xD541	0x60A0	0x1541	0x20A2	0x1541	0x20A2	0x1501	0x20A2
0x60	0x0000	0x0000	0x0800	0x0081	0x0400	0x0201	0x1200	0x0001
0x70	0x0280	0x0001	0x0030	0x0049	0x007A	0x4000	0x0224	0x9252
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Figure 8-4 : PCI9030 Configuration EEPROM Content

8.2 IP Interface

The IP FPGA provides the interface between the PCI9030 local bus and the IP slots.

The IP FPGA also provides the IP Interface Control Registers.

The IP FPGA is configured at power-up or board reset by an on board serial Flash.

Board Initialization software should verify successful FPGA configuration in the Utility Status Register.

8.2.1 PCI9030 Local Space Assignment

The PCI9030 local spaces are used to access the IP interface. The PCI base address for each local space can be obtained from the PCI9030 PCI configuration register space.

PCI9030 Local Space	Size (Byte)	Port Width (Bit)	Endian Mode	PCI Space	IP Interface Space
0	256	16	BIG	MEM	IP Interface Register
1	1 K	16	BIG	MEM	IP A-D ID, INT, IO Space (8/16 bit)
2	32 M	16	BIG	MEM	IP A-D MEM Space (8/16 bit)
3	16 M	8	BIG	MEM	IP A-D MEM Space (8 bit)

Figure 8-5 : PCI9030 Local Space Assignment

8.2.2 Local Space 0 Address Map

The PCI9030 local space 0 is used for the IP interface registers.

The PCI base address for local space 0 is PCIBAR2 at offset 0x18 in the PCI9030 PCI configuration register space.

Offset (Base = PCI Base Address 2)	Size (Byte)	Register
0x00	2	REVISION ID
0x02	2	IP A CONTROL
0x04	2	IP B CONTROL
0x06	2	IP C CONTROL
0x08	2	IP D CONTROL
0x0A	2	RESET
0x0C	2	STATUS
0x0E	2	Reserved
0x10 - 0xFF	240	Reserved

Figure 8-6 : Local Space 0 Address Map (IP Interface Register)

8.2.3 IP Interface Register

8.2.3.1 Revision ID Register

The Revision ID Register shows the revision of the on board IP FPGA logic.

Bit	Name	Description
15 (MSB)	-	Read : Undefined Write : No Effect
14		
13		
12		
11		
10		
9		
8		
7	REV_ID	Read: FPGA Logic Revision ID Write : No Effect
6		
5		
4		
3		
2		
1		
0 (LSB)		

Figure 8-7 : Revision ID Register

8.2.3.2 IP X Control Registers

The IP X Control Registers are used to control IP interrupts, recover time and clock rate.

There is one IP Control Register for each IP Slot (A-D).

Bit	Name	Description
15 (MSB)	-	Read : Undefined Write : No Effect. Should be written with 0's
14		
13		
12		
11		
10		
9		
8	SEL_MODE	0 : Single IP Select Cycle 1 : Extended IP Select Cycle IP Select is held active until the first IP Acknowledge Cycle is detected. May be required by some IP modules.
7	INT1_EN	0 : IP Interrupt 1 Disabled 1 : IP Interrupt 1 Enabled
6	INT0_EN	0 : IP Interrupt 0 Disabled 1 : IP Interrupt 0 Enabled
5	INT1_SENSE	0 : IP Interrupt 1 Level Sensitive 1 : IP Interrupt 1 Edge Sensitive
4	INT0_SENSE	0 : IP Interrupt 0 Level Sensitive 1 : IP Interrupt 0 Edge Sensitive
3	ERR_INT_EN	0 : IP Error Interrupt Disabled 1 : IP Error Interrupt Enabled
2	TIME_INT_EN	0 : IP Timeout Interrupt Disabled 1 : IP Timeout Interrupt Enabled
1	RECOVER	0 : IP Recover Time Disabled 1 : IP Recover Time Enabled
0 (LSB)	CLKRATE	0 : IP Clock Rate 8 MHz 1 : IP Clock Rate 32 MHz

Figure 8-8 : IP X Control Register

After power-up or board reset all bits in the IP X Control Registers are cleared.

If IP recover time is enabled for an IP slot, an IP cycle for this slot will not begin until the IP recover time is expired. The IP recover time is app. 1µs.

8.2.3.3 Reset Register

The Reset Register is used to assert the IP RESET# signal and to detect when the IP reset phase is done.

Bit	Name	Description
15 (MSB)	-	Read : Undefined Write : No Effect. Should be written with 0's
14		
13		
12		
11		
10		
9		
8		
7		
6		
5		
4		
3		
2		
1		
0 (LSB)	IP_RESET	Read : 0 : IP RESET# Signal is De-asserted 1 : IP RESET# Signal is Asserted Write : 0 : No Effect 1 : Assert IP RESET# Signal (Automatic Negation)

Figure 8-9 : Reset Register

The IP RESET# signal is also asserted at power-up or board reset.

8.2.3.4 Status Register

The Status Register is used to read IP timeout, error and interrupt status.

The IP timeout time is app. 8µs.

An IP timeout occurs if the IP module fails to generate the IP ACK# signal within the IP timeout time. An IP timeout is not reported to the PCI9030 or the PCI Master, but in the Status Register. For timeout reads all F's are returned.

Bit	Name	Description
15 (MSB)	TIME_D	Read : 0 : No Timeout on IP_D 1 : IP_D Timeout has occurred Write : 0 : No Effect 1 : Clear IP_D Timeout Status
14	TIME_C	Read : 0 : No Timeout on IP_C 1 : IP_C Timeout has occurred Write : 0 : No Effect 1 : Clear IP_C Timeout Status
13	TIME_B	Read : 0 : No Timeout on IP_B 1 : IP_B Timeout has occurred Write : 0 : No Effect 1 : Clear IP_B Timeout Status
12	TIME_A	Read : 0 : No Timeout on IP_A 1 : IP_A Timeout has occurred Write : 0 : No Effect 1 : Clear IP_A Timeout Status
11	ERR_D	Read : 0 : No Error on IP_D 1 : IP_D ERROR# Signal Asserted Write : No Effect
10	ERR_C	Read : 0 : No Error on IP_C 1 : IP_C ERROR# Signal Asserted Write : No Effect
9	ERR_B	Read : 0 : No Error on IP_B 1 : IP_B ERROR# Signal Asserted Write : No Effect

Bit	Name	Description
8	ERR_A	Read : 0 : No Error on IP_A 1 : IP_A ERROR# Signal Asserted Write : No Effect
7	INT1_D	Read : 0 : No Interrupt 1 Request on IP_D 1 : Active IP_D Interrupt 1 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_D Interrupt 1 Status
6	INT0_D	Read : 0 : No Interrupt 0 Request on IP_D 1 : Active IP_D Interrupt 0 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_D Interrupt 0 Status
5	INT1_C	Read : 0 : No Interrupt 1 Request on IP_C 1 : Active IP_C Interrupt 1 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_C Interrupt 1 Status
4	INT0_C	Read : 0 : No Interrupt 0 Request on IP_C 1 : Active IP_C Interrupt 0 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_C Interrupt 0 Status
3	INT1_B	Read : 0 : No IP_B Interrupt 1 Request 1 : Active IP_B Interrupt 1 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_B Interrupt 1 Status
2	INT0_B	Read : 0 : No Interrupt 0 Request on IP_B 1 : Active IP_B Interrupt 0 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_B Interrupt 0 Status
1	INT1_A	Read : 0 : No Interrupt 1 Request on IP_A 1 : Active IP_A Interrupt 1 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_A Interrupt 1 Status

Bit	Name	Description
0 (LSB)	INT0_A	Read : 0 : No Interrupt 0 Request on IP_A 1 : Active IP_A Interrupt 0 Request Write : 0 : No Effect 1 : Clear Edge Sensitive IP_A Interrupt 0 Status

Figure 8-10 : Status Register

8.2.4 Local Space 1 Address Map

The PCI9030 local space 1 is used for the IP A-D ID, INT and I/O space.

The PCI base address for local space 1 is PCIBAR3 at offset 0x1C in the PCI9030 PCI configuration register space.

Offset (Base = PCI Base Address 3)		Size (Byte)	IP Slot	IP Space
Start	End			
0x0000_0000	0x0000_007F	128	A	I/O
0x0000_0080	0x0000_00BF	64	A	ID
0x0000_00C0	0x0000_00FF	64	A	INT
0x0000_0100	0x0000_017F	128	B	I/O
0x0000_0180	0x0000_01BF	64	B	ID
0x0000_01C0	0x0000_01FF	64	B	INT
0x0000_0200	0x0000_027F	128	C	I/O
0x0000_0280	0x0000_02BF	64	C	ID
0x0000_02C0	0x0000_02FF	64	C	INT
0x0000_0300	0x0000_037F	128	D	I/O
0x0000_0380	0x0000_03BF	64	D	ID
0x0000_03C0	0x0000_03FF	64	D	INT

Figure 8-11 : Local Space 1 Address Map (IP A-D ID, INT, I/O Space)

The TVME8240A will perform write cycles to the IP ID space.

Any access to the IP INT space will assert the IP INTSEL# signal on the selected IP slot. The TVME8240A will perform write cycles to the IP INT space.

The user should perform IP INT space read cycles on the desired IP slot to generate an IP INTSEL# cycle and read the interrupt vector. For this read cycle the address must reflect if the IP INTSEL# cycle is for IP INT0# or for IP INT1#.

8.2.5 Local Space 2 Address Map

The PCI9030 local space 2 is used for the IP A-D Memory space (16/32 bit).

The PCI base address for local space 2 is PCIBAR4 at offset 0x20 in the PCI9030 PCI configuration register space.

Offset (Base = PCI Base Address 4)		Size (Byte)	IP Slot	IP Space
Start	End			
0x0000_0000	0x007F_FFFF	8 M	A	MEM (16 bit)
0x0080_0000	0x00FF_FFFF	8 M	B	MEM (16 bit)
0x0100_0000	0x017F_FFFF	8 M	C	MEM (16 bit)
0x0180_0000	0x01FF_FFFF	8 M	D	MEM (16 bit)

Figure 8-12 : Local Space 2 Address Map (IP A-D Memory Space 16 bit)

8.2.6 Local Space 3 Address Map

The PCI9030 local space 3 is used for the IP A-D Memory space (8 bit port).

The PCI base address for local space 3 is PCIBAR5 at offset 0x24 in the PCI9030 PCI configuration register space.

Offset (Base = PCI Base Address 5)		Size (Byte)	Description
Start	End		
0x0000_0000	0x003F_FFFF	4 M	IP A MEM Space (8 bit)
0x0040_0000	0x007F_FFFF	4 M	IP B MEM Space (8 bit)
0x0080_0000	0x00BF_FFFF	4 M	IP C MEM Space (8 bit)
0x00C0_0000	0x00FF_FFFF	4 M	IP D MEM Space (8 bit)

Figure 8-13 : Local Space 3 Address Map (IP A-D Memory Space 8 bit)

The 8 bit IP Memory space should be used for memory space linear byte addressing of IP modules that use IP data lines D[7:0] only.

8.3 IP Interrupts

All IP Interface interrupt sources are mapped to the PCI9030 local interrupt input 1 (LINT1#). The PCI9030 local interrupt 2 (LINT2#) is not used. The PCI9030 PCI interrupt output is mapped to the serial interrupt no. 4 of the MPC8245 PIC.

Upon detecting PIC Serial Interrupt No. 4 read the IP Status Register to determine the IP interrupt source. Timeout interrupts and edge sensitive IP interrupts must be cleared in the IP Status Register. Error interrupts should be disabled after being noticed once.

9 PCI Device Summary

PCI Device	Device Number	Device ID	Vendor ID	Subsys ID	Subsys Vendor ID	PCI Arbiter Line (MPC8245)	Required Memory Space (Byte)	Required I/O Space (Byte)
MPC8245 Integrated Host PPC	Host	0x0006	0x1057	0x0000	0x0000	-	-	-
Universe-II VME / PCI Bridge	13	0x0000	0x10E3	-	-	0	4K + Appl. dep. PCI Target Images	4K
82551 Fast Ethernet Controller (1)	14	0x1209	0x8086	0x0000	0x0000	1	4K + 128	64
PCI9030 PCI Target Chip IPAC Interface	16	0x9030	0x10B5	0x2030	9x1498	-	32M + 16M + 1K + 256 + 128	128
82551 Fast Ethernet Controller (2)	17	0x1209	0x8086	0x0000	0x0000	4	4K + 128K	64
PCI Expansion Connector	Depends on PCI Exp. Card	Depends on PCI Exp. Card	Depends on PCI Exp. Card	Depends on PCI Exp. Card	Depends on PCI Exp. Card	3	Depends on PCI Exp. Card	Depends on PCI Exp. Card

Figure 9-1 : PCI Device Summary

10 Board I/O

10.1 Board I/O Overview

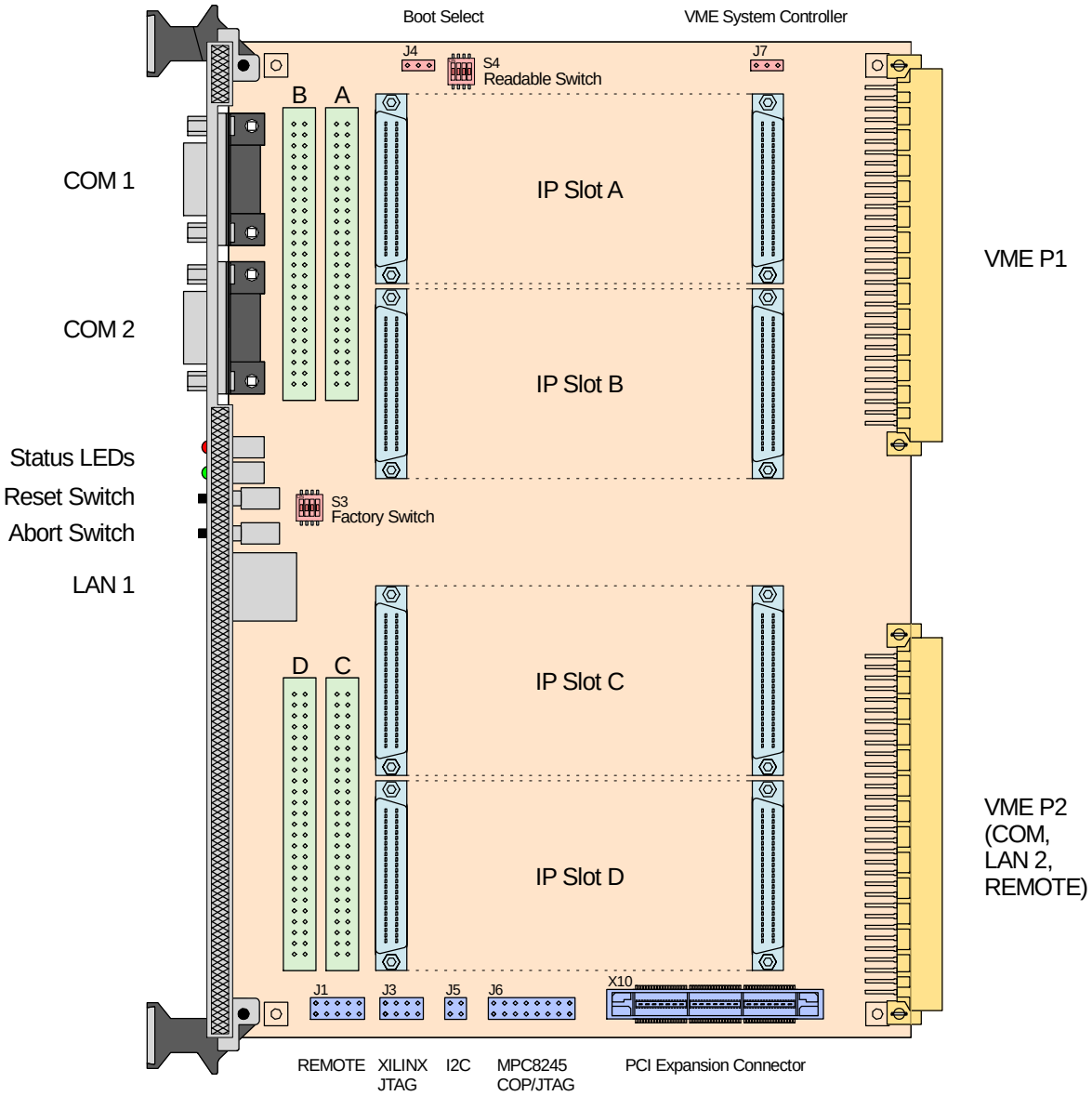


Figure 10-1 : Board I/O Overview

10.2 Jumper

10.2.1 Boot Select Jumper

Boot Select Jumper Configuration	
Open	Run Flash Application after board initialization
1 - 2 Installed	
2 - 3 Installed	Run PMON Bug Program after board initialization

Figure 10-2 : Boot Select Jumper Configuration

The boot select jumper status can be read in the Utility Status Register.

After board initialization the boot select jumper determines the address of the next program instruction.

If used, the first instruction in the Application Flash must reside at address 0x7000_0100.

10.2.2 VME System Controller Jumper

VME SYSTEM CONTROLLER JUMPER	
Open	VME System Controller
1 - 2 Installed	Not VME System Controller
2 - 3 Installed	VME System Controller Auto Configuration

Figure 10-3 : VME System Controller Jumper

The VME system controller jumper sets the Universe-II BGIN3# input signal, which the Universe-II samples at the end of VME SYSRST# to determine the VME System Controller mode.

10.3 Header

10.3.1 Remote Front Header

The Remote Front Header could be used to control the TVME8240A front panel switches from a remote location and to indicate the TVME8240A front panel LED status at a remote location.

Pin	Signal	Signal	Pin
1	NC	+5V	2
3	ACTIVITY_LED#	FUSE_LED#	4
5	FAIL_LED#	NC (no pin)	6
7	SYSCON_LED#	ABORT_SW#	8
9	RESET_SW#	GND	10

Figure 10-4 : Remote Front Header

The LED output signals are generated from a 5V CMOS level push-pull output stage (74ACT logic).

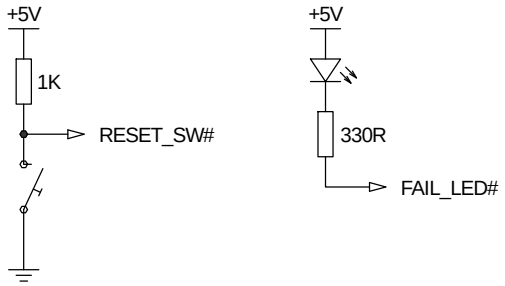


Figure 10-5 : Remote Connection Example

10.4 LEDs

During board reset the four front panel LEDs are ON.

LED	Front Text	Color	Control	Set Condition
Failure	FAIL	Red	SW	Register Bit set
Fuse Alarm	FUSE	Red	HW	On board Fuse triggers
Activity	ACT	Green	HW	Board Local Memory Bus or PCI Bus activity
System Controller	SYS	Green	HW	Board is VME System Controller

Figure 10-6 : LED Overview

10.4.1 Failure LED

The Failure LED (FAIL) (red) is set by software control to indicate a failure condition.

Please see the Utility Register Section for details.

10.4.2 Fuse Alarm LED

The Fuse Alarm LED (FUSE) (red) is set by hardware control if any of the on board resettable fuses triggers.

There is one resettable fuse for each of the following power supplies:

- IP Slot A/B +5V
- IP Slot C/D +5V
- IP Slot A/B/C/D +12V
- IP Slot A/B/C/D -12V

10.4.3 Activity LED

The Activity LED (ACT) (green) is set by hardware control if there is any activity on the Local Memory bus or PCI bus.

10.4.4 System Controller LED

The System Controller LED (SYS) (green) is set by hardware control if the Universe (VME-PCI Bridge) is the VME bus System Controller.

10.5 Switches

The TVME8240A provides two push-button switches plus a software readable DIP-Switch.

The two push-button switches are available at the TVME8240A front plate. Additionally, both switches could also be activated by dedicated pins on the 10-pin Remote Front Header or by the use of VME P2 connector signals.

10.5.1 Reset Switch

The Reset switch (RST) is used to generate a board reset.

A board reset is also performed at power-up.

A board reset can also be asserted by software, programming a Utility Control Register.

A board reset will perform a general board hardware reset, re-configuration and reset of the IP FPGA, PCI reset and CPU reset.

If the TVME8240A is the VME bus system controller, a board reset will also assert a VME bus system reset.

10.5.2 Abort Switch

The Abort switch (ABT) is used to generate a CPU interrupt.

The Abort Switch is mapped to serial interrupt no. 1 of the MPC8245 PIC. If used, Serial interrupt no. 1 must be configured as edge sensitive.

10.5.3 Software Readable DIP-Switch

The software readable DIP-Switch provides 4 positions, readable in a Utility Status Register.

Please see the Utility Register Section for details.

10.6 Connectors

10.6.1 VME Interface Connectors

10.6.1.1 VME P1 Connector

Pin	Row A	Row B	Row C
1	VME_D0	VME_BBSY#	VME_D8
2	VME_D1	VME_BCLR#	VME_D9
3	VME_D2	VME_ACFAIL#	VME_D10
4	VME_D3	VME_BGIN0#	VME_D11
5	VME_D4	VME_BGOUT0#	VME_D12
6	VME_D5	VME_BGIN1#	VME_D13
7	VME_D6	VME_BGOUT1#	VME_D14
8	VME_D7	VME_BGIN2#	VME_D15
9	GND	VME_BGOUT2#	GND
10	VME_SYSCLK	VME_BGIN3#	VME_SYSFAIL#
11	GND	VME_BGOUT3#	VME_BERR#
12	VME_DS1#	VME_BR0#	VME_SYSRST#
13	VME_DS0#	VME_BR1#	VME_LWORD#
14	VME_WRITE#	VME_BR2#	VME_AM5
15	GND	VME_BR3#	VME_A23
16	VME_DTACK#	VME_AM0	VME_A22
17	GND	VME_AM1	VME_A21
18	VME_AS#	VME_AM2	VME_A20
19	GND	VME_AM3	VME_A19
20	VME_IACK#	GND	VME_A18
21	VME_IACKIN#	NC	VME_A17
22	VME_IACKOUT#	NC	VME_A16
23	VME_AM4	GND	VME_A15
24	VME_A7	VME_IRQ7#	VME_A14
25	VME_A6	VME_IRQ6#	VME_A13
26	VME_A5	VME_IRQ5#	VME_A12
27	VME_A4	VME_IRQ4#	VME_A11
28	VME_A3	VME_IRQ3#	VME_A10
29	VME_A2	VME_IRQ2#	VME_A9
30	VME_A1	VME_IRQ1#	VME_A8
31	-12V	NC	+12V
32	+5V	+5V	+5V

Figure 10-7 : VME P1 Connector

10.6.1.2 VME P2 Connector

Pin	Row A	Row B	Row C
1	Reserved	+5V	Reserved
2	Reserved	GND	Reserved
3	Reserved	NC	LAN2_TD-
4	Reserved	VME_A24	LAN2_TD+
5	Reserved	VME_A25	LAN2_RD-
6	Reserved	VME_A26	LAN2_RD+
7	Reserved	VME_A27	Reserved
8	Reserved	VME_A28	LAN2_TERMPLANE
9	Reserved	VME_A29	LAN2_TERMPLANE
10	Reserved	VME_A30	+5V
11	Reserved	VME_A31	ACT_LED# (o)
12	Reserved	GND	FUSE_LED# (o)
13	Reserved	+5V	FAIL_LED# (o)
14	Reserved	VME_D16	SYS_LED# (o)
15	Reserved	VME_D17	ABORT_SW# (i)
16	Reserved	VME_D18	RESET_SW# (i)
17	Reserved	VME_D19	GND
18	Reserved	VME_D20	COM2_RXD2+ (i)
19	COM2_TXD+ (o)	VME_D21	NC
20	NC	VME_D22	Reserved
21	NC	VME_D23	NC
22	NC	GND	NC
23	NC	VME_D24	NC
24	NC	VME_D25	NC
25	COM2_RXD/RXD- (i)	VME_D26	NC
26	COM2_TXD/TXD- (o)	VME_D27	Reserved
27	COM2_CTS (i)	VME_D28	COM1_TXD (o)
28	NC	VME_D29	COM1_RXD (i)
29	COM2_RTS (o)	VME_D30	COM1_RTS (o)
30	NC	VME_D31	COM1_CTS (i)
31	NC	GND	COM1_DTR (o)
32	NC	+5V	COM1_DCD (i)

Figure 10-8 : VME P2 Connector

For each serial port, only one connection scheme is allowed at a time, either via the VME P2 connector or via the front plate DB9 connector.

10.6.2 IP Interface Connectors

10.6.2.1 IP P1 Connector

Pin	Signal	Pin	Signal
1	GND	2	CLK
3	RESET#	4	D0
5	D1	6	D2
7	D3	8	D4
9	D5	10	D6
11	D7	12	D8
13	D9	14	D10
15	D11	16	D12
17	D13	18	D14
19	D15	20	BS0#
21	BS1#	22	-12V
23	+12V	24	+5V
25	GND	26	GND
27	+5V	28	WRITE#
29	IDSEL#	30	NC
31	MEMSEL#	32	NC
33	INTSEL#	34	DMAACK#
35	IOSEL#	36	RSV0
37	A1	38	DMAEND#
39	A2	40	ERROR#
41	A3	42	INTREQ0#
43	A4	44	INTREQ1#
45	A5	46	STROBE#
47	A6	48	ACK#
49	RSV1	50	GND

Figure 10-9 : IP P1 Connector

The following signals have an on board pull-up resistor (4K7, 3.3V): WRITE#, IDSEL#, IOSEL#, INTSEL#, MEMSEL#.

The following signals have an on board pull-up resistor (4K7, 5V): ACK#, INTREQ0#, INTREQ1#, ERROR#, STROBE#, RSV0, RSV1, DMAREQ0#, DMAREQ1#, DMAACK#, DMAEND#.

DMA is not supported on the TVME8240A IP interface.

10.6.2.2 IP P2 Connector

For each IP slot the IP P2 connector signals (IP I/O lines) are routed directly to the appropriate pins of the 50P IP I/O ribbon cable connector.

The IP module connector type used is AMP/TYCO 173280-3.

The IP I/O connector type used is AMP/TYCO 281278-1.

10.6.3 PCI Expansion Connector

Pin	Signal		Pin	Signal
1	+3.3V		2	+3.3V
3	CLK		4	INTA#
5	GND		6	INTB#
7	PONRST#		8	INTC#
9	HRST#		10	INTD#
11	TDO		12	TDI
13	TMS		14	TCK
15	TRST#		16	PRSNT#
17	GNT#	GND	18	REQ#
19	+12V		20	-12V
21	PERR#		22	SERR#
23	LOCK#		24	SDONE
25	DEVSEL#		26	SBO#
27	GND		28	GND
29	TRDY#		30	IRDY#
31	STOP#		32	FRAME#
33	GND		34	GND
35	ACK64#		36	NC
37	REQ64#		38	NC
39	PAR		40	RST#
41	C/BE1#		42	C/BE0#
43	C/BE3#		44	C/BE2#
45	AD1		46	AD0
47	AD3		48	AD2
49	AD5		50	AD4
51	AD7		52	AD6
53	AD9		54	AD8
55	AD11		56	AD10
57	AD13	+5V	58	AD12
59	AD15		60	AD14
61	AD17		62	AD16
63	AD19		64	AD18
65	AD21		66	AD20

Pin	Signal		Pin	Signal
67	AD23		68	AD22
69	AD25		70	AD24
71	AD27		72	AD26
73	AD29		74	AD28
75	AD31		76	AD30
77	NC		78	NC
79	NC		80	NC
81	NC		82	NC
83	NC		84	NC
85	NC		86	NC
87	NC		88	NC
89	NC		90	NC
91	NC		92	NC
93	NC		94	NC
95	NC	GND	96	NC
97	NC		98	NC
99	NC		100	NC
101	NC		102	NC
103	NC		104	NC
105	NC		106	NC
107	NC		108	NC
109	NC		110	NC
111	NC		112	NC
113	NC		114	NC

Figure 10-10 : PCI Expansion Connector

The PCI Expansion Connector type used is AMP/TYCO 2-767004-4.

10.6.4 Serial Interface Connectors

10.6.4.1 Serial Port 1

Pin	RS232 Signal
1	DCD (input)
2	RXD (input)
3	TXD (output)
4	DTR (output)
5	GND
6	DSR (input)
7	RTS (output)
8	CTS (input)
9	RI (input)

Figure 10-11 : Serial Port 1 DB9 Male Connector

10.6.4.2 Serial Port 2

Pin	RS232 Mode Signal	RS422 Mode Signal
1	Reserved	RXD+ (input)
2	RXD (input)	RXD- (input)
3	TXD (output)	TXD- (output)
4	Reserved	TXD+ (output)
5	GND	GND
6	Reserved	Reserved
7	RTS (output)	Reserved
8	CTS (input)	Reserved
9	Reserved	Reserved

Figure 10-12 : Serial Port 2 DB9 Male Connector

The serial interface signals are also available on the VME P2 connector.

For each serial port only one connection scheme is allowed at a time, either via the VME P2 connector or via the DB9 connector at the front plate.

The DB9 connector type used is AMP/TYCO 747840-4.

Serial port 1 mode is always RS232. Serial port 2 mode is programmable for RS232 (default) or RS422 mode.

10.6.5 LAN RJ45 Connector

Pin	Signal
1	TD+
2	TD-
3	RD+
4	NC
5	NC
6	RD-
7	NC
8	NC

Figure 10-13 : LAN RJ45 Connector

The LAN RJ45 connector type used is HALO HFJ-2450E-L11.

11 Installation and Use Notes

11.1 NVRAM Real-Time Clock Control

The TVME8240A provides a M48T37 NVRAM / RTC device with a snaphat battery plugged on top. The snaphat battery provides power for the SRAM cells when the main power supply is off.

The TVME8240A is shipped with the snaphat battery installed on top of the M48T37 NVRAM device. The Real-Time Clock function of the M48T37 device is **turned-off by default**, to save battery energy.

If the M48T37 Real-Time Clock function has been turned-off (factory default), it must be enabled again, before using any other board resources (e.g. Ethernet).

The PMON "date" command can be used to enable the Real-Time Clock function.

Setup / Start the Real-Time Clock function:

(Required for normal operation)

```
PMON> date 200408101445.00
Tue Aug 10 14:45:00 2004
PMON> reboot
```

Stop the Real-Time Clock function :

(Recommended for TVME8240A board storage)

```
PMON> date -x
Clock is stopped...
PMON>
```

12 Technical Information

12.1 Processor

- Motorola MPC8245 Integrated Host PPC (300 MHz Core Frequency)
- Embedded Version MPC603e (G2) Processor Core
- Floating Point Unit
- DMA Controller
- 16 Kbyte I-Cache, 16 kbyte D-Cache
- Four cascadable 31 bit timer

12.2 Memory

- 64 Mbyte (TVME8240A-11) or 256 Mbyte (TVME8240A-21) 64 bit wide SDRAM (100 MHz)
- 8 Mbyte (TVME8240A-11) or 32 Mbyte (TVME8240A-21) 64 bit wide Flash Memory
- 32 Kbyte NVRAM (M48T37) with exchangeable battery
- 2 Mbyte 8 bit wide Boot-/Firmware- Flash

12.3 VME Interface

- Tundra Universe-II
- A16-A32 Master/Slave Address Modes; D08-D64 Master/Slave Data Transfer Modes
- RR/PRI VME bus Arbiter
- IRQ 1-7 (any of seven IRQs)
- System Controller Jumper (Yes, No, Auto Detect)
- Four Location Monitors
- DMA Controller
- VME Bus Error Interrupt

12.4 Ethernet Interface

- Intel 82551ER Fast Ethernet Controller (2x)
- PCI DMA support
- 10Base-T/100Base-TX Interface on RJ45 front-I/O connector
- 10Base-T/100Base-TX Interface on VME P2 back-I/O connector

12.5 Asynchronous Serial Interface

- Dual 16C850 compatible UART (1.8432 MHz clock-source)

- Port 1 : RS232 full modem, Port 2 : simple RS232 / RS422 (programmable)
- Max baud rate 115kbps
- Two DB9 front panel connectors
- VME P2 interface

12.6 PCI Expansion Connector

- 32 bit 33 MHz PCI Interface (114-pin connector)
- 5V PCI Signaling Voltage (PCI Expansion Board may drive 3.3V or 5V PCI signal levels, PCI Expansion Board must tolerate 5V PCI signal levels)
- Supports Motorola PMC-Span-002 and TEWS' IP-Span (TVME230)

12.7 IndustryPack Interface

12.7.1 Logic Interface

- Four single size / two double size IP slots
- Clock rate : 8 MHz or 32 MHz, selectable for each IP slot
- Data bus width : max 16 bit per slot / combined slot
- Spaces available for each single IP slot (A, B, C, D):
  - 128 byte I/O space (8/16 bit)
  - 64 byte ID space (8/16 bit)
  - 64 byte INT space (8/16 bit)
  - 8 Mbyte MEM space (8/16 bit)
  - 4 Mbyte MEM space (8 bit linear)

12.7.2 I/O Interface

- Four 50-pin planar connectors for ribbon cable front-I/O
- 1A max continuous dc current per IP I/O line

12.8 Power Requirements

The TVME8240A uses the +5V, +12V and -12V power supply from the VME P1 and P2 connectors as the main power supply.

+ 5V Supply:

On board load: 4A (max), (2A typ)

Additional load by optional I/O:

- PCI Expansion Connector

- IP interface (2A fused for IP slots A/B, 2A fused for IP slots C/D. So max. 2A for the total of IP slots A + B, max. 2A for the total of IP slots C + D)

+ 12V Supply: (not required for system function, only used by the 12V fuse status sensing logic)

On board load: 1mA (typ)

Additional load by optional I/O:

- PCI Expansion Connector (unfused)
- VME P2 Connector - LAN Power (1A fused)
- IP interface (Available on all IP slots, fused for a total of 2A, max. 1A per IP Slot)

- 12V Supply: (not required for system function, only used by the 12V fuse status sensing logic)

On board load: 4mA (typ)

Additional load by optional I/O:

- PCI Expansion Connector (Unfused)
- IP interface (Available on all IP slots, fused for a total of 2A, max. 1A per IP Slot)

On-board generated power supplies:

- +3.3V (generated using the +5V power supply)
- MPC8245 Core Power Supply (generated using the +5V power supply)
- FPGA Core Power Supply (generated using the +3.3V power supply)

Power Supply Pins on VME Connectors:

The VME P1 and P2 connectors are rated for 2A max. @ 20°C (appr. 1.5A max. @ 70°C) per pin.

For the +5V power supply there are 3-pins on the VME P1 connector and 3-pins on the VME P2 connector.

For the +12V power supply there is 1-pin on the VME P1 connector.

For the -12V power supply there is 1-pin on the VME P1 connector.

Along with the VME backplane used, this should be considered for the total power supply load (on board load plus optional I/O load).

12.9 Physical Data

12.9.1 MTBF

(Based on calculation)

TVME8240A Board Option	MTBF Value
-11/-21	174237h

Figure 12-1 : MTBF Data

12.9.2 Temperature

Operating Temperature Range: 0°C to 55°C (forced air cooling)

Non-Operating Temperature Range: -40°C to 85°C

12.9.3 Weight

TVME8240A Board Option	Weight
-11/-21	374 g

Figure 12-2 : Weight Data

12.9.4 Humidity

5% to 90% (non-condensing)

12.9.5 Form Factor

- Standard one slot 6U VME
- 3-row (a, b, c) VME P1 & P2 connectors

(optional PCI expansion board occupies an additional VME slot if installed)