The Embedded I/O Company

TEWS TECHNOLOGIES

TVME8300

Single Board Computer
with IndustryPack® Interface
(VME64x IP Back I/O)

Version 1.0

User Manual

Issue 1.4

September 2006

TEWS TECHNOLOGIES GmbH
Am Bahnhof 7
25469 Halstenbek, Germany
www.tews.com
Phone: +49-(0)4101-4058-0
Fax: +49-(0)4101-4058-19
e-mail: info@tews.com

TEWS TECHNOLOGIES LLC
9190 Double Diamond Parkway,
Suite 127, Reno, NV 89521, USA
www.tews.com
Phone: +1 (775) 850 5830
Fax: +1 (775) 201 0347
e-mail: usasales@tews.com

TVME8300

Single Board Computer with IndustryPack Interface (Back I/O)

Available Board Options :

TMVE8300-10

MPC8245 300 MHz, 64 MB SDRAM, 8 MB FLASH, Fast Ethernet, VME64x IP Back I/O

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	Initial Issue	October 2003
1.1	CPU Operating Frequency corrected	January 2004
1.2	Added “Installation and Use Notes” section / Corrected Memory Flash first instruction offset / Added Memory Flash Types / Updated Technical Information section	January 2005
1.3	Ultra-2 SCSI Controller / TVME8300-11 Board Option Obsolete.	June 2006
1.4	New address TEWS LLC	September 2006

Table of Contents

Table of Figures

1 Introduction

The TVME8300 is a standard 6U VME single slot Single Board Computer (SBC) card, using the Motorola MPC8245 Integrated Host PowerPC Processor.

The board provides four single IndustryPack (IP) slots (double-sized IP modules supported) running at 8 MHz or 32 MHz (programmable for each slot) with 16 bit port width. The IndustryPack I/O lines are available at the VME P2 and P0 connectors (conforming to the VME64x IP I/O Mapping).

Other supported I/O is: Fast Ethernet, dual UART (RS232) and a PCI Expansion Board connector.

On board memory is: 64 Mbyte 64 bit SDRAM, 8 Mbyte 64 bit FLASH, 8 KB 8 bit NVRAM.

1.1 Features

Processor	Motorola MPC8245 (300 MHz) PowerPC Integrated Host Processor (G2 Core, Timer, DMA, I2C, Interrupt Controller, Memory Controller, PCI Arbiter)
FLASH Memory	1 Mbyte 8 bit wide socket Boot FLASH 8 Mbyte 64 bit wide on board Memory FLASH
System Memory	64 Mbyte 64 bit wide synchronous DRAM (100 MHz)
VME Bus Interface	Tundra Universe-II VME / PCI Bridge
Ethernet Interface	Intel 82551ER Fast Ethernet Controller IEEE 802.3 10Base-T / 100Base-TX RJ45 Front I/O
IndustryPack Interface	Four single-sized / Two double-sized IndustryPack modules (16 bit) supported 8 MHz / 32 MHz clock rate selectable for each slot VME64x IndustryPack I/O mapping (back I/O) IP DMA not supported
PCI Expansion Capability	PMC-Span, IPspan support, 32 bit / 33 MHz PCI bus
NVRAM & RTC	8 Kbyte (M48T59 device)
Asynchronous Serial Interface	Two asynchronous RS232 ports (DB9)
Miscellaneous	RESET switch ABORT switch Front panel status indicators
Form Factor	Standard 6U VME (Monolithic VME64x Backplane with P1, P0, P2 connectors)

Figure 1-1 : Features TVME8300

1.2 Block Diagram

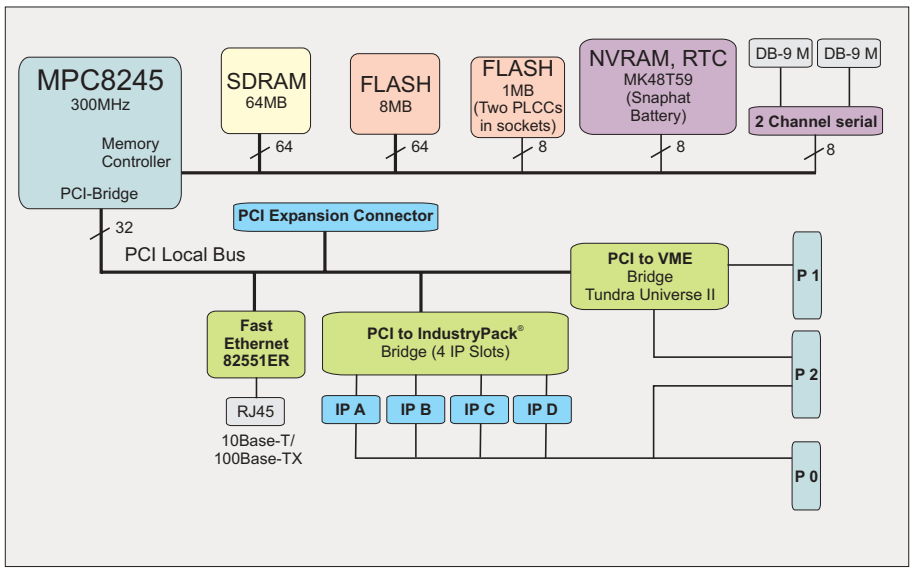

Figure 1-2 : Block diagram TVME8300

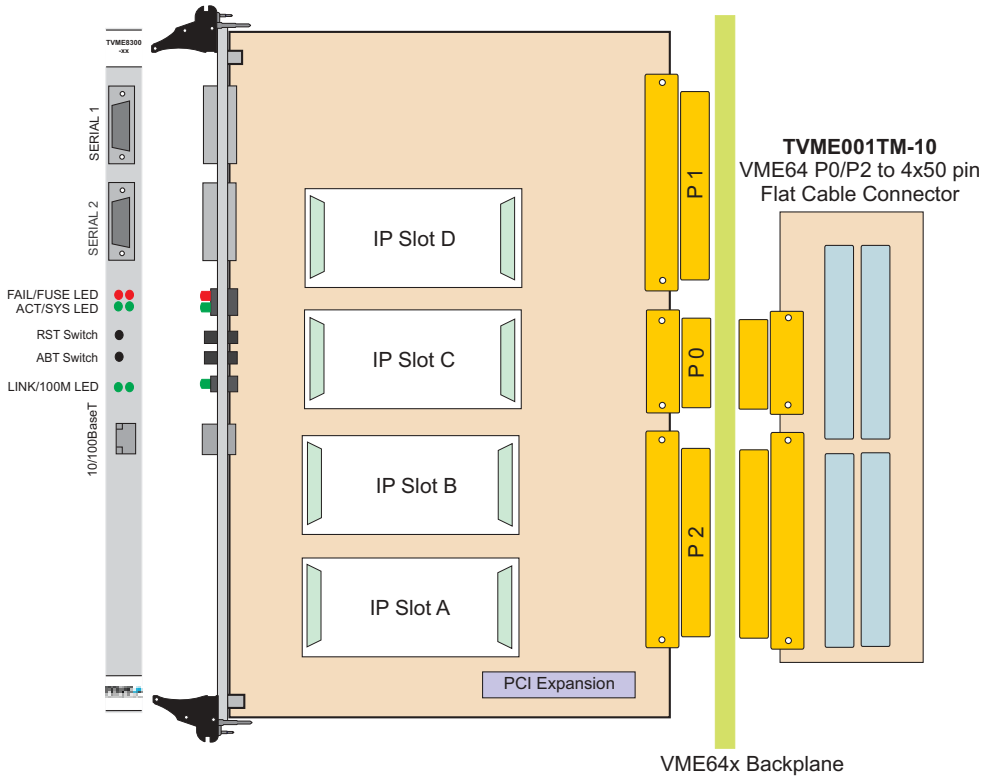

Figure 1-3 : Board Layout TVME8300

2 Description

2.1 Processor

The TVME8300 uses the Motorola MPC8245 Integrated Host PowerPC processor.

Please refer to the MPC8245 documentation for details.

2.2 Local Memory Bus

The TVME8300 provides the following devices on the MPC8245 local memory bus:

- Socket Boot FLASH (1 Mbyte, 8 bit wide)
- Board mounted Memory FLASH (8 Mbyte, 64 bit wide)
- SDRAM memory (64 Mbyte, 64 bit wide)
- NVRAM (8 Kbyte, 8 bit wide) / Real Time Clock / Watchdog (M48T59 compatible)
- 16550 compatible Dual-UART (8 bit wide)
- Utility Registers (8 bit wide)

2.2.1 FLASH Memory

The TVME8300 provides two banks of FLASH memory:

- Bank 0 consists of two 32-pin PLCC sockets each populated with a 512 K x 8 bit FLASH device for a total of 1 Mbyte 8 bit wide Boot FLASH memory
- Bank 1 consists of four 1 M x16 bit on board FLASH devices providing a total of 8 Mbyte 64 bit wide Memory FLASH memory

2.2.2 SDRAM Memory

The TVME8300 provides 64 Mbyte 64 bit wide SDRAM memory build with four 8 M x 16 bit SDRAM devices.

2.2.3 NVRAM / Real Time Clock

The TVME8300 uses a ST M48T59 compatible device to provide 8 Kbyte of non-volatile static RAM and real time clock.

The M48T59 device consists of two parts:

- A 28-pin 330mil SO device which contains the RTC, 8 Kbyte SRAM and sockets for the snaphat battery
- A snaphat battery that is placed on top of the device

Please refer to the M48T59 manual for details.

2.2.4 16550 compatible Dual UART

The TVME8300 uses the Exar XR16C2550 16550 compatible dual UART with a 1.8432 MHz clock-oscillator, providing two asynchronous serial ports.

Please refer to the XR16C2550 manual for details.

2.2.5 Utility Registers

The TVME8300 provides some additional registers for board control and status functions.

Please refer to the address map section of this manual for details.

2.3 PCI Bus

The TVME8300 implements a 32 bit, 33 MHz PCI bus.

The following devices are available on the TVME8300 PCI bus:

- MPC8245 Integrated Host PowerPC Processor (Motorola)
- Universe-II VME / PCI Bridge (Tundra)
- 82551ER Fast Ethernet Controller (Intel)
- PCI9030 PCI Target Chip (PLX Technology)
- Optional PCI Devices on PCI Expansion Connector (e.g. PMCspan, IPspan)
- The MPC8245 integrated PCI Arbiter is used for PCI bus arbitration.

Please see the PCI Bus Overview section for more details.

2.4 VME Bus Interface

The TVME8300 uses the Tundra Universe-II VME / PCI Bridge for the VME bus interface.

The Universe-II VME / PCI Bridge provides a 32 bit address / 32 bit data VME bus interface.

Please refer to the Universe-II documentation for details.

2.5 Ethernet Interface

The TVME8300 uses the Intel 82551ER Fast Ethernet Controller for the Ethernet interface.

An IEEE 802.3 10Base-T / 100Base-TX interface is available on an 8P RJ45 connector on the TVME8300 front panel.

Please refer to the 82551ER manual for details.

2.6 IndustryPack Interface

The TVME8300 uses the PLX Technology PCI9030 PCI Target Chip to access the IndustryPack interface on the PCI bus.

Four single-sized IP slots (A–D) are provided. Double-sized IP modules (16 bit) can be used on combined IP slots A/B or IP slots C/D. The clock rate for each IP slot can be programmed to 8 MHz or 32 MHz.

The IP I/O lines are available at the VME P2 and P0 connectors (conforming to the VME64x IP I/O mapping).

Please refer to the IP interface section in this manual for details.

2.7 PCI Expansion Interface

The TVME8300 provides a 114-pin PCI expansion connector for using existing VME PCI Expansion Boards (e.g. Motorola PMCspan or TEWS IPspan).

2.8 Asynchronous Serial Interface

The TVME8300 provides two asynchronous RS232 serial interface ports used with the on board Dual UART.

Both serial ports are available on DB9 male connectors on the TVME8300 front panel.

2.9 Interrupt Controller

The TVME8300 uses the MPC8245 Programmable Interrupt Controller (PIC) in the serial mode for all on board interrupt sources.

The following interrupt sources are available:

- Utility Register
- ABORT Switch
- 82551ER (Fast Ethernet Controller)
- PCI9030 (PCI Target Chip for IndustryPack Interface)
- Universe-II LINT0 (VME / PCI Bridge)
- Universe-II LINT1 (VME / PCI Bridge)
- Universe-II LINT2 (VME / PCI Bridge)
- Universe-II LINT3 (VME / PCI Bridge)
- PCI Expansion INTA (PCI Expansion Connector)
- PCI Expansion INTB (PCI Expansion Connector)
- PCI Expansion INTC (PCI Expansion Connector)
- PCI Expansion INTD (PCI Expansion Connector)
- Alarm / Watchdog (NVRAM / RTC Device)
- UART Channel A
- UART Channel B

Please see the MPC8245 PIC section for details on the serial interrupt source mapping.

2.10 Status Indicators (LEDs)

The TVME8300 provides six LED status indicators visible on the TVME8300 front panel.

The following LED indicators are available:

- VME Bus System Controller (Green)
- Board Activity (Green)
- Board Failure (Red)
- Fuse Status (Red)
- LAN Link Status (Green)
- LAN Speed Status (Green)

Please see the Board I/O section for more details.

2.11 Front Panel Switches

The TVME8300 provides 2 momentary switches available at the TVME8300 front panel.

The following switches are available:

- Reset (Board Reset)
- Abort (CPU Interrupt)

Please see the Board I/O section for more details.

3 Address Maps

The following address maps reflect MPC8245 configuration register settings done by board initialization software.

3.1 Address Map - Processor View

Processor Address		Size (Byte)	Description
Start	End		
0x0000_0000	0x03FF_FFFF	64M	SDRAM Memory (64 bit wide)
0x0400_0000	0x3FFF_FFFF	1G – 64M	Reserved
0x4000_0000	0x7FFF_FFFF	1G	Reserved
0x8000_0000	0xFCEF_FFFF	2G – 49M	PCI MEM Space
0xFCF0_0000	0xFCFF_FFFF	1M	MPC8245 EUMB
0xFD00_0000	0xFDFF_FFFF	16M	PCI MEM Space (0-based)
0xFE00_0000	0xFE00_FFFF	64K	PCI I/O Space (0-based)
0xFE01_0000	0xFE7F_FFFF	8M - 64K	Reserved
0xFE80_0000	0xFEBF_FFFF	4M	PCI I/O Space (0-based)
0xFEC0_0000	0xFEDF_FFFF	2M	Configuration Address Register
0xFEE0_0000	0xFEEF_FFFF	1M	Configuration Data Register
0xFEF0_0000	0xFEFF_FFFF	1M	PCI Interrupt Acknowledge
0xFF00_0000	0xFF7F_FFFF	8M	Memory FLASH (64 bit wide)
0xFF80_0000	0xFFDF_FFFF	6M	Reserved
0xFFE0_0000	0xFFEF_FFFF	1M	Peripheral Devices (8 bit wide)
0xFFF0_0000	0xFFFF_FFFF	1M	Boot FLASH (8 bit wide)

Figure 3-1 : Address Map – Processor View

Device	Read	Write
SDRAM	All	All
Memory FLASH	All	64 bit Only
Peripheral Devices	8 bit Only	8 bit Only
Boot FLASH	All	8 bit Only

Figure 3-2 : Supported Transfer Sizes

Processor Address		Translated PCI Address		PCI Space
Start	End	Start	End	
0x8000_0000	0xFCEF_FFFF	0x8000_0000	0xFCEF_FFFF	MEM
0xFD00_0000	0xFDFF_FFFF	0x0000_0000	0x00FF_FFFF	MEM
0xFE00_0000	0xFE00_FFFF	0x0000_0000	0x0000_FFFF	I/O
0xFE80_0000	0xFEBF_FFFF	0x0080_0000	0x00BF_FFFF	I/O

Figure 3-3 : PCI Address Translation

3.2 Address Map – PCI Memory Master View

PCI Memory Address		Size (Byte)	Description
Start	End		
0x0000_0000	0x03FF_FFFF	64M	SDRAM Memory (64 bit wide)
0x0400_0000	0x3FFF_FFFF	1G – 64M	Reserved
0x4000_0000	0x7FFF_FFFF	1G	Reserved
0x8000_0000	0xFCEF_FFFF	2G – 49M	PCI Memory Space
0xFCF0_0000	0xFCF0_0FFF	4K	PCI accessible MPC8245 EUMB
0xFCF0_1000	0xFCFF_FFFF	1M - 4K	Reserved
0xFD00_0000	0xFDFF_FFFF	16M	SDRAM Memory (0-Based)
0xFE00_0000	0xFEFF_FFFF	16M	Reserved
0xFF00_0000	0xFF7F_FFFF	8M	Memory FLASH (64 bit wide)
0xFF80_0000	0xFFDF_FFFF	6M	Reserved
0xFFE0_0000	0xFFEF_FFFF	1M	Peripheral Devices (8 bit wide)
0xFFF0_0000	0xFFFF_FFFF	1M	Boot FLASH (8 bit wide)

Figure 3-4 : Address Map – PCI Memory Master View

On the TVME8300 the MPC8245 responds as a target to PCI Memory cycles for accessing SDRAM, PCI accessible MPC8245 EUMB, Memory FLASH, Peripheral Devices and Boot FLASH.

3.3 Address Map – PCI I/O Master View

PCI I/O Address		Size (Byte)	Description
Start	End		
0x0000_0000	0x0000_FFFF	64K	PCI I/O Space
0x0001_0000	0x007F_FFFF	8M – 64K	Reserved
0x0080_0000	0x00BF_FFFF	4M	PCI I/O Space
0x00C0_0000	0xFFFF_FFFF	4G – 12M	Reserved

Figure 3-5 : Address Map – PCI I/O Master View

The MPC8245 does not respond as a target to PCI I/O cycles.

3.4 Address Map – Peripheral Devices Detail

Address		Size (Byte)	Description
Start	End		
0xFFE0_0000	0xFFE0_1FFF	8K	NVRAM / RTC
0xFFE0_2000	0xFFE3_FFFF	256K – 8K	Reserved
0xFFE4_0000	0xFFE4_0003	4	UTILITY REG
0xFFE4_0004	0xFFE7_FFFF	256K – 4	Reserved
0xFFE8_0000	0xFFE8_0007	8	UART CH A
0xFFE8_0008	0xFFE8_000F	8	UART CH B
0xFFE8_0010	0xFFEF_FFFF	512K -16	Reserved

Figure 3-6 : Address Map – Peripheral Devices Detail

For read or write accesses to the Peripheral Devices only 8 bit (byte) transfer sizes are allowed.

For the NVRAM / RTC register map please refer to the M48T59 device documentation.

For the UART register map please refer to the XR16C2550 documentation.

3.5 Address Map – Utility Register Detail

Address	Size (Byte)	Register Name
0xFFE4_0000	1	CONTROL
0xFFE4_0001	1	STATUS
0xFFE4_0002	1	INTERRUPT
0xFFE4_0003	1	LED
0xFFE4_0004	1	JUMPER
0xFFE4_0005	1	FUSE
0xFFE4_0006	1	Reserved
0xFFE4_0007	1	Reserved

Figure 3-7 : Address Map – Utility Register Detail

3.5.1 Control Register

Bit	Name	Access	Reset	Function
0 (MSB)	BOARD_RST	R/W	0	0: Normal Board Operation 1: Assert Board Reset
1	I2C_EEP_WE	R/W	0	0: I2C EEPROM Writes Disabled 1: I2C EEPROM Writes Enabled
2	MEM_FLASH_WE	R/W	0	0: Memory FLASH Writes Disabled 1: Memory FLASH Writes Enabled
3	BOOT_FLASH_WE	R/W	0	0: Boot FLASH Writes Disabled 1: Boot FLASH Writes Enabled
4	FUSE_INT_EN	R/W	0	0: Fuse Interrupt Disabled 1: Fuse Interrupt Enabled
5	Reserved	-	-	Write as '0' Undefined for Reads
6				
7 (LSB)				

Figure 3-8 : Control Register

3.5.2 Status Register

Bit	Name	Access	Reset	Function
0 (MSB)	BOOT_JMP	R	-	0: Boot Jumper Open 1: Boot Jumper Closed
1	PCI_EXP_PRSNT	R	-	0: PCI Expansion Board Not Present 1: PCI Expansion Board Present
2	FPGA_DONE	R	-	0: IP FPGA Configuration Not Done 1: IP FPGA Configuration Done
3	ABORT_SW	R	-	0: Abort Switch Not Active 1: Abort Switch Active
4	FUSE	R	-	0: All Fuses OK 1: At least one Fuse triggered
5	SYSCON	R	-	0: Not VME System Controller 1: VME System Controller
6	Reserved	-	-	Undefined for Reads
7 (LSB)				

Figure 3-9 : Status Register

Board initialization software should verify successful IP FPGA configuration.

All board fuses are recoverable fuses.

3.5.3 Interrupt Register

Bit	Name	Access	Reset	Function
0 (MSB)	USR_INT	R/W	0	0: No User Interrupt / Clear Interrupt 1: Active User Interrupt
1	FUSE_INT	R/C	0	Read : 0: No Fuse Interrupt 1: Active Fuse Interrupt Write ‘1’ to clear interrupt
2	Reserved	-	-	Write as '0' Undefined for Reads
3				
4				
5				
6				
7 (LSB)				

Figure 3-10: Interrupt Register

3.5.4 LED Register

Bit	Name	Access	Reset	Function
0 (MSB)	FAIL_LED	R/W	0	0: Set Fail LED OFF 1: Set Fail LED ON
1	Reserved	-	-	Write as '0' Undefined for Reads
2				
3				
4				
5				
6				
7 (LSB)				

Figure 3-11: LED Register

3.5.5 Jumper Register

Bit	Name	Access	Reset	Function
0 (MSB)	JMP_0	R	-	0: Jumper 0 Open 1: Jumper 0 Closed
1	JMP_1	R	-	0: Jumper 1 Open 1: Jumper 1 Closed
2	JMP_2	R	-	0: Jumper 2 Open 1: Jumper 2 Closed
3	JMP_3	R	-	0: Jumper 3 Open 1: Jumper 3 Closed
4	Reserved	-	-	Undefined for Reads
5				
6				
7 (LSB)				

Figure 3-12: Jumper Register

3.5.6 Fuse Register

Bit	Name	Access	Reset	Function
0 (MSB)	FUSE_IPAB5	R	-	0 : Fuse IP Slots A/B 5V OK 1 : Fuse IP Slots A/B 5V Triggered
1	FUSE_IPCD5	R	-	0 : Fuse IP Slots C/D 5V OK 1 : Fuse IP Slots C/D 5V Triggered
2	FUSE_IP12P	R	-	0 : Fuse IP Slots +12V OK 1 : Fuse IP Slots +12V Triggered
3	FUSE_IP12N	R	-	0 : Fuse IP Slots -12V OK 1 : Fuse IP Slots -12V Triggered
4	Reserved	-	-	Undefined for Reads
5	Reserved	-	-	Undefined for Reads
6				
7 (LSB)				

Figure 3-13: Fuse Register

All board fuses are recoverable fuses.

3.5.7 Utility Register Interrupts

There are two interrupt sources under Utility Registers control. Both interrupt sources are mapped to a single Utility Interrupt Source which is part of the MPC8245 PIC Serial Interrupt Map. When any bit in the Interrupt Register is set, the Utility Interrupt is active.

- User Interrupt

  To assert a user interrupt, set the USR_INT bit in the Interrupt Register. Write ‘0’ to the USR_INT bit to clear the user interrupt.

- Fuse Interrupt

  The FUSE_INT_EN bit in the Control Register controls whether an active fuse status is latched into the FUSE_INT bit in the Interrupt Register. Write ‘1’ to the FUSE_INT bit in the Interrupt Register to clear a latched fuse interrupt. Disabling the fuse interrupt does also clear the fuse interrupt.

  The fuse status register bits reflect the actual fuse status (unlatched). So when the fuse recovers before the interrupt service routine reads the Fuse Status Register, it is possible that the interrupt service routine finds all fuse status bits clear.

  If a fuse interrupt occurs, this should be indicated to the system and the fuse interrupt should be disabled (otherwise there may be permanent fuse interrupts as long as the overload situation exists).

4 MPC8245

The TVME8300 uses the MPC8245 in host mode with address map B.

The MPC8245 processor and peripheral logic are configured to operate in big endian mode.

4.1 Configuration Registers

Setting up the MPC8245 Configuration Registers is scope of the board initialization software.

Configuration Register settings are shown for information only and may not reflect the settings for the actual revision of the board initialization software.

4.1.1 Configuration Register Access

The MPC8245 Configuration Registers are accessed in two steps:

1. A 32 bit register address 0x8000_00nn is written to the CONFIG_ADDR port at 0xFEC0_0000, where nn is the (word-aligned) register offset.
2. Data is accessed at the CONFIG_DATA port at 0xFEE0_000m, where m is the offset within the word-aligned address (depending on transfer size).

Data can be accessed multiple times at the CONFIG_DATA port until the CONFIG_ADDR port value is changed.

All of the MPC8245 Configuration Registers are intrinsically little endian. Therefore all of the following Configuration Register settings are shown in little endian order.

Since on the TVME8300 the MPC8245 processor and peripheral logic operates in big endian mode, software must either use byte reversed load / store instructions or byte-swap the values for the CONFIG_ADDR and CONFIG_DATA port access.

E.g. for reading the Device ID Register (offset 0x02) one should write 0x0000_0080 (0x00 is the word-aligned offset for 0x02) to 0xFEC0_0000 and read the half-word 0x0600 at 0xFEE0_0002.

E.g. for setting the Output Driver Control Register (offset 0x73) one should write 0x7000_0080 (0x70 is the word-aligned offset for 0x73) to 0xFEC0_0000 and write the byte 0xD5 to 0xFEE0_0003.

E.g. for setting the EUMBBAR Register (offset 0x78) to 0xFCF0_0000 one should write 0x78000080 to 0xFEC0_0000 and write the word 0x0000F0FC to 0xFEE0_0000.

4.1.2 Configuration Register Settings

Register Offset	Register Description	Size (Byte)	Access Type	Setting
0x00	Vendor ID	2	R	0x1057
0x02	Device ID	2	R	0x0006
0x04	PCI Command Register	2	R/W	0x0006
0x06	PCI Status Register	2	R/C	*status*
0x08	Revision ID	1	R	0x14
0x09	Standard Programming Interface	1	R	0x00
0x0A	Subclass Code	1	R	0x00
0x0B	Class Code	1	R	0x06
0x0C	Cache Line Size	1	R/W	0x00
0x0D	Latency Timer	1	R/W	-
0x0E	Header Type	1	R	0x00
0x0F	BIST Control	1	R	0x00
0x10	Local Memory Base Address Register 0	4	R/W	*reset_default*
0x14	Peripheral Control Status Register Base Address Register	4	R/W	0xFCF0_0000
0x18	Local Memory Base Address Register 1	4	R/W	*reset_default*
0x2C	Subsystem Vendor ID	2	R/W	0x0000
0x2E	Subsystem ID	2	R/W	0x0000
0x30	Expansion ROM Base Address	4	R	0x0000_0000
0x3C	Interrupt Line	1	R/W	0x00
0x3D	Interrupt Pin	1	R	0x01
0x3E	MIN GNT	1	R	0x00
0x3F	MAX LAT	1	R	0x00
0x40	Bus Number	1	R/W	0x00
0x41	Subordinate Bus Number	1	R/W	0x00
0x44	PCI General Control Register	2	R/W	0x0000
0x46	PCI Arbiter Control Register	2	R/W	0x8400
0x70	Power Management Configuration Register 1	2	R/W	0xC001
0x72	Power Management Configuration Register 2	1	R/W	0x20
0x73	Output Driver Control Register	1	R/W	0xD5
0x74	Clock Driver Control Register	2	R/W	0x0000
0x76	Misc. I/O Control Register 1	1	R/W	0x00
0x77	Misc. I/O Control Register 2	1	R/W	0x30

Register Offset	Register Description	Size (Byte)	Access Type	Setting
0x78	Embedded Utilities Memory Block Base Address (EUMBBAR)	4	R/W	0xFCF0_0000
0x80, 0x84	Memory Starting Address Registers	4	R/W	0x4040_4000, 0x40404040
0x88, 0x8C	Extended Memory Starting Address Registers	4	R/W	0x0000_0000, 0x0000_0000
0x90, 0x94	Memory Ending Address Registers	4	R/W	0x4F4F_4F3F, 0x4F4F_4F4F
0x98, 0x9C	Extended Memory Ending Address Registers	4	R/W	0x0000_0000, 0x0000_0000
0xA0	Memory Bank Enable Register	1	R/W	0x01
0xA3	Page Mode Register	1	R/W	0x00
0xA8	Processor Interface Configuration Register 1	4	R/W	0x0014_1A98
0xAC	Processor Interface Configuration Register 2	4	R/W	0x2000_0600
0xB8	ECC Single Bit Error Counter Register	1	R/W	*status*
0xB9	ECC Single Bit Error Trigger Register	1	R/W	*reset_default*
0xC0	Error Enabling Register 1	1	R/W	*reset_default*
0xC1	Error Detection Register 1	1	R/C	*status*
0xC3	Processor Internal Bus Error Status Register	1	R/C	*status*
0xC4	Error Enabling Register 2	1	R/W	*reset_default*
0xC5	Error Detection Register 2	1	R/C	*status*
0xC7	PCI Bus Error Status Register	1	R/C	*status*
0xC8	Processor/PCI Error Address Register	4	R	*status*
0xD0	Extended ROM Configuration Register 1	4	R/W	*reset_default*
0xD4	Extended ROM Configuration Register 2	4	R/W	*reset_default*
0xD8	Extended ROM Configuration Register 3	4	R/W	*reset_default*
0xDC	Extended ROM Configuration Register 4	4	R/W	*reset_default*
0xE0	Address Map B Options Register (AMBOR)	1	R/W	0xC0
0xE2	PLL Configuration Register	1	R	0x08
0xF0	Memory Control Configuration Register 1 (MCCR1)	4	R/W	0x03E8_0000
0xF4	Memory Control	4	R/W	0x0A40_1820

Register Offset	Register Description	Size (Byte)	Access Type	Setting
	Configuration Register 2 (MCCR2)			
0xF8	Memory Control Configuration Register 3 (MCCR3)	4	R/W	0x0700_0000
0xFC	Memory Control Configuration Register 4 (MCCR4)	4	R/W	0x2610_2220

Figure 4-1 : MPC8245 Configuration Register Settings

Board initialization software notes:

The MEMGO bit in the MCCR1 register (offset 0xF0) must not be set until all other memory configuration parameters have been appropriately configured.

The DLL_RESET bit in the AMBOR register (offset 0xE0) must be explicitly set and then cleared by software during initialization.

4.2 Programmable Interrupt Controller (PIC)

The TVME8300 uses the MPC8245 Programmable Interrupt Controller (PIC) in serial mode as the board interrupt controller.

4.2.1 PIC Serial Interrupt Assignment

The following interrupt sources are available and mapped to the PIC serial interrupt channel:

PIC Serial Interrupt No.	Edge / Level	Active Polarity	Interrupt Source
0	Level	Low	Utility Register
1	Edge	Low	ABORT Switch
2	Level	Low	82551ER (Ethernet)
3	Level	Low	Reserved
4	Level	Low	PCI9030 (IPAC)
5	Level	Low	Universe-II LINT0 (VME)
6	Level	Low	Universe-II LINT1 (VME)
7	Level	Low	Universe-II LINT2 (VME)
8	Level	Low	Universe-II LINT3 (VME)
9	Level	Low	PCI Expansion INTA (EXP)
10	Level	Low	PCI Expansion INTB (EXP)
11	Level	Low	PCI Expansion INTC (EXP)
12	Level	Low	PCI Expansion INTD (EXP)
13	Level	Low	Alarm / Watchdog (NVRAM)
14	Level	Low	UART Channel A (Serial A)
15	Level	Low	UART Channel B (Serial B)

Figure 4-2 : PIC Serial Interrupt Assignment

4.2.2 PIC Register Access

The PIC Registers are part of the MPC8245 Embedded Utility Memory Block (EUMB).

The EUMB base address is set in the EUMBBAR Register.

For the TVME8300 memory map the EUMB base address is set to 0xFCF0_0000.

4.2.3 PIC Register Settings

4.2.3.1 Global Configuration Register (GCR)

Offset from EUMBBAR: 0x4_1020

The mode bit in the GCR must be set for PIC mixed mode operation.

4.2.3.2 Interrupt Configuration Register (ICR)

Offset from EUMBBAR: 0x4_1030

The ICR clock ratio field should be set to 0x2 for optimized interrupt performance.

The ICR SIE bit must be set to enable Serial Interrupt Mode.

4.2.3.3 Serial Interrupt Vector / Priority Registers (SVPR)

The polarity and sense bits in the SVPRs must be configured accordingly to the PIC Serial Interrupt Assignment table.

4.2.4 PIC Register Programming

The PIC Programming Guidelines from the MPC8245 manual should be followed.

4.3 I2C Bus

The TVME8300 provides an on board I2C EEPROM for board specific data.

4.3.1 I2C EEPROM

EEPROM Offset	Description	Content
0x00	Check sum	See note below
0x01	Number Of Valid Bytes Following	e.g. 0x06
0x02	Board Type (High Byte)	0x206C for TVME8300
0x03	Board Type (Low Byte)	
0x04	Board Option (High Byte)	e.g. 0x000A for TVME8300-10
0x05	Board Option (Low Byte)	
0x06	Board Version (Major)	V <major>.<minor> e.g. 0x0100 = V1.0
0x07	Board Version (Minor)	
0x08 ... 0x0F	Factory Reserved	
0x10 ... 0xFF	Reserved	

Figure 4-3 : I2C EEPROM Content

The address of the on board I2C EEPROM is 0b000.

Writes to the on board I2C EEPROM must be enabled in the Utility Control Register.

The check sum is the 2's-complement of the lower byte of the sum of all used locations of the I2C EEPROM, except the check sum byte.

5 FLASH Programming

5.1 8 bit Wide Socket Boot FLASH

The TVME8300 provides 1 MByte of 8 bit wide socket Boot FLASH using two 512 K x 8 bit 32-pin PLCC FLASH devices.

The Boot FLASH address range is 0xFFF0_0000 to 0xFFFF_FFFF.

Boot FLASH Socket XU1 is for the lower 512 Kbyte address range (0xFFF0_0000 to 0xFFF7_FFFF).

Boot FLASH Socket XU2 is for the upper 512 Kbyte address range (0xFFF8_0000 to 0xFFFF_FFFF).

For writes to the Boot FLASH byte (8 bit) transfer sizes must be used.

Writes to the Boot FLASH must be enabled in the Utility Control Register.

The 8 bit wide socket Boot FLASH (Socket XU1) must always be installed and provide the board initialization code at the system reset vector (0xFFF0_0100).

Command Sequence	Cycles	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	RA	RD										
Reset	1	Base+ 0x000	0xF0										
Auto Select	4	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	Base+ 0x555	0x90	Base+ 0x000	MID				
								Base+ 0x001	DID				
Write	4	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	Base+ 0x555	0xA0	WA	WD				
Chip Erase	6	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	Base+ 0x555	0x80	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	Base+ 0x555	0x10
Sector Erase	6	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	Base+ 0x555	0x80	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	SAx	0x30

Figure 5-1 : Boot FLASH Command Cycles

All Boot FLASH command cycles are write cycles except the 1st cycle of the Read command and the 4th cycle of the Auto Select command which are read cycles.

The base address for the lower 512 Kbyte Boot FLASH device is 0xFFF0_0000.

The base address for the upper 512 Kbyte Boot FLASH device is 0xFFF8_0000.

For Write commands poll for RD = WD from RA = WA after the 4th cycle.

For Erase commands poll for RD = 0xFF from the Boot FLASH device base address for Chip Erase or from SAx for Sector Erase after the 6th cycle.

Symbols:

DID = Device ID, MID = Manufacturer ID, RA = Read Address, RD = Read Data,

SA = Sector Address, WA = Write Address, WD = Write Data

Manufacturer	Device	Manufacture ID	Device ID
AMD	29F040B	0x01	0xA4
ST	29F040B	0x20	0xE2

Figure 5-2 : Boot FLASH Auto Select Codes

Sector	Sector Size (Byte)	Sector Address Range
SA0	64K	0xFFF0_0000 - 0xFFF0_FFFF
SA1	64K	0xFFF1_0000 - 0xFFF1_FFFF
SA2	64K	0xFFF2_0000 - 0xFFF2_FFFF
SA3	64K	0xFFF3_0000 - 0xFFF3_FFFF
SA4	64K	0xFFF4_0000 - 0xFFF4_FFFF
SA5	64K	0xFFF5_0000 - 0xFFF5_FFFF
SA6	64K	0xFFF6_0000 - 0xFFF6_FFFF
SA7	64K	0xFFF7_0000 - 0xFFF7_FFFF
SA8	64K	0xFFF8_0000 - 0xFFF8_FFFF
SA9	64K	0xFFF9_0000 - 0xFFF9_FFFF
SA10	64K	0xFFFA_0000 - 0xFFFA_FFFF
SA11	64K	0xFFFB_0000 - 0xFFFB_FFFF
SA12	64K	0xFFFC_0000 - 0xFFFC_FFFF
SA13	64K	0xFFFD_0000 - 0xFFFD_FFFF
SA14	64K	0xFFFE_0000 - 0xFFFE_FFFF
SA15	64K	0xFFFF_0000 - 0xFFFF_FFFF

Figure 5-3 : Boot FLASH Sector Map

5.2 64 bit Wide On Board Memory FLASH

The TVME8300 provides 8 Mbyte of 64 bit wide board mounted Memory FLASH using four 1 M x 16 bit FLASH devices.

The Memory FLASH address range is 0xFF00_0000 to 0xFF7F_FFFF.

For writes to the Memory FLASH double-word (64 bit) transfer sizes must be used.

Writes to the Memory FLASH must be enabled in the Utility Control Register.

For 64 bit writes to the Memory Flash, the processor may issue a single-beat 64 bit write, using a caching-inhibited stfd (store floating point double), with the data in a Floating Point Register (FPR).

Cmd.-Seq.	#Cyc	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	RA	RD										
Reset	1	Base + 0x0_0000	0x00F000F0 00F000F0										
Auto Select	4	Base + 0x2_AAA8	0x00AA00AA 00AA00AA	Base + 0x1_5550	0x00550055 00550055	Base + 0x2_AAA8	0x00900090 00900090	Base + 0x0_0000	MID				
								Base + 0x0_0008	DID				
Write	4	Base + 0x2_AAA8	0x00AA00AA 00AA00A	Base + 0x1_5550	0x00550055 00550055	Base + 0x2_AAA8	0x00A000A0 00A000A0	WA	WD				
Chip Erase	6	Base + 0x2_AAA8	0x00AA00AA 00AA00A	Base + 0x1_5550	0x00550055 00550055	Base + 0x2_AAA8	0x00800080 00800080	Base + 0x2_AAA8	0x00AA00AA 00AA00A	Base + 0x1_5550	0x00550055 00550055	Base + 0x2_AAA8	0x00100010 00100010
Sector Erase	6	Base + 0x2_AAA8	0x00AA00AA 00AA00A	Base + 0x1_5550	0x00550055 00550055	Base + 0x2_AAA8	0x00800080 00800080	Base + 0x2_AAA8	0x00AA00AA 00AA00A	Base + 0x1_5550	0x00550055 00550055	SAx	0x00300030 00300030

Figure 5-4 : Memory FLASH Command Cycles

All the Memory FLASH command cycles are write cycles except the 1st cycle of the Read command and the 4th cycle of the Auto Select command which are read cycles.

The Memory FLASH base address is 0xFF00_0000.

For Write commands poll for RD = WD from RA = WA after the 4th cycle.

For Erase commands poll for RD = 0xFFFFFFFFFFFFFFFF from the Memory FLASH base address for Chip Erase or from SAx for Sector Erase after the 6th cycle.

Symbols:

DID = Device ID, MID = Manufacturer ID, RA = Read Address, RD = Read Data,

SA = Sector Address, WA = Write Address, WD = Write Data

Manufacturer	Device	Manufacturer ID	Device ID
SST	39VF160	0x00BF00BF00BF00BF	0x2782278227822782
SST	39VF1601	0x00BF00BF00BF00BF	0x234B234B234B234B
SST	39VF1602	0x00BF00BF00BF00BF	0x234A234A234A234A

Figure 5-5 : Memory FLASH Auto Select Codes

Sector	Sector Size (Byte)	Sector Address Range
SST 39xF160x (Uniform)		
SA0	16K	0xFF00_0000 - 0xFF00_3FFF
SA1	16K	0xFF00_4000 - 0xFF00_7FFF
SA2	16K	0xFF00_8000 - 0xFF00_BFFF
SA3	16K	0xFF00_C000 - 0xFF00_FFFF
SA4	16K	0xFF01_0000 - 0xFF01_3FFF
…	…	…
SA511	16K	0xFF7F_C000 - 0xFF7F_FFFF

Figure 5-6 : Memory FLASH Sector Map

6 VME Bus Interface

The Tundra Universe-II VME / PCI bridge is used as the TVME8300 VME / PCI bridge.

The Universe-II is accessible on both the VME bus and the TVME8300 PCI bus (device number 13).

Please refer to the Universe-II manual for a detailed description of the Universe-II VME / PCI bridge.

6.1 Universe-II PCI Header

Offset	PCI Configuration Register				Setting
	31 - 24	23 - 16	15 - 08	07 - 00	
0x00	Device ID		Vendor ID		0x0000_10E3
0x04	Status		Command		0x0200_0007
0x08	Class Code			Revision ID	0x0680_0002
0x0C	Reserved	Header	Latency	Cache Line	0x0000_xx00
0x10	PCI Base Address 0 (Configuration Register I/O Mapped)				0xFFFF_F001(1) (4 Kbyte)
0x14	PCI Base Address 1 (Configuration Register Memory Mapped)				0xFFFF_F000(1) (4 Kbyte)
0x18	PCI Unimplemented				0x0000_0000
0x1C	PCI Unimplemented				0x0000_0000
0x20	PCI Unimplemented				0x0000_0000
0x24	PCI Unimplemented				0x0000_0000
0x28	PCI Reserved				0x0000_0000
0x2C	PCI Reserved				0x0000_0000
0x30	PCI Unimplemented				0x0000_0000
0x34	PCI Reserved				0x0000_0000
0x38	PCI Reserved				0x0000_0000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	0x0003_0100

(1) Read back value after writing all 1's.

Figure 6-1 : Universe-II PCI Header

6.2 Universe-II Power-Up Options

The TVME8300 uses the default Universe-II power-up option configuration.

Please see the Universe-II user manual for details.

6.3 Universe-II Reset Signals

The Universe-II PWRRST# input is controlled by a power-up reset logic.

The Universe-II RST# input is connected to the PCI reset signal.

If the Universe-II is the VME bus System Controller, a board reset will also trigger the Universe-II VMERST# input, asserting a VME bus System Reset.

If the Universe-II is not the VME bus System Controller, a VME bus System Reset will also trigger a TVME8300 board reset (using the Universe-II LRST# output).

The Universe-II VRSYSRST# and VXSYSRST# signals are mapped to the VME bus SYSRST# signal.

Please see the Universe-II user manual for details.

6.4 Universe-II Interrupts

The Universe-II LINT#[4:7] interrupt pins are not used.

The Universe-II LINT#[0:3] interrupt pins are used as outputs and are mapped to the serial interrupts no. [5:8] of the MPC8245 PIC.

6.5 Universe-II VME Bus Modes

The Universe-II supports VME bus A32/24/16 master and slave address modes and D32/16/8 master and slave data transfer modes.

Please see the Universe-II user manual for details.

7 Ethernet Interface

The Intel 82551ER Fast Ethernet Controller is used for the TVME8300 Ethernet interface.

The 82551ER is accessible on the TVME8300 PCI bus (device number 14).

The 82551ER INT# interrupt output is mapped to serial channel no. 2 of the MPC8245 PIC.

The 82551ER is reset by a PCI reset.

Please refer to the 82551ER manual for a detailed description of the 82551ER Fast Ethernet Controller.

7.1 82551ER PCI Header

Offset	PCI Configuration Register				Setting
	31 - 24	23 - 16	15 - 08	07 - 00	
0x00	Device ID		Vendor ID		0x1209_8086
0x04	Status		Command		0x0290_0007
0x08	Class Code			Revision ID	0x0200_00xx
0x0C	BIST	Header	Latency	Cache Line	0x0000_xx00
0x10	PCI Base Address 0 (Memory Mapped Configuration Register)				0xFFFF_F000(1) (4 Kbyte)
0x14	PCI Base Address 0 (I/O Mapped Configuration Register)				0xFFFF_FF81(1) (64 Byte)
0x18	PCI Base Address 0 (Memory Mapped FLASH Space)				0xFFFE_0000(1) (128 Kbyte)
0x1C	Reserved				0x0000_0000
0x20	Reserved				0x0000_0000
0x24	Reserved				0x0000_0000
0x28	Reserved				0x0000_0000
0x2C	Subsystem ID		Subsystem Vendor ID		0x1209_8086
0x30	Expansion ROM PCI Base Address				0x0000_0000
0x34	Reserved			Cap. Pointer	0x0000_00DC
0x38	Reserved				0x0000_0000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	0xxx08_0100
0xDC	Power Management Cap.		Next Cap.	Cap. ID	0x7E22_0001
0xE0	Reserved	Data	Power Management CSR		0x4B00_4000

(1) Read back Value after writing all 1's.

Figure 7-1 : 82551ER PCI Header

7.2 82551ER Configuration EEPROM

EEPROM Address (16 bit Address)	Description	
	Bits 15 - 8	**Bits 07 - 00**
0x00	Ethernet Address Byte 1	Ethernet Address Byte 0
	0x01	0x00
0x01	Ethernet Address Byte 3	Ethernet Address Byte 2
	xx	0x06
0x02	Ethernet Address Byte 5	Ethernet Address Byte 4
	zz	*yy*
0x0A	EEPROM ID	
	0x4840	
0x0B	Subsystem ID	
	0x1209	
0x0C	Subsystem Vendor ID	
	0x8086	
0x0D	Reserved	
	Tbd.	
0x0E	Reserved	
	Tbd.	
0x0F	Reserved	
	Tbd.	
0x10 - 0x3E	Reserved	
	0xFFFF	
0x3F	EEPROM Checksum	
	variant	

Figure 7-2 : 82551ER Configuration EEPROM Settings

7.3 Media Capabilities

IEEE 802.3 10Base-T / 100Base-TX interface on the RJ45 front panel connector.

8 IP Interface

The TVME8300 IP interface is accessible in the PCI Memory space.

The PLX Technology PCI9030 PCI Target Chip is used as the PCI target chip device for accessing the IP interface.

8.1 PCI9030 PCI Target Chip

The PCI9030 provides four local spaces 0:3 that are used for accessing the TVME8300 IP interface.

The PCI9030 is accessible on the TVME8300 PCI bus (device number 16).

The PCI9030 INT# interrupt output is mapped to serial channel no. 4 of the MPC8245 PIC.

Basic PCI9030 register configuration is loaded from a serial EEPROM after power-up or board reset.

Programming of the PCI9030 configuration registers is scope of the board initialization software.

8.1.1 PCI9030 PCI Header

Offset	PCI Configuration Register				Setting
	31 - 24	23 - 16	15 - 08	07 - 00	
0x00	Device ID		Vendor ID		0x9030_10B5
0x04	Status		Command		0x0280_0003
0x08	Class Code			Revision ID	0x0680_0000
0x0C	Not Supported	Header	Not Supported	Cache Line	0x0000_0000
0x10	PCI Base Address 0 (PCIBAR0) (PCI9030 Local Configuration Register Memory Mapped)				0xFFFF_FF80 (128 Byte)
0x14	PCI Base Address 1 (PCIBAR1) (PCI9030 Local Configuration Register I/O Mapped)				0xFFFF_FF81(1) (128 Byte)
0x18	PCI Base Address 2 (PCIBAR2) (Local Space 0) (IP Interface Control & Status Register)				0xFFFF_FF00(1) (256 Byte)
0x1C	PCI Base Address 3 (PCIBAR3) (Local Space 1) (IP A – D I/O, ID, INT Space)				0xFFFF_FC00(1) (1 Kbyte)
0x20	PCI Base Address 4 (PCIBAR4) (Local Space 2) (IP A – D MEM Space 16bit)				0xFE00_0000(1) (32 Mbyte)
0x24	PCI Base Address 5 (PCIBAR5) (Local Space 3) (IP A – D MEM Space 8bit)				0xFF00_0000(1) (16 Mbyte)
0x28	Not Supported				0x0000_0000
0x2C	Subsystem ID (TVME8300)		Subsystem Vendor ID (TEWS TECHNOLOGIES)		0x206C_1498
0x30	PCI Expansion ROM Base Address				0x0000_0000
0x34	Reserved			Cap. Pointer	0x0000_0040
0x38	Reserved				0x0000_0000
0x3C	Not Supported	Not Supported	Interrupt Pin	Interrupt Line	0x0000_0100
0x40	PM Capabilities		PM NxtCap	PM CapID	0x4801_0001
0x44	PM Data	PM CSR EXT	PM CSR		0x0000_0000
0x48	Reserved	HS CSR	HS NxtCap	HS CapID	0x0000_0006
0x4C	VPD Address		VPD NxtCap	VPD CapID	0x0000_0003
0x50	VPD Data				0x0000_0000

(1) Read back Value after writing all 1's.

Figure 8-1 : PCI9030 PCI Header

8.1.2 Local Configuration Register

The PCI base address for the PCI9030 Local Configuration Registers can be obtained from the PCIBAR0 (PCI Memory mapped) register at offset 0x10 or from the PCIBAR1 (PCI I/O mapped) register at offset 0x14 in the PCI9030 PCI configuration register space.

Register Offset	Local Configuration Register	Name	Setting
0x00	Local Space 0 Range	LAS0RR	0x0FFF_FF00
0x04	Local Space 1 Range	LAS1RR	0x0FFF_FC00
0x08	Local Space 2 Range	LAS2RR	0x0E00_0000
0x0C	Local Space 3 Range	LAS3RR	0x0F00_0000
0x10	Expansion ROM Range	EROMRR	0x0000_0000
0x14	Local Space 0 Remap	LAS0BA	0x0800_0001
0x18	Local Space 1 Remap	LAS1BA	0x0400_0001
0x1C	Local Space 2 Remap	LAS2BA	0x0000_0001
0x20	Local Space 3 Remap	LAS3BA	0x0200_0001
0x24	Expansion ROM Remap	EROMBA	0x0000_0000
0x28	Local Space 0 Descriptor	LAS0BRD	0x1541_20A0
0x2C	Local Space 1 Descriptor	LAS1BRD	0x1541_20A2
0x30	Local Space 2 Descriptor	LAS2BRD	0x1541_20A2
0x34	Local Space 3 Descriptor	LAS3BRD	0x1501_20A2
0x38	Expansion ROM Descriptor	EROMBRD	0x0000_0000
0x3C	Local Chip Select 0	CS0BASE	0x0800_0081
0x40	Local Chip Select 1	CS1BASE	0x0400_0201
0x44	Local Chip Select 2	CS2BASE	0x0100_0001
0x48	Local Chip Select 3	CS3BASE	0x0280_0001
0x4C	Serial EEPROM / Interrupt Control & Status	PROT_AREA / INTCSR	0x0030_0049
0x50	Miscellaneous	CNTRL	0x007A_4000
0x54	General Purpose I/O	GPIOC	0x0224_9251

Figure 8-2 : PCI9030 Local Configuration Register

Shown values are register values after serial EEPROM configuration.

8.1.3 PCI9030 Configuration EEPROM

Basic PCI9030 register configuration is loaded from an on board serial EEPROM at power-up or board reset.

EEPROM Offset	Register Offset	Register Description	Register Bits Affected	Value
0x00	PCI 0x02	Device ID	PCIIDR[31:16]	0x9030
0x02	PCI 0x00	Vendor ID	PCIIDR[15:0]	0x10B5
0x04	PCI 0x06	PCI Status	PCISR[15:0]	0x0280
0x06	PCI 0x04	PCI Command	Reserved	0x0000
0x08	PCI 0x0A	Class Code	PCICCR[15:0]	0x0680
0x0A	PCI 0x08	Class Code / Revision	PCICR[7:0] / PCIREV[7:0]	0x0000
0x0C	PCI 0x2E	Subsystem ID	PCISID[15:0]	0x206C
0x0E	PCI 0x2C	Subsystem Vendor ID	PCISVID[15:0]	0x1498
0x10	PCI 0x36	MSB New Capability Pointer	Reserved	0x0000
0x12	PCI 0x34	LSB New Capability Pointer	CAP_PTR[7:0]	0x0040
0x14	PCI 0x3E	Max_Lat, Max_Gnt	Reserved	0x0000
0x16	PCI 0x3C	Interrupt Pin	PCIIPR[7:0] / Reserved	0x0100
0x18	PCI 0x42	MSW Power Management Capabilities	PMC[14:11, 5, 3:0]	0x4801
0x1A	PCI 0x40	LSW Power Management Capabilities	PM_NEXT[7:0] / PMCAPID[7:0]	0x0001
0x1C	PCI 0x46	MSW Power Management Data / PMCSR Bridge Support Ext.	Reserved	0x0000
0x1E	PCI 0x44	LSW Power Management Control / Status	PMCSR[14:8]	0x0000
0x20	PCI 0x4A	MSW Hot Swap Control / Status	Reserved	0x0000
0x22	PCI 0x48	LSW Hot Swap Next Capability Pointer / Hot Swap Control	HS_NEXT[7:0] / HS_CNTL[7:0]	0x0006
0x24	PCI 0x4E	PCI Vital Product Data Address	Reserved	0x0000
0x26	PCI 0x4C	PCI Vital Product Data Next Capability Pointer / PCI Vital Product Data Control	PVPD_NEXT[]7:0] / PVPD_CNTL[7:0]	0x0003
0x28	Local 0x02	MSW Local Space 0 Range	LAS0RR[31:16]	0x0FFF
0x2A	Local 0x00	LSW Local Space 0 Range	LAS0RR[15:0]	0xFF00
0x2C	Local 0x06	MSW Local Space 1 Range	LAS1RR[31:16]	0x0FFF
0x2E	Local 0x04	LSW Local Space 1 Range	LAS1RR[15:0]	0xFC00
0x30	Local 0x0A	MSW Local Space 2 Range	LAS2RR[31:16]	0x0E00
0x32	Local 0x08	LSW Local Space 2 Range	LAS2RR[15:0]	0x0000
0x34	Local 0x0E	MSW Local Space 3 Range	LAS3RR[31:16]	0x0F00
0x36	Local 0x0C	LSW Local Space 3 Range	LAS3RR[15:0]	0x0000
0x38	Local 0x12	MSW Local Exp. ROM Range	EROMRR[31:16]	0x0000
0x3A	Local 0x10	LSW Local Exp. ROM Range	EROMRR[15:0]	0x0000
0x3C	Local 0x16	MSW Local Space 0 Remap	LAS0BA[31:16]	0x0800
0x3E	Local 0x14	LSW Local Space 0 Remap	LAS0BA[15:0]	0x0001
0x40	Local 0x1A	MSW Local Space 1 Remap	LAS1BA[31:16]	0x0400
0x42	Local 0x18	LSW Local Space 1 Remap	LAS1BA[31:16]	0x0001

EEPROM Offset	Register Offset	Register Description	Register Bits Affected	Value
0x44	Local 0x1E	MSW Local Space 2 Remap	LAS2BA[31:16]	0x0000
0x46	Local 0x1C	LSW Local Space 2 Remap	LAS2BA[31:16]	0x0001
0x48	Local 0x22	MSW Local Space 3 Remap	LAS3BA[31:16]	0x0200
0x4A	Local 0x20	LSW Local Space 3 Remap	LAS3BA[31:16]	0x0001
0x4C	Local 0x26	MSW Local Exp. ROM Remap	EROMBA[31:16]	0x0000
0x4E	Local 0x24	LSW Local Exp. ROM Remap	EROMBA[15:0]	0x0000
0x50	Local 0x2A	MSW Local Space 0 Descriptor	LAS0BRD[31:0]	0x1541
0x52	Local 0x28	LSW Local Space 0 Descriptor	LAS0BRD[15:0]	0x20A0
0x54	Local 0x2E	MSW Local Space 1 Descriptor	LAS1BRD[31:0]	0x1541
0x56	Local 0x2C	LSW Local Space 1 Descriptor	LAS1BRD[15:0]	0x20A2
0x58	Local 0x32	MSW Local Space 2 Descriptor	LAS2BRD[31:0]	0x1541
0x5A	Local 0x30	LSW Local Space 2 Descriptor	LAS2BRD[15:0]	0x20A2
0x5C	Local 0x36	MSW Local Space 3 Descriptor	LAS3BRD[31:0]	0x1501
0x5E	Local 0x34	LSW Local Space 3 Descriptor	LAS3BRD[15:0]	0x20A2
0x60	Local 0x3A	MSW Local Exp. ROM Descriptor	EROMBRD[31:16]	0x0000
0x62	Local 0x38	LSW Local Exp. ROM Descriptor	EROMBRD[15:0]	0x0000
0x64	Local 0x3E	MSW Local Chip Select 0	CS0BASE[31:16]	0x0800
0x66	Local 0x3C	LSW Local Chip Select 0	CS0BASE[15:0]	0x0081
0x68	Local 0x42	MSW Local Chip Select 1	CS1BASE[31:16]	0x0400
0x6A	Local 0x40	LSW Local Chip Select 1	CS1BASE[15:0]	0x0201
0x6C	Local 0x46	MSW Local Chip Select 2	CS2BASE[31:16]	0x0100
0x6E	Local 0x44	LSW Local Chip Select 2	CS2BASE[15:0]	0x0001
0x70	Local 0x4A	MSW Local Chip Select 3	CS3BASE[31:16]	0x0280
0x72	Local 0x48	LSW Local Chip Select 3	CS3BASE[15:0]	0x0001
0x74	Local 0x4E	Serial EEPROM Write Protect	PROT_AREA[7:0]	0x0030
0x76	Local 0x4C	LSW Interrupt Control / Status	INTCSR[15:0]	0x0049
0x78	Local 0x52	MSW Miscellaneous	CNTRL[31:16]	0x007A
0x7A	Local 0x50	LSW Miscellaneous	CNTRL[15:0]	0x4000
0x7C	Local 0x56	MSW General Purpose I/O Control	GPIOC[31:16]	0x0224
0x7E	Local 0x54	LSW General Purpose I/O Control	GPIOC[15:0]	0x9251
0x80	Local 0x72	MSW Power Management Data Select		0x0000
0x82	Local 0x70	LSW Power Management Data Select		0x0000
0x84	Local 0x76	MSW Power Management Data Scale		0x0000
0x86	Local 0x74	LSW Power Management Data Scale		0x0000

Figure 8-3 : PCI9030 Configuration EEPROM Settings

EEPROM Offset	0x00	0x02	0x04	0x06	0x08	0x0A	0x0C	0x0E
0x00	0x9030	0x10B5	0x0280	0x0000	0x0680	0x0000	0x206C	0x1498
0x10	0x0000	0x0040	0x0000	0x0100	0x4801	0x0001	0x0000	0x0000
0x20	0x0000	0x0006	0x0000	0x0003	0x0FFF	0xFF00	0x0FFF	0xFC00
0x30	0x0E00	0x0000	0x0F00	0x0000	0x0000	0x0000	0x0800	0x0001
0x40	0x0400	0x0001	0x0000	0x0001	0x0200	0x0001	0x0000	0x0000
0x50	0x1541	0x20A0	0x1541	0x20A2	0x1541	0x20A2	0x1501	0x20A2
0x60	0x0000	0x0000	0x0800	0x0081	0x0400	0x0201	0x0100	0x0001
0x70	0x0280	0x0001	0x0030	0x0049	0x007A	0x4000	0x0224	0x9251
0x80	0x0000	0x0000	0x0000	0x0000	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0x90	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xA0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xB0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xC0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xD0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xE0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF
0xF0	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF	0xFFFF

Figure 8-4 : PCI9030 Configuration EEPROM Content

8.2 IP Interface

The IP interface is controlled by an IP FPGA logic. The IP FPGA also provides some IP Interface Control & Status Registers.

The IP FPGA logic is configured at power-up or board reset by an on board serial PROM.

Board Initialization software should verify successful FPGA configuration in the Utility Status Register.

8.2.1 PCI9030 Local Space Assignment

The PCI9030 local spaces must be used to access the IP interface. The PCI base address for each local space can be obtained from the PCI9030 PCI configuration register space.

PCI9030 Local Space	Size (Byte)	Port Width (Bit)	Endian Mode	PCI Space	IP Interface Space
0	256	16	Big	Mem	IP Interface Register
1	1K	16	Big	Mem	IP A – D ID, INT, IO Space
2	32M	16	Big	Mem	IP A – D MEM Space (16 bit port)
3	16M	8	Big	Mem	IP A – D MEM Space (8 bit port)

Figure 8-5 : PCI9030 Local Space Assignment

8.2.2 Local Space 0 Address Map

The PCI9030 local space 0 is used for the IP interface registers.

The PCI base address for local space 0 is PCIBAR2 at offset 0x18 in the PCI9030 PCI configuration register space.

Offset (Base = PCI Base Address 2)	Size (Byte)	Register
0x00	2	REVISION ID
0x02	2	IP A CONTROL
0x04	2	IP B CONTROL
0x06	2	IP C CONTROL
0x08	2	IP D CONTROL
0x0A	2	RESET
0x0C	2	STATUS
0x0E	2	Reserved
0x10 - 0xFF	240	Reserved

Figure 8-6 : Local Space 0 Address Map (IP Interface Register)

8.2.3 IP Interface Register

8.2.3.1 Revision ID Register

The Revision ID Register indicates the revision of the on board IP FPGA logic.

Bit	Name	Description
15 (MSB)	REV_ID	Read Only FPGA Logic Revision ID
14		
13		
12		
11		
10		
9		
8		
7		
6		
5		
4		
3		
2		
1		
0 (LSB)		

Figure 8-7 : Revision ID Register

8.2.3.2 IP Control Registers

The IP Control Registers can be used to control IP interrupts, recover time and clock rate.

There is one IP Control Register for each IP Slot (A - D).

Bit	Name	Description
15 (MSB)	Reserved	Undefined for Reads Write as '0'
14		
13		
12		
11		
10		
9		
8		
7	INT1_EN	0 : IP Interrupt 1 Disabled 1 : IP Interrupt 1 Enabled
6	INT0_EN	0 : IP Interrupt 0 Disabled 1 : IP Interrupt 0 Enabled
5	INT1_SENSE	0 : IP Interrupt 1 Level Sensitive 1 : IP Interrupt 1 Edge Sensitive
4	INT0_SENSE	0 : IP Interrupt 0 Level Sensitive 1 : IP Interrupt 0 Edge Sensitive
3	ERR_INT_EN	0 : IP Error Interrupt Disabled 1 : IP Error Interrupt Enabled
2	TIME_INT_EN	0 : IP Timeout Interrupt Disabled 1 : IP Timeout Interrupt Enabled
1	RECOVER	0 : IP Recover Time Disabled 1 : IP Recover Time Enabled
0 (LSB)	CLKRATE	0 : IP Clock Rate 8 MHz 1 : IP Clock Rate 32 MHz

Figure 8-8 : IP Control Register

After power-up or board reset all bits in the IP Control Registers are cleared.

Defined register bits support read/write access.

If IP recover time is enabled for an IP slot, an IP cycle for this slot will not begin until the IP recover time is expired after the previous IP access. The IP recover time is app. 1µs.

8.2.3.3 Reset Register

The Reset Register can be used to assert the IP RESET# signal and to detect when the IP RESET# signal is negated.

Bit	Name	Description
15 (MSB)	Reserved	Undefined for Reads Write as '0'
14		
13		
12		
11		
10		
9		
8		
7		
6		
5		
4		
3	IP_D_RESET	Read : 0 : IP RESET# Signal on Slot x is De-asserted 1 : IP RESET# Signal on Slot x is Asserted Write '1' to assert the IP RESET# Signal on Slot x (Automatic De-assertion). Write 0x000F to assert reset on all IP slots.
2	IP_C_RESET	
1	IP_B_RESET	
0 (LSB)	IP_A_RESET	

Figure 8-9 : Reset Register

The IP RESET# signal is also asserted on all IP slots at power-up or board reset.

Asserting IP reset by software does not reset the clock mode to 8 MHz.

If 32 MHz clock mode is used, the clock mode should be reset to 8 MHz prior to asserting the IP reset by software.

8.2.3.4 Status Register

The Status Register can be used to read IP timeout, error and interrupt status.

Bit	Name	Description
15 (MSB)	TIME_D	Read : 0 : No Timeout on IP_D 1 : IP_D Timeout has occurred Write '1' to clear IP_D Timeout Status
14	TIME_C	Read : 0 : No Timeout on IP_C 1 : IP_C Timeout has occurred Write '1' to clear IP_C Timeout Status
13	TIME_B	Read : 0 : No Timeout on IP_B 1 : IP_B Timeout has occurred Write '1' to clear IP_B Timeout Status
12	TIME_A	Read : 0 : No Timeout on IP_A 1 : IP_A Timeout has occurred Write '1' to clear IP_A Timeout Status
11	ERR_D	Read : 0 : No Error on IP_D 1 : IP_D ERROR# Signal Asserted Write : No Effect
10	ERR_C	Read : 0 : No Error on IP_C 1 : IP_C ERROR# Signal Asserted Write : No Effect
9	ERR_B	Read : 0 : No Error on IP_B 1 : IP_B ERROR# Signal Asserted Write : No Effect
8	ERR_A	Read : 0 : No Error on IP_A 1 : IP_A ERROR# Signal Asserted Write : No Effect
7	INT1_D	Read : 0 : No Interrupt 1 Request on IP_D 1 : Active IP_D Interrupt 1 Request Write '1' to clear Edge Sensitive IP_D Interrupt 1 Status
6	INT0_D	Read : 0 : No Interrupt 0 Request on IP_D 1 : Active IP_D Interrupt 0 Request Write '1' to clear Edge Sensitive IP_D Interrupt 0 Status
5	INT1_C	Read : 0 : No Interrupt 1 Request on IP_C 1 : Active IP_C Interrupt 1 Request Write '1' to clear Edge Sensitive IP_C Interrupt 1 Status

Bit	Name	Description
4	INT0_C	Read : 0 : No Interrupt 0 Request on IP_C 1 : Active IP_C Interrupt 0 Request Write '1' to clear Edge Sensitive IP_C Interrupt 0 Status
3	INT1_B	Read : 0 : No IP_B Interrupt 1 Request 1 : Active IP_B Interrupt 1 Request Write '1' to clear Edge Sensitive IP_B Interrupt 1 Status
2	INT0_B	Read : 0 : No Interrupt 0 Request on IP_B 1 : Active IP_B Interrupt 0 Request Write '1' to clear Edge Sensitive IP_B Interrupt 0 Status
1	INT1_A	Read : 0 : No Interrupt 1 Request on IP_A 1 : Active IP_A Interrupt 1 Request Write '1' to clear Edge Sensitive IP_A Interrupt 1 Status
0 (LSB)	INT0_A	Read : 0 : No Interrupt 0 Request on IP_A 1 : Active IP_A Interrupt 0 Request Write '1' to clear Edge Sensitive IP_A Interrupt 0 Status

Figure 8-10: Status Register

The IP timeout time is app. 8µs.

An IP timeout occurs if the IP module fails to generate the IP ACK# signal within the IP timeout time. An IP timeout is not reported to the PCI9030 or the PCI Master, but is reported in the Status Register. For timed-out reads all F's are returned.

8.2.4 Local Space 1 Address Map

The PCI9030 local space 1 is used for the IP A - D ID, INT and I/O space.

The PCI base address for local space 1 is PCIBAR3 at offset 0x1C in the PCI9030 PCI configuration register space.

Offset (Base = PCI Base Address 3)		Size (Byte)	Description
Start	End		
0x0000_0000	0x0000_007F	128	IP A I/O Space
0x0000_0080	0x0000_00BF	64	IP A ID Space
0x0000_00C0	0x0000_00FF	64	IP A INT Space
0x0000_0100	0x0000_017F	128	IP B I/O Space
0x0000_0180	0x0000_01BF	64	IP B ID Space
0x0000_01C0	0x0000_01FF	64	IP B INT Space
0x0000_0200	0x0000_027F	128	IP C I/O Space
0x0000_0280	0x0000_02BF	64	IP C ID Space
0x0000_02C0	0x0000_02FF	64	IP C INT Space
0x0000_0300	0x0000_037F	128	IP D I/O Space
0x0000_0380	0x0000_03BF	64	IP D ID Space
0x0000_03C0	0x0000_03FF	64	IP D INT Space

Figure 8-11: Local Space 1 Address Map (IP A-D ID, INT, I/O Space)

The TVME8300 will perform write cycles to the IP ID space.

Any access to the IP INT space will assert the IP INTSEL# signal on the selected IP slot. The TVME8300 will perform write cycles to the IP INT space.

The user should perform IP INT space read cycles on the desired IP slot to generate an IP INTSEL# cycle and read the interrupt vector. For this read cycle the IP A1 address must reflect if the IP INTSEL# cycle is for IP INT0# or for IP INT1#.

8.2.5 Local Space 2 Address Map

The PCI9030 local space 2 is used for the IP A-D Memory space (16 bit port).

The PCI base address for local space 2 is PCIBAR4 at offset 0x20 in the PCI9030 PCI configuration register space.

Offset (Base = PCI Base Address 4)		Size (Byte)	Description
Start	End		
0x0000_0000	0x007F_FFFF	8M	IP A MEM Space (16 bit)
0x0080_0000	0x00FF_FFFF	8M	IP B MEM Space (16 bit)
0x0100_0000	0x017F_FFFF	8M	IP C MEM Space (16 bit)
0x0180_0000	0x01FF_FFFF	8M	IP D MEM Space (16 bit)

Figure 8-12: Local Space 2 Address Map (IP A-D Memory Space 16 bit)

8.2.6 Local Space 3 Address Map

The PCI9030 local space 3 is used for the IP A-D Memory space (8 bit port).

The PCI base address for local space 3 is PCIBAR5 at offset 0x24 in the PCI9030 PCI configuration register space.

Offset (Base = PCI Base Address 5)		Size (Byte)	Description
Start	End		
0x0000_0000	0x003F_FFFF	4M	IP A MEM Space (8 bit)
0x0040_0000	0x007F_FFFF	4M	IP B MEM Space (8 bit)
0x0080_0000	0x00BF_FFFF	4M	IP C MEM Space (8 bit)
0x00C0_0000	0x00FF_FFFF	4M	IP D MEM Space (8 bit)

Figure 8-13: Local Space 3 Address Map (IP A-D Memory Space 8 bit)

The 8 bit IP Memory space should be used for memory space incremental byte addressing of IP modules that use IP data lines D[7:0] only.

8.3 IP Interrupts

The IP FPGA maps all IP interface interrupt sources (Timeout, Error, INT0, INT1) to the PCI9030 local interrupt input 1 (LINT1#). The PCI9030 local interrupt 2 (LINT2#) is reserved.

The PCI9030 PCI Target Chip maps its local interrupt inputs to its PCI interrupt output (INTA#).

The PCI9030 PCI interrupt output is mapped to the serial interrupt no. 4 of the MPC8245 PIC.

Upon detecting MPC8245 PIC Serial Interrupt No. 4, read the IP Status Register (PCI9030 Local Space 0) to determine the IP interrupt source.

Timeout interrupts and edge sensitive IP interrupts must be cleared in the IP Status Register.

For using Error interrupts it is assumed that the IP module holds the asserted ERROR# signal level and provides an acknowledge mechanism by register access to clear the error signal assertion. If the IP module does not hold the asserted ERROR# signal level, there is a possibility of spurious interrupts. If the IP module does hold the asserted ERROR# signal level, but does not provide an acknowledge mechanism, the ERROR# interrupt should be disabled when entered for the first time.

9 PCI Bus Overview

PCI Device	Device Number	Device ID	Vendor ID	Subsys ID	Subsys Vendor ID	PCI Arbiter Line (MPC8245)	Required Memory Space (Byte)	Required I/O Space (Byte)
MPC8245 Integrated Host PPC	-	0x0006	0x1057	0x0000	0x0000	-	-	-
Universe-II VME / PCI Bridge	13	0x0000	0x10E3	-	-	0	4K + Appl. Dep. PCI Target Images	4K
82551ER Fast Ethernet Controller	14	0x1209	0x8086	0x0000	0x0000	1	4K	64
PCI9030 PCI target Chip (IP Interface)	16	0x9030	0x10B5	0x206C	0x1498	N/A	128 + 256 + 1K + 32M +16M	128
PCI Expansion Connector	Depends on PCI Exp. Card	Depends on PCI Exp. Card	Depends on PCI Exp. Card	Depends on PCI Exp. Card	Depends on PCI Exp. Card	3	Depends on PCI Exp. Card	Depends on PCI Exp. Card

Figure 9-1: PCI Bus Overview

10 Board I/O

10.1 Board I/O Overview

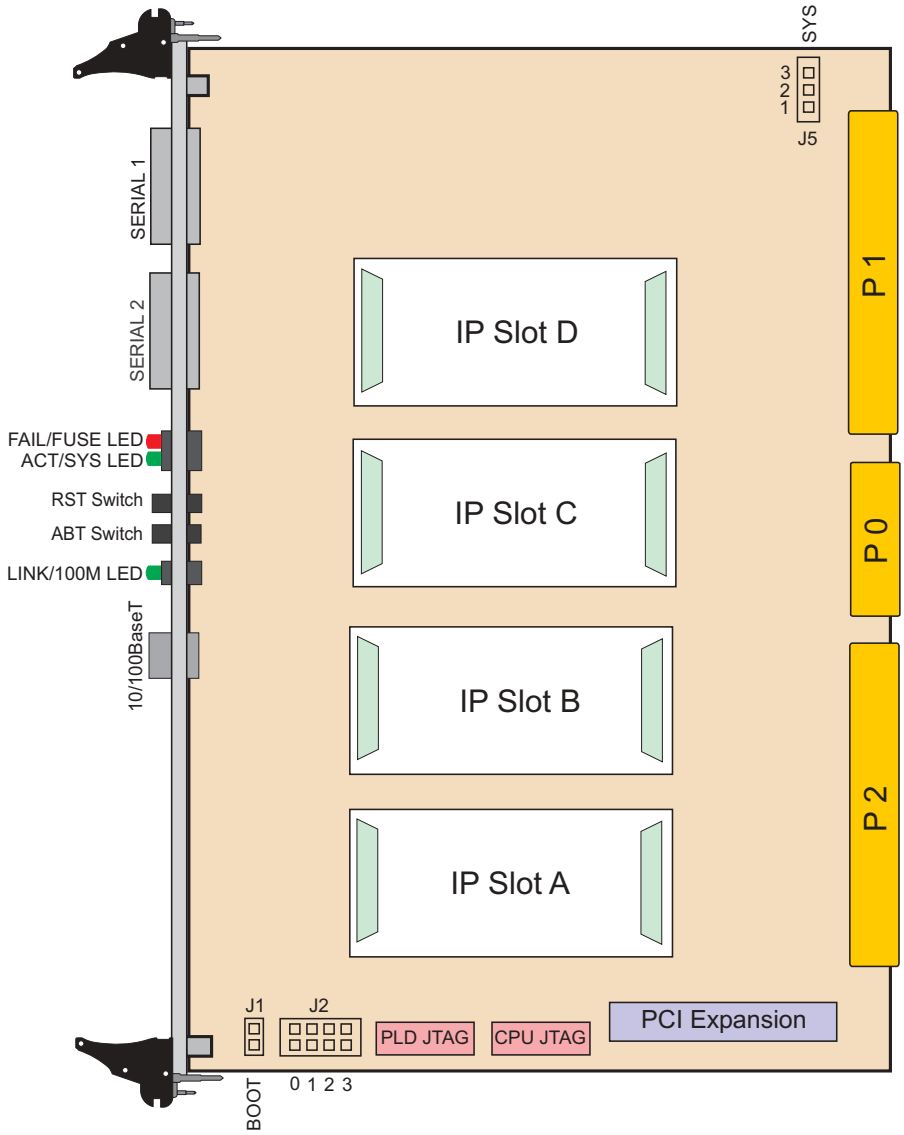

Figure 10-1: Board I/O Overview

10.2 Jumper

10.2.1 Boot Jumper

The boot jumper status can be read in the Utility Status Register.

The boot jumper function is reserved by the (factory default) boot initialization software.

The (factory default) board initialization software checks the boot jumper to decide if program execution continues from the Boot FLASH (boot jumper open = start bug monitor program), or from the Memory FLASH (boot jumper closed = start user application).

If used, the first instruction in the Memory FLASH must reside at address 0xFF00_0100.

BOOT JUMPER	
Jumper Installed	Execute Memory FLASH Program after board initialization
No Jumper Installed	Execute Bug Monitor Program after board initialization

Figure 10-2: Boot Jumper

The boot jumper function is reserved by the (factory default) boot initialization software.

The 8 bit wide socket Boot FLASH must always be installed and provide the board initialization code at the system reset vector.

If used, the first instruction in the Memory FLASH must reside at address 0xFF00_0100.

10.2.2 VME System Controller Jumper

The VME system controller jumper is used to configure the VME system controller mode of the TVME8300 Universe-II VME to PCI bridge.

VME SYSTEM CONTROLLER JUMPER	
Jumper 1-2 Installed	Not VME System Controller
Jumper 2-3 Installed	VME System Controller Auto Configuration
No Jumper Installed	VME System Controller

Figure 10-3: VME System Controller Jumper

The VME system controller jumper controls the Universe-II BGIN3# input signal, which the Universe-II samples at power-up to determine VME System Controller mode.

10.2.3 User Jumper

The TVME8300 provides four user defined jumpers.

The status of the four user jumpers can be read in the Utility User Jumper Status Register.

10.3 LEDs

Function	Label	Color	Description
Board Activity	ACT	Green	Indicates Memory Bus or PCI Bus activity
VME Bus System Controller	SYS	Green	Indicates if the TVME8300 is configured as VME Bus System Controller
Board Failure	FAIL	Red	User controlled Status LED
Active Fuse	FUSE	Red	Indicates triggered fuses for IP Interface Power Supply
LAN Link	LINK	Green	Indicates LAN Link Status
LAN Speed	100M	Green	Indicates LAN 100Mbps Speed

Figure 10-4: Status Indicators

During board reset all LEDs are on.

10.3.1 ACT LED

The ACT (Activity) LED (Green) is set by hardware control if there is any activity on the Local Memory bus or PCI bus.

10.3.2 SYS LED

The SYS (System Controller) LED (Green) is set by hardware control if the Universe-II (VME to PCI Bridge) is the VME bus System Controller.

10.3.3 FAIL LED

The FAIL LED (Red) can be set by software control via the Utility LED Register to indicate a failure condition.

10.3.4 FUSE LED

The FUSE LED (Red) is set by hardware control if any of the on board resettable fuses triggers.

There is one resettable fuse for each of the following power supplies:

- IP Slot A/B +5V (2A Fuse)
- IP Slot C/D +5V (2A Fuse)
- IP Slot A/B/C/D +12V (2A Fuse)
- IP Slot A/B/C/D -12V (2A Fuse)

10.3.5 LINK LED

The LINK LED indicates if the 82551ER PHY unit detects valid link pulses on the Ethernet connection.

10.3.6 100M LED

The 100M (100Mbps) LED indicates if the Ethernet connection is operating at 100Mbps speed.

10.4 Switches

10.4.1 RST Switch

The RST (RESET) switch can be used to generate a board reset.

A board reset is also performed at power-up.

A board reset can also be asserted by software, programming the Utility Control Register.

A board reset will perform a general board hardware reset, re-configuration of the IP FPGA, PCI reset and CPU reset.

10.4.2 ABT Switch

The ABT (ABORT) switch can be used to generate a CPU interrupt.

The Abort Switch is mapped to serial interrupt no. 1 of the MPC8245 PIC.

Serial interrupt no. 1 must be configured as edge sensitive.

10.5 Connectors

10.5.1 VME Interface Connectors

10.5.1.1 VME P1 Connector

Pin	Row Z	Row A	Row B	Row C	Row D
1	-	VME_D0	VME_BBSY#	VME_D8	-
2	GND	VME_D1	VME_BCLR#	VME_D9	GND
3	-	VME_D2	VME_ACFAIL#	VME_D10	-
4	GND	VME_D3	VME_BGIN0#	VME_D11	-
5	-	VME_D4	VME_BGOUT0#	VME_D12	-
6	GND	VME_D5	VME_BGIN1#	VME_D13	-
7	-	VME_D6	VME_BGOUT1#	VME_D14	-
8	GND	VME_D7	VME_BGIN2#	VME_D15	-
9	-	GND	VME_BGOUT2#	GND	-
10	GND	VME_SYSCLK	VME_BGIN3#	VME_SYSFAIL#	-
11	-	GND	VME_BGOUT3#	VME_BERR#	-
12	GND	VME_DS1#	VME_BR0#	VME_SYSRST#	VME_3.3V
13	-	VME_DS0#	VME_BR1#	VME_LWORD#	-
14	GND	VME_WRITE#	VME_BR2#	VME_AM5	VME_3.3V
15	-	GND	VME_BR3#	VME_A23	-
16	GND	VME_DTACK#	VME_AM0	VME_A22	VME_3.3V
17	-	GND	VME_AM1	VME_A21	-
18	GND	VME_AS#	VME_AM2	VME_A20	VME_3.3V
19	-	GND	VME_AM3	VME_A19	-
20	GND	VME_IACK#	GND	VME_A18	VME_3.3V
21	-	VME_IACKIN#	-	VME_A17	-
22	GND	VME_IACKOUT#	-	VME_A16	VME_3.3V
23	-	VME_AM4	GND	VME_A15	-
24	GND	VME_A7	VME_IRQ7#	VME_A14	VME_3.3V
25	-	VME_A6	VME_IRQ6#	VME_A13	-
26	GND	VME_A5	VME_IRQ5#	VME_A12	VME_3.3V
27	-	VME_A4	VME_IRQ4#	VME_A11	-
28	GND	VME_A3	VME_IRQ3#	VME_A10	VME_3.3V
29	-	VME_A2	VME_IRQ2#	VME_A9	-
30	GND	VME_A1	VME_IRQ1#	VME_A8	VME_3.3V
31	-	-12V	-	+12V	GND
32	GND	+5V	+5V	+5V	-

Figure 10-5: VME P1 Connector

10.5.1.2 VME P0 Connector

Pin	A	B	C	D	E	F
1	IP_D_IO_01	IP_D_IO_02	IP_D_IO_03	IP_D_IO_04	IP_D_IO_05	GND
2	IP_D_IO_06	IP_D_IO_07	IP_D_IO_08	IP_D_IO_09	IP_D_IO_10	GND
3	IP_D_IO_11	IP_D_IO_12	IP_D_IO_13	IP_D_IO_14	IP_D_IO_15	GND
4	IP_D_IO_16	IP_D_IO_17	IP_D_IO_18	IP_D_IO_19	IP_D_IO_20	GND
5	IP_D_IO_21	IP_D_IO_22	IP_D_IO_23	IP_D_IO_24	IP_D_IO_25	GND
6	IP_D_IO_26	IP_D_IO_27	IP_D_IO_28	IP_D_IO_29	IP_D_IO_30	GND
7	IP_D_IO_31	IP_D_IO_32	IP_D_IO_33	IP_D_IO_34	IP_D_IO_35	GND
8	IP_D_IO_36	IP_D_IO_37	IP_D_IO_38	IP_D_IO_39	IP_D_IO_40	GND
9	IP_D_IO_41	IP_D_IO_42	IP_D_IO_43	IP_D_IO_44	IP_D_IO_45	GND
10	IP_D_IO_46	IP_D_IO_47	IP_D_IO_48	IP_D_IO_49	IP_D_IO_50	GND
11	IP_C_IO_01	IP_C_IO_02	IP_C_IO_03	IP_C_IO_04	IP_C_IO_05	GND
12	IP_C_IO_06	IP_C_IO_07	IP_C_IO_08	IP_C_IO_09	IP_C_IO_10	GND
13	IP_C_IO_11	IP_C_IO_12	IP_C_IO_13	IP_C_IO_14	IP_C_IO_15	GND
14	IP_C_IO_16	IP_C_IO_17	IP_C_IO_18	IP_C_IO_19	IP_C_IO_20	GND
15	IP_C_IO_21	IP_C_IO_22	IP_C_IO_23	IP_C_IO_24	IP_C_IO_25	GND
16	IP_C_IO_26	IP_C_IO_27	IP_C_IO_28	IP_C_IO_29	IP_C_IO_30	GND
17	IP_C_IO_31	IP_C_IO_32	IP_C_IO_33	IP_C_IO_34	IP_C_IO_35	GND
18	IP_C_IO_36	IP_C_IO_37	IP_C_IO_38	IP_C_IO_39	IP_C_IO_40	GND
19	IP_C_IO_41	IP_C_IO_42	IP_C_IO_43	IP_C_IO_44	IP_C_IO_45	GND

Figure 10-6: VME P0 Connector

10.5.1.3 VME P2 Connector

Pin	Row Z	Row A	Row B	Row C	Row D
1	IP_C_IO_46	IP_B_IO_41	+5V	IP_B_IO_42	IP_C_IO_47
2	GND	IP_B_IO_43	GND	IP_B_IO_44	IP_C_IO_48
3	IP_C_IO_49	IP_B_IO_45	-	IP_B_IO_46	IP_C_IO_50
4	GND	IP_B_IO_47	VME_A24	IP_B_IO_48	IP_B_IO_01
5	IP_B_IO_02	IP_B_IO_49	VME_A25	IP_B_IO_50	IP_B_IO_03
6	GND	IP_A_IO_01	VME_A26	IP_A_IO_02	IP_B_IO_04
7	IP_B_IO_05	IP_A_IO_03	VME_A27	IP_A_IO_04	IP_B_IO_06
8	GND	IP_A_IO_05	VME_A28	IP_A_IO_06	IP_B_IO_07
9	IP_B_IO_08	IP_A_IO_07	VME_A29	IP_A_IO_08	IP_B_IO_09
10	GND	IP_A_IO_09	VME_A30	IP_A_IO_10	IP_B_IO_10
11	IP_B_IO_11	IP_A_IO_11	VME_A31	IP_A_IO_12	IP_B_IO_12
12	GND	IP_A_IO_13	GND	IP_A_IO_14	IP_B_IO_13
13	IP_B_IO_14	IP_A_IO_15	+5V	IP_A_IO_16	IP_B_IO_15
14	GND	IP_A_IO_17	VME_D16	IP_A_IO_18	IP_B_IO_16
15	IP_B_IO_17	IP_A_IO_19	VME_D17	IP_A_IO_20	IP_B_IO_18
16	GND	IP_A_IO_21	VME_D18	IP_A_IO_22	IP_B_IO_19
17	IP_B_IO_20	IP_A_IO_23	VME_D19	IP_A_IO_24	IP_B_IO_21
18	GND	IP_A_IO_25	VME_D20	IP_A_IO_26	IP_B_IO_22
19	IP_B_IO_23	IP_A_IO_27	VME_D21	IP_A_IO_28	IP_B_IO_24
20	GND	IP_A_IO_29	VME_D22	IP_A_IO_30	IP_B_IO_25
21	IP_B_IO_26	IP_A_IO_31	VME_D23	IP_A_IO_32	IP_B_IO_27
22	GND	IP_A_IO_33	GND	IP_A_IO_34	IP_B_IO_28
23	IP_B_IO_29	IP_A_IO_35	VME_D24	IP_A_IO_36	IP_B_IO_30
24	GND	IP_A_IO_37	VME_D25	IP_A_IO_38	IP_B_IO_31
25	IP_B_IO_32	IP_A_IO_39	VME_D26	IP_A_IO_40	IP_B_IO_33
26	GND	IP_A_IO_41	VME_D27	IP_A_IO_42	IP_B_IO_34
27	IP_B_IO_35	IP_A_IO_43	VME_D28	IP_A_IO_44	IP_B_IO_36
28	GND	IP_A_IO_45	VME_D29	IP_A_IO_46	IP_B_IO_37
29	IP_B_IO_38	IP_A_IO_47	VME_D30	IP_A_IO_48	IP_B_IO_39
30	GND	IP_A_IO_49	VME_D31	IP_A_IO_50	IP_B_IO_40
31	VME_3.3V	VME_3.3V	GND	VME_3.3V	GND
32	GND	+5V	+5V	+5V	-

Figure 10-7: VME P2 Connector

10.5.2 IP Interface Connectors

10.5.2.1 IP P1 Connector

Pin	Signal	Pin	Signal
1	GND	2	CLK
3	RESET#	4	D0
5	D1	6	D2
7	D3	8	D4
9	D5	10	D6
11	D7	12	D8
13	D9	14	D10
15	D11	16	D12
17	D13	18	D14
19	D15	20	BS0#
21	BS1#	22	-12V
23	+12V	24	+5V
25	GND	26	GND
27	+5V	28	WRITE#
29	IDSEL#	30	DMAREQ0#
31	MEMSEL#	32	DMAREQ1#
33	INTSEL#	34	DMAACK#
35	IOSEL#	36	RSV0
37	A1	38	DMAEND#
39	A2	40	ERROR#
41	A3	42	INTREQ0#
43	A4	44	INTREQ1#
45	A5	46	STROBE#
47	A6	48	ACK#
49	RSV1	50	GND

Figure 10-8: IP P1 Connector

The following signals have an on board pull-up resistor (4K7, 3.3V):

RESET#, WRITE#, IDSEL#, IOSEL#, INTSEL#, MEMSEL#, ACK#, INTREQ0#, INTREQ1#, ERROR#, STROBE#, RSV0, RSV1, DMAREQ0#, DMAREQ1#, DMAACK#, DMAEND#.

DMA is not supported on the TVME8300 IP interface.

10.5.2.2 IP P2 Connector

For each IP slot the IP P2 connector signals (IP module I/O lines) are routed directly to the appropriate pins on the VME P2 and VME P0 connectors (conforming to the VME64x IP I/O mapping).

Please see VME Interface Connectors for details.

10.5.3 PCI Expansion Connector

Pin	Signal		Pin	Signal
1	+3.3V		2	+3.3V
3	CLK		4	INTA#
5	GND		6	INTB#
7	PONRST#		8	INTC#
9	HRST#		10	INTD#
11	TDO		12	TDI
13	TMS		14	TCK
15	TRST#		16	PRSNT#
17	GNT#		18	REQ#
19	+12V	GND	20	-12V
21	PERR#		22	SERR#
23	LOCK#		24	SDONE
25	DEVSEL#		26	SBO#
27	GND		28	GND
29	TRDY#		30	IRDY#
31	STOP#		32	FRAME#
33	GND		34	GND
35	ACK64#		36	-
37	REQ64#		38	-
39	PAR		40	RST#
41	C/BE1#		42	C/BE0#
43	C/BE3#		44	C/BE2#
45	AD1		46	AD0
47	AD3		48	AD2
49	AD5		50	AD4
51	AD7		52	AD6
53	AD9		54	AD8
55	AD11		56	AD10
57	AD13	+5V	58	AD12
59	AD15		60	AD14
61	AD17		62	AD16
63	AD19		64	AD18
65	AD21		66	AD20
67	AD23		68	AD22
69	AD25		70	AD24
71	AD27		72	AD26
73	AD29		74	AD28
75	AD31		76	AD30
77	-		78	-
79	-		80	-
81	-		82	-

Pin	Signal		Pin	Signal
83	-	GND	84	-
85	-		86	-
87	-		88	-
89	-		90	-
91	-		92	-
93	-		94	-
95	-		96	-
97	-		98	-
99	-		100	-
101	-		102	-
103	-		104	-
105	-		106	-
107	-		108	-
109	-		110	-
111	-		112	-
113	-		114	-

Figure 10-9: PCI Expansion Connector

The PCI Expansion Connector type is AMP 2-767004-4.

10.5.4 Serial Interface Connectors

10.5.4.1 Serial Port A

Pin	Signal	Level
1	DCD (input)	RS232
2	RXD (input)	RS232
3	TXD (output)	RS232
4	DTR (output)	RS232
5	GND	
6	DSR (input)	RS232
7	RTS (output)	RS232
8	CTS (input)	RS232
9	RI (input)	RS232

Figure 10-10: Serial Port A (RS232) (DB9 Male Connector)

10.5.4.2 Serial Port B

Pin	Signal	Level
1	DCD (input)	RS232
2	RXD (input)	RS232
3	TXD (output)	RS232
4	DTR (output)	RS232

5	GND	
6	DSR (input)	RS232
7	RTS (output)	RS232
8	CTS (input)	RS232
9	RI (input)	RS232

Figure 10-11: Serial Port B (RS232) (DB9 Male Connector)

The serial port signals are shown in the TVME8300 pin function.

E.g. the TXD output line of the external device must be connected to pin 2 (RXD input) of the serial port connector, not to pin 3 (TXD output).

10.5.5 Ethernet Interface Connector

Pin	Signal
1	TD+
2	TD-
3	RD+
4	
5	
6	RD-
7	
8	

Figure 10-12: Ethernet Connector (8P RJ45)

11 Installation and Use Notes

11.1 NVRAM Real-Time Clock Control

The TVME8300 provides a M48T59 NVRAM / RTC device with a snaphat battery plugged on top. The snaphat battery provides power for the SRAM cells when the main power supply is off.

The TVME8300 is shipped with the snaphat battery installed on top of the M48T59 NVRAM device. The Real-Time Clock function of the M48T59 device is **turned-off by default**, to save battery energy.

If the M48T59 Real-Time Clock function has been turned-off (factory default), it must be enabled again, before using any other board resources (e.g. Ethernet).

The PMON "date" command can be used to enable the Real-Time Clock function.

Setup / Start the Real-Time Clock function:

```
PMON> date 200408101445.00
Tue Aug 10 14:45:00 2004
PMON> reboot
```

Stop the Real-Time Clock function:

(This is recommended for TVME8300 board storage) :

```
PMON> date -x
Clock is stopped...
PMON>
```

12 Technical Information

12.1 Processor

- Motorola MPC8245 Integrated Host PPC (300 MHz Core Frequency)
- Embedded Version MPC603e (G2) Processor Core
- Floating Point Unit
- DMA Controller
- 16 Kbyte I-Cache, 16 kbyte D-Cache
- Four cascadable 31 bit timer

12.2 Memory

- 64 Mbyte 64 bit wide SDRAM (100 MHz)
- 8 Mbyte 64 bit wide Flash Memory

12.3 Other Devices

- 8 Kbyte NVRAM (M48T59) with exchangeable battery
- 1 Mbyte 8 bit wide Boot-Flash (two PLCC sockets)

12.4 VME Interface

- Tundra Universe-II
- A16-A32 Master/Slave Address Modes; D08-D64 Master/Slave Data Transfer Modes
- RR/PRI VME bus Arbiter
- IRQ 1-7 (any of seven IRQs)
- System Controller Jumper (Yes, No, Auto Detect)
- Four Location Monitors
- DMA Controller

12.5 Ethernet Interface

- Intel 82551ER Controller
- PCI DMA support
- 10Base-T / 100Base-TX Interface on RJ-45 front panel connector

12.6 Asynchronous Serial Interface

- Dual 16C550 compatible UART (1.8432 MHz clock-source)
- Port 1, Port 2 : RS232 configuration
- Max baud rate 115kbps
- Two DB9 front panel connectors

12.7 PCI Expansion Connector

- 32 bit 33 MHz PCI Interface (114-pin connector)
- 5V PCI Signaling Voltage (PCI Expansion Board may drive 3.3V or 5V PCI signal levels, PCI Expansion Board must tolerate 5V PCI signal levels)
- Supports Motorola PMC-Span, TEWS' IP-Span (TVME230)

12.8 IndustryPack Interface

12.8.1 Logic Interface

- Four single size / two double size IP slots
- Spaces available for each IP slot :
  128 byte I/O space, 64 byte ID space, 64 byte INT space, 8 Mbyte MEM space (16 bit), 4 Mbyte MEM space (8 bit)
- Data bus width : 16 bit
- Clock rate : 8 MHz / 32 MHz selectable for each IP slot

12.8.2 I/O Interface

- VME64x IndustryPack I/O on VME P0 & P2 connectors
- 0.75A max continuous dc current per IP I/O line

12.9 Power Supply

12.9.1 Power Supply Scheme

The TVME8300 uses the +5V, +12V and -12V power supply pins available on the VME P1 and P2 connectors as the main power supply.

The TVME8300 +3.3V power supply and other power supply voltages are derived from the +5V power supply on board.

12.9.2 Restrictions by VME Connectors

The VME P1 and P2 connectors are rated for 2A max @ 20°C (appr. 1.5A max @ 70°C) per pin.

For the +5V power supply there are 3 pins on the VME P1 connector and 3 + 2 pins on the VME P2 connector.

For the +12V power supply there is 1 pin on the VME P1 connector.

For the -12V power supply there is 1 pin on the VME P1 connector.

This must be considered for the total power supply load (on board load plus additional I/O load).

12.9.3 Power Supply Requirements

12.9.3.1 +5V Supply

On board load: Max 4A

Additional load (optional I/O):

- PCI Expansion Connector

  Unfused

- IP interface

  Available on all IP slots, max 2A per IP slot (limited by number of +5V pins on IP connector), max 2A total for IP slots A + B (IP slots A + B fused for a total of 2A), max 2A total for IP slots C + D (IP slots C + D fused for a total of 2A)

12.9.3.2 +12V Supply

On board load: Max 3mA

Not needed for board system function, only used in the +12V fuse status sensing logic

Additional load (optional I/O):

- PCI Expansion Connector

  Unfused, additional limit by connector pin max current

- IP Interface

  Available on all IP slots, max 1A per IP slot (limited by number of +12V pins on IP connector), max 2A total for all IP slots (IP slots A – D fused for a total of 2A)

12.9.3.3 -12V Supply

On board load: Max 3mA

Not needed for board system function, only used in the -12V fuse status sensing logic

Additional load (optional I/O):

- PCI Expansion Connector

  Unfused, additional limit by connector pin max current

- IP Interface

  Available on all IP slots, max 1A per IP slot (limited by number of -12V pins on IP connector), max 2A total for all IP slots (IP slots A – D fused for a total of 2A)

12.10 Physical Data

12.10.1 MTBF Data

(based on calculation)

TVME8300 Board Option	MTBF Value
TVME8300-10	210000 h

Figure 12-1 : MTBF Data

12.10.2 Temperature

Operating Temperature Range: 0°C to 55°C forced air cooling

Non-Operating Temperature Range: -40°C to 85°C

12.10.3 Weight

TVME8300-10 : 365g

12.10.4 Humidity

5% to 90% (Non-Condensing)

12.10.5 Form Factor

- One slot 6U VME
- 5-row (z, a, b, c, d) VME P1 & P2 connectors + VME64x P0 connector

(PCI expansion board occupies an additional VME slot if installed)