The Embedded I/O Company

TVME8400

PowerPC based CPU board

with two PMC Slots

Version 1.0

User Manual

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TVME8400

PowerPC based CPU board with two PMC Slots

TMVE8400-10R

MPC8245 300 MHz, 64 Mbyte SDRAM, 8 Mbyte Flash, Fast Ethernet, two PMC slots with front panel I/O and VME64x back I/O, Operating temperature range: 0°C to 55°C (forced air cooling)

TMVE8400-11R

Same as TVME8400-10R but with additional VME P0 connector for full PMC-2 back-I/O support

TMVE8400-20R

Same as TVME8400-10R but with 256 MB SDRAM

TMVE8400-21R

Same as TVME8400-10R but with 256 MB SDRAM and additional VME P0 connector for full PMC-2 back-I/O support

TVME8400-xxR-ET

Operating temperature range: -40°C to +85°C (forced air cooling)

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0	Initial Issue	January 2005
1.1	Ethernet Connector Type changed / Added LED description Added Extended Temperature Option	December 2005
1.2	Added Board Option TVME8400-20	June 2006
1.3	New address TEWS LLC	September 2006
1.0.4	New Notation for User Manual and Engineering Documentation	February 2010
1.0.5	(1) New board revision E supports mapping local PMC PCI interrupts to the VME bus. Added description, new chapter “Interrupt Routing”, new bit in the Control Register, new chapter “PMC Carrier”. (2) MPC8245 Configuration Register Setup modified (support Workarounds for MPC8245 Chip Errara No. 28): Processor Interface Configuration Register (0xAC) CB_OPT Bit, Address Map B Options Register (0xE0) PCMWB_OP Bit	September 2010
1.0.6	Added a sub-chapter for the TVME8400 bug monitor program (PMON)	December 2010
1.0.7	Added TVME8400-11 and TVME8400-21 board options for full PMC-2 back-I/O support	June 2011
1.0.8	Corrected Pin 1 Indication for the PMC Connectors in Board-I/O Overview Figure	November 2011
1.0.9	General Revision	August 2014

Table of Contents

1 INTRODUCTION 9
1.1 Block Diagram 9
1.2 Processor 10
1.3 Local Memory Bus 10
1.3.1 Socket Boot Flash 10
1.3.2 Board mounted Application Flash 10
1.3.3 SDRAM Memory 10
1.3.4 NVRAM / Real-Time Clock 10
1.3.5 16550 compatible Dual UART 10
1.3.6 Utility Registers 11
1.4 PCI Bus 11
1.5 VME Bus Interface 11
1.6 Ethernet Interface 11
1.7 PCI Mezzanine Card (PMC) Interface 12
1.8 PCI Expansion Interface 12
1.9 Asynchronous Serial Interface 12
1.10 Interrupts 13
1.11 LED Indicators 14
1.12 Front Panel Switch 14
2 ADDRESS MAPS 15
2.1 Address Map - Processor View 15
2.2 Address Map – PCI Memory Master View 16
2.3 Address Map – PCI I/O Master View 17
2.4 Address Map – Peripheral Devices Detail 17
2.5 Address Map – Utility Register Detail 18
2.5.1 Control Register 18
2.5.2 Status Register 19
2.5.3 Interrupt Register 19
2.5.4 LED Register 20
2.5.5 DIP Switch Register 20
2.5.6 PMC JTAG Register 21
3 MPC8245 22
3.1 Configuration Registers 22
3.1.1 Configuration Register Access 22
3.1.2 Configuration Register Settings 23
3.2 Programmable Interrupt Controller (PIC) 26
3.2.1 PIC Serial Interrupt Assignment 26
3.2.2 PIC Register Access 26
3.2.3 PIC Register Settings 26
3.2.3.1 Global Configuration Register (GCR) 26
3.2.3.2 Interrupt Configuration Register (ICR) 26
3.2.3.3 Serial Interrupt Vector / Priority Registers (SVPR) 26
3.2.4 PIC Register Programming 26
3.3 I2C Bus 27
3.3.1 I2C EEPROM 27
4 FLASH PROGRAMMING 28
4.1 8 bit Wide Socket Boot Flash 28
4.2 64 bit Wide On Board Application Flash 30
5 VME BUS INTERFACE 33
5.1 Universe-II PCI Header 33
5.2 Universe-II Power-Up Options 33

5.3 Universe-II Reset Signals 34
5.4 Universe-II Interrupts 34
5.5 Universe-II VME Bus Modes 34
6 ETHERNET INTERFACE 35
6.1 82551 PCI Header 35
6.2 82551 Configuration EEPROM 36
6.3 Media Capabilities 36
7 PCI BUS OVERVIEW 37
8 INTERRUPT ROUTING 38
8.1 TVME8400 Interrupt Sources 38
8.2 MPC8245 PIC Serial Interrupt Channel Assignment 38
8.3 Universe-II Interrupt Mapping Features 39
8.4 Extended PMC/EXP Slot Interrupt Routing 39
9 PMC CARRIER APPLICATION 42
9.1 TVME8400 as a passive PMC carrier 42
9.2 TVME8400 as an active PMC carrier 42
10 INSTALLATION AND USE NOTES 43
10.1 PMON Bug Monitor 43
10.2 NVRAM Real-Time Clock Control 43
11 BOARD I/O 45
11.1 Board I/O Overview 45
11.2 Jumper 46
11.2.1 Startup Jumper 46
11.2.2 VME System Controller Jumper 46
11.3 DIP Switch 47
11.4 LEDs 47
11.5 Push button Switch 48
11.6 Connectors 49
11.6.1 VME Interface Connectors 49
11.6.1.1 VME P1 Connector 49
11.6.1.2 VME P2 Connector 50
11.6.1.3 VME P0 Connector 51
11.6.2 PMC Interface Connectors 52
11.6.2.1 PMC 1 - J11 Connector (PCI, +5V) 52
11.6.2.2 PMC 1 - J12 Connector (PCI, +3.3V) 53
11.6.2.3 PMC 1 - J14 Connector (I/O) 54
11.6.2.4 PMC 2 - J21 Connector (PCI, +5V) 55
11.6.2.5 PMC 2 - J22 Connector (PCI, +3.3V) 56
11.6.2.6 PMC 2 - J24 Connector (I/O) 57
11.6.3 PCI Expansion Connector 58
11.6.4 Serial Interface Connectors 60
11.6.4.1 Serial Port 1 60
11.6.4.2 Serial Port 2 60
11.6.5 Ethernet Interface Connector 61
12 TECHNICAL INFORMATION 62
12.1 Processor 62
12.2 Memory 62
12.3 Other Devices 62
12.4 VME Interface 62
12.5 Ethernet Interface 63
12.6 Asynchronous Serial Interface 63
12.7 PCI Expansion Connector 63

12.8 PMC Interface 63
12.9 Power Requirements 63
12.10 Physical Data 64
12.10.1 MTBF 64
12.10.2 Temperature 64
12.10.3 Weight 64
12.10.4 Humidity 64
12.10.5 Form Factor 64

List of Figures

FIGURE 1-1 : BLOCK DIAGRAM TVME8400 9
FIGURE 8-1 : TVME8400 PMC/EXP SLOT INTERRUPT ROUTING SCHEME 41
FIGURE 11-1: BOARD I/O OVERVIEW 45
FIGURE 11-2 : FRONT PANEL VIEW 46
FIGURE 11-3: LAN LEDS ON RJ45 CONNECTOR 47

List of Tables

TABLE 2-1 : ADDRESS MAP – PROCESSOR VIEW 15
TABLE 2-2 : SUPPORTED TRANSFER SIZES 15
TABLE 2-3 : PCI ADDRESS TRANSLATION 16
TABLE 2-4 : ADDRESS MAP – PCI MEMORY MASTER VIEW 16
TABLE 2-5 : ADDRESS MAP – PCI I/O MASTER VIEW 17
TABLE 2-6 : ADDRESS MAP – PERIPHERAL DEVICES DETAIL 17
TABLE 2-7 : ADDRESS MAP – UTILITY REGISTER DETAIL 18
TABLE 2-8 : CONTROL REGISTER 18
TABLE 2-9 : STATUS REGISTER 19
TABLE 2-10: INTERRUPT REGISTER 19
TABLE 2-11: LED REGISTER 20
TABLE 2-12: DIP SWITCH REGISTER 20
TABLE 2-13: PMC JTAG REGISTER 21
TABLE 3-1 : MPC8245 CONFIGURATION REGISTER SETTINGS 25
TABLE 3-2 : I2C EEPROM CONTENT 27
TABLE 4-1 : BOOT FLASH COMMAND CYCLES 28
TABLE 4-2 : BOOT FLASH AUTO SELECT CODES 29
TABLE 4-3 : BOOT FLASH SECTOR MAP 29
TABLE 4-4 : APPLICATION FLASH COMMAND CYCLES 31
TABLE 4-5 : APPLICATION FLASH AUTO SELECT CODES 32
TABLE 4-6 : APPLICATION FLASH SECTOR MAP 32
TABLE 5-1 : UNIVERSE-II PCI HEADER 33
TABLE 6-1 : 82551 PCI HEADER 35
TABLE 6-2 : 82551 CONFIGURATION EEPROM SETTINGS 36
TABLE 7-1 : PCI BUS OVERVIEW 37
TABLE 8-1 : MPC8245 PIC SERIAL INTERRUPT CHANNEL ASSIGNMENT 39
TABLE 8-2 : TVME8400 PMC/EXP SLOT INTERRUPT ROUTING 40
TABLE 11-1: BOOT JUMPER 46
TABLE 11-2: VME SYSTEM CONTROLLER JUMPER 46
TABLE 11-3: LED INDICATION 47
TABLE 11-4: VME P1 CONNECTOR 49
TABLE 11-5: VME P2 CONNECTOR 50
TABLE 11-6: VME P0 CONNECTOR 51
TABLE 11-7: PMC 1 - J11 CONNECTOR 52
TABLE 11-8: PMC 1 - J12 CONNECTOR 53

TABLE 11-9: PMC 1 - J14 CONNECTOR....54
TABLE 11-10: PMC 2 - J21 CONNECTOR....55
TABLE 11-11: PMC 2 - J22 CONNECTOR....56
TABLE 11-12: PMC 2 - J24 CONNECTOR....57
TABLE 11-13: PCI EXPANSION CONNECTOR....59
TABLE 11-14: SERIAL PORT 1 (RS232) (RJ45 CONNECTOR)....60
TABLE 11-15: SERIAL PORT 2 (RS232) (RJ45 CONNECTOR)....60
TABLE 11-16: ETHERNET CONNECTOR (RJ45 CONNECTOR)....61
TABLE 12-1: MTBF DATA....64
TABLE 12-2: TEMPERATURE RANGE....64
TABLE 12-3: WEIGHT....64

1 Introduction

The TVME8400 is a standard 6U VMEbus single slot CPU board based on the MPC8245 Integrated Host PowerPC Processor with a G2 MPC603e CPU core, a powerful Memory Controller and PCI interface.

The TVME8400 provides two single size 32 bit 33 MHz PCI Mezzanine Card (PMC) slots with front I/O and VME 64x back I/O support.

All TVME8400 board options provide PMC-P4 I/O pin mapping according to ANSI/VITA 35-2000 “Mapping of single PMC-P4 to VME-P2-Rows-A,C” for PMC-1 I/O lines 1 to 64 and “Mapping of Single PMC-P4 to VME64x-P2-Rows-D,Z” for PMC-2 I/O lines 1 to 46. TVME8400-x1 board options also provide the VME P0 connector for PMC-2 I/O lines 47-64.

Other on-board I/O is a Fast Ethernet interface, a VME Master/Slave interface based on the Universe-II VME/PCI bridge chip, a dual UART (RS232) interface and a PCI expansion board connector.

On-board memory is 64 bit wide 8 Mbyte Flash, 64 bit wide 64 or 256 Mbyte SDRAM memory and 8 bit wide 8 Kbyte NVRAM/RTC.

1.1 Block Diagram

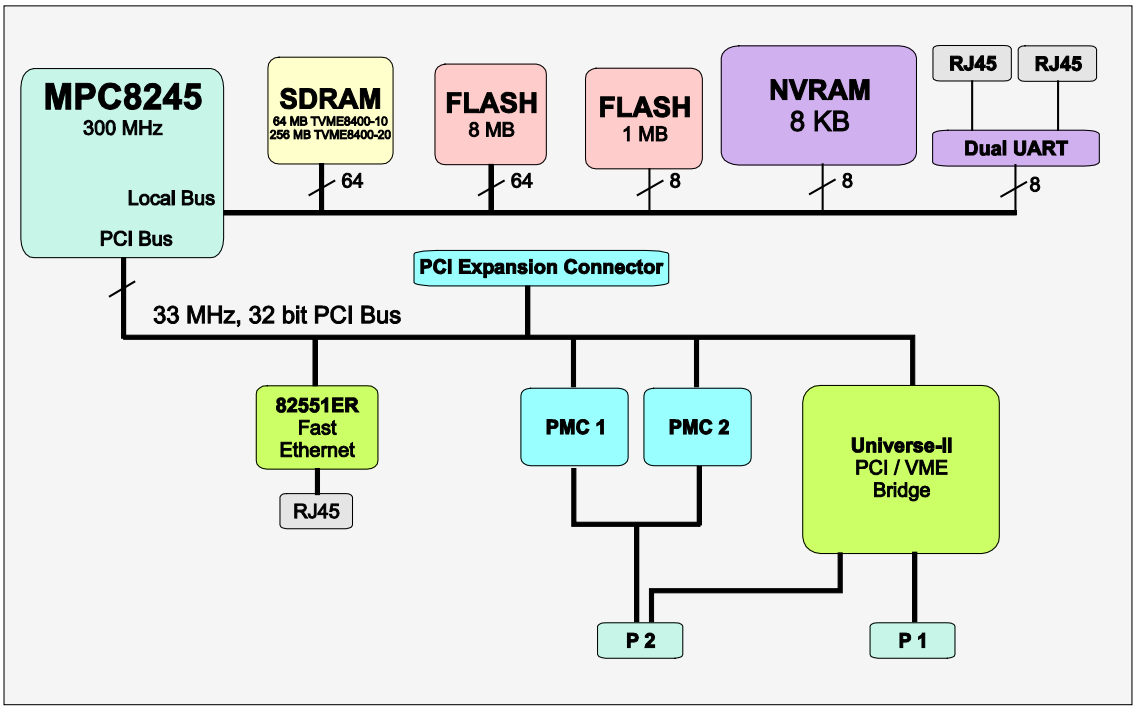

Figure 1-1 : Block diagram TVME8400

1.2 Processor

The TVME8400 uses the Motorola MPC8245 Integrated Host PowerPC processor.

Please refer to the MPC8245 documentation for details.

1.3 Local Memory Bus

The TVME8400 provides the following devices on the MPC8245 local memory bus:

- Socket Boot Flash (1 Mbyte, 8 bit wide)
- Board mounted Application Flash (8 Mbyte, 64 bit wide)
- SDRAM Memory
  (TVME8400-1x : 64 Mbyte, 64 bit wide)
  (TVME8400-2x : 256 Mbyte, 64 bit wide)
- NVRAM (8 Kbyte, 8 bit wide) / Real Time Clock / Watchdog (M48T59 or compatible)
- 16550 compatible Dual UART (8 bit wide)
- Utility Registers (8 bit wide)

1.3.1 Socket Boot Flash

The TVME8400 provides two 32-pin PLCC sockets, each populated with a 512 K x 8 bit Flash device for a total of 1 Mbyte 8 bit wide Boot Flash memory.

1.3.2 Board mounted Application Flash

The TVME8400 provides four 1 M x 16 bit on board Flash devices providing a total of 8 Mbyte 64 bit wide Application Flash storage (ask for extended Application Flash options).

1.3.3 SDRAM Memory

The TVME8400-1x provides 64 Mbyte 64 bit wide SDRAM memory build with four 8 M x 16 bit SDRAM devices.

The TVME8400-2x provides 256 Mbyte 64 bit wide SDRAM memory build with four 32 M x 16 bit SDRAM devices.

1.3.4 NVRAM / Real-Time Clock

The TVME8400 uses a ST M48T59 (or compatible) device to provide 8 Kbyte of non-volatile static RAM and real-time clock function.

The M48T59 (or compatible) device consists of two parts:

- A 28-pin 330mil SO device which contains the RTC, 8 Kbyte SRAM and sockets for the snaphat battery.
- A snaphat battery that is placed on top of the device.

Please refer to the M48T59 (or compatible) manual for details.

1.3.5 16550 compatible Dual UART

The TVME8400 uses the Exar XR16C2550 16550 compatible dual UART with a 1.8432 MHz clock source, providing two asynchronous serial RS232 ports.

Please refer to the XR16C2550 manual for details.

1.3.6 Utility Registers

The TVME8400 provides some additional registers for board control and status functions.

Please refer to the Address Maps section of this manual for details.

1.4 PCI Bus

The TVME8400 implements a 32 bit 33 MHz PCI bus.

The following devices are available on the TVME8400 PCI bus:

- MPC8245 Integrated Host PowerPC Processor (Motorola / Freescale)
- Universe-II VME / PCI Bridge (Tundra)
- 82551 Fast Ethernet Controller (Intel)
- Optional PCI Devices on PMC Slot 1, PMC Slot 2
- Optional PCI Devices on PCI Expansion Connector (e.g. PMC-Span, IP-Span)

The MPC8245 integrated PCI Arbiter is used for PCI bus arbitration.

Please see the PCI Bus Overview section in this manual for more details.

1.5 VME Bus Interface

The TVME8400 uses the Tundra Universe-II VME / PCI Bridge for the VME bus interface.

The Universe-II VME / PCI Bridge provides a 32 bit address / 32 bit data VME bus Master / Slave interface.

Please refer to the Universe-II documentation for details.

1.6 Ethernet Interface

The TVME8400 uses the Intel 82551 Fast Ethernet Controller for the Ethernet interface.

An IEEE 802.3 10Base-T / 100Base-TX interface is available on an 8-pin RJ45 connector at the TVME8400 front panel. The RJ45 connector provides two LEDs indicating Speed and Link/Activity status.

Please refer to the 82551 manual for details.

1.7 PCI Mezzanine Card (PMC) Interface

The TVME8400 provides two 32 bit 33 MHz single size PCI Mezzanine Card (PMC) slots, with front I/O and VME back I/O support.

The following PMC I/O signals are available for VME back I/O:

All PMC 1 I/O lines 1 to 64 are available at the VME P2 connector rows a & c.

PMC 2 I/O lines 1 to 46 are available at the VME P2 connector rows z & d.

PMC 2 I/O lines 47 to 64 are available at the VME P0 connector (TVME8400-x1 board options only).

1.8 PCI Expansion Interface

The TVME8400 provides a 114-pin PCI expansion connector for using existing 6U VME PCI Expansion Boards (e.g. Motorola PMC-Span or TEWS' IP-Span TVME230).

By the use of a PCI Expansion board, it is possible to have 2 more PMC slots or 4 additional IndustryPack Slots.

1.9 Asynchronous Serial Interface

The TVME8400 provides two asynchronous RS232 serial interface ports used with the on board Dual UART.

Both serial ports are available on RJ45 connectors at the front panel.

1.10 Interrupts

The following interrupt sources are available:

- Utility Interrupt Register
- ABORT Switch
- 82551 (Fast Ethernet Controller)
- Alarm / Watchdog (NVRAM / RTC Device)
- PMC / EXP Slot INT0 (Shared)
- PMC / EXP Slot INT1 (Shared)
- PMC / EXP Slot INT2 (Shared)
- PMC / EXP Slot INT3 (Shared)
- Universe-II LINT0 (VME / PCI Bridge)
- Universe-II LINT1 (VME / PCI Bridge)
- Universe-II LINT2 (VME / PCI Bridge)
- Universe-II LINT3 (VME / PCI Bridge)
- UART Channel 1
- UART Channel 2

All interrupt sources are forwarded to the TVME8400 MPC8245 Programmable Interrupt Controller (PIC). The MPC8245 PIC is used in serial mode, so each interrupt source is mapped to a certain serial channel of the MPC8245 PIC.

The Universe-II LINT#[0:3] pins are bidirectional and can be used as inputs or open drain outputs.

By default, the Universe-II LINT#[0:3] pins are used as outputs mapped to the MPC8245 PIC.

The TVME8400 Control Register (0xFFE40000) provides an option for mapping the PMC / EXP Slot PCI interrupts to both the MPC8245 PIC and the Universe-II LINT#[0:3] pins. In this case Universe-II LINT# pins may be used as inputs for mapping TVME8400 PMC PCI interrupts to the VME bus.

Please see the MPC8245 PIC section in this manual for more details.

Please see the Universe-II Interrupt section in this manual for more details.

Please see the Interrupt Routing chapter in this manual for more details.

1.11 LED Indicators

The TVME8400 provides a (bi-color) LED status indicator at the front panel.

The following LED indications are available:

- Board Activity (Green)
- Board Failure (Red)

Please see the Board I/O section in this manual for more details.

Additionally the RJ45 LAN connector at the front panel provides two LEDs, indicating Speed and Link/Activity status of the Ethernet interface.

1.12 Front Panel Switch

The TVME8400 provides a momentary push button switch at the front panel.

The following switch functions are available:

- Abort (CPU Interrupt)
- Reset (Board Reset)

Please see the Board I/O section in this manual for more details.

2 Address Maps

The following address maps reflect certain MPC8245 configuration register settings done by the board initialization software.

2.1 Address Map - Processor View

Processor Address		Size (Byte)	Description
Start	End		
0x0000_0000	0x03FF_FFFF 0x0FFF_FFFF	64 M Opt. 256 M Opt.	SDRAM Memory (64 bit wide)
0x0400_0000	0x0FFF_FFFF	256 M - 64 M	Reserved for 64 Mbyte RAM Opt.
0x1000_0000	0x6FFF_FFFF	2 G - 512 M	Reserved
0x7000_0000	0x707F_FFFF	8 M	Application Flash (64 bit wide)
0x7080_0000	0x7FFF_FFFF	256 M – 8 M	Reserved
0x8000_0000	0xFCEF_FFFF	2 G – 49 M	PCI MEM Space
0xFCF0_0000	0xFCFF_FFFF	1 M	MPC8245 EUMB
0xFD00_0000	0xFDFF_FFFF	16 M	PCI MEM Space (0-based)
0xFE00_0000	0xFE00_FFFF	64 K	PCI I/O Space (0-based)
0xFE01_0000	0xFE7F_FFFF	8 M – 64 K	Reserved
0xFE80_0000	0xFEBF_FFFF	4 M	PCI I/O Space (0-based)
0xFEC0_0000	0xFEDF_FFFF	2 M	Configuration Address Register
0xFEE0_0000	0xFEEF_FFFF	1 M	Configuration Data Register
0xFEF0_0000	0xFEFF_FFFF	1 M	PCI Interrupt Acknowledge
0xFF00_0000	0xFF7F_FFFF	8 M	Reserved
0xFF80_0000	0xFFDF_FFFF	6 M	Reserved
0xFFE0_0000	0xFFEF_FFFF	1 M	Peripheral Devices (8 bit wide)
0xFFF0_0000	0xFFFF_FFFF	1 M	Boot Flash (8 bit wide)

Table 2-1 : Address Map – Processor View

Device	Read	Write
SDRAM	All	All
Application Flash	All	64 bit Only
Boot Flash	All	8 bit Only
Peripheral Devices	8 bit Only	8 bit Only

Table 2-2 : Supported Transfer Sizes

Processor Address		Translated PCI Address		PCI Space
Start	End	Start	End	
0x8000_0000	0xFCEF_FFFF	0x8000_0000	0xFCEF_FFFF	MEM
0xFD00_0000	0xFDFF_FFFF	0x0000_0000	0x00FF_FFFF	MEM
0xFE00_0000	0xFE00_FFFF	0x0000_0000	0x0000_FFFF	I/O
0xFE80_0000	0xFEBF_FFFF	0x0080_0000	0x00BF_FFFF	I/O

Table 2-3 : PCI Address Translation

2.2 Address Map – PCI Memory Master View

PCI Memory Address		Size (Byte)	Description
Start	End		
0x0000_0000	0x03FF_FFFF 0x0FFF_FFFF	64 M Opt. 256 M Opt.	SDRAM Memory (64 bit wide)
0x0400_0000	0x0FFF_FFFF	256 M – 64 M	Reserved for 64 Mbyte RAM Opt.
0x1000_0000	0x6FFF_FFFF	1 G – 512 M	Reserved
0x7000_0000	0x707F_FFFF	8 M	Application Flash (64 bit wide)
0x7080_0000	0x7FFF_FFFF	256 M – 8 M	Reserved
0x8000_0000	0xFCEF_FFFF	2 G – 49 M	PCI Memory Space
0xFCF0_0000	0xFCF0_0FFF	4 K	PCI accessible MPC8245 EUMB
0xFCF0_1000	0xFCFF_FFFF	1 M – 4 K	Reserved
0xFD00_0000	0xFDFF_FFFF	16 M	SDRAM Memory (0-Based)
0xFE00_0000	0xFEFF_FFFF	16 M	Reserved
0xFF00_0000	0xFF7F_FFFF	8 M	Reserved
0xFF80_0000	0xFFDF_FFFF	6 M	Reserved
0xFFE0_0000	0xFFEF_FFFF	1 M	Peripheral Devices (8 bit wide)
0xFFF0_0000	0xFFFF_FFFF	1 M	Boot Flash (8 bit wide)

Table 2-4 : Address Map – PCI Memory Master View

On the TVME8400 the MPC8245 responds as a target to PCI Memory cycles for accessing SDRAM, PCI accessible MPC8245 EUMB, Application Flash, Peripheral Devices and Boot Flash.

2.3 Address Map – PCI I/O Master View

PCI I/O Address		Size (Byte)	Description
Start	End		
0x0000_0000	0x0000_FFFF	64 K	PCI I/O Space
0x0001_0000	0x007F_FFFF	8 M – 64 K	Reserved
0x0080_0000	0x00BF_FFFF	4 M	PCI I/O Space
0x00C0_0000	0xFFFF_FFFF	4 G – 12 M	Reserved

Table 2-5 : Address Map – PCI I/O Master View

The MPC8245 does not respond as a target to PCI I/O cycles.

2.4 Address Map – Peripheral Devices Detail

Address		Size (Byte)	Description
Start	End		
0xFFE0_0000	0xFFE0_1FFF	8 K	NVRAM / RTC
0xFFE0_2000	0xFFE3_FFFF	256 K – 8 K	Reserved
0xFFE4_0000	0xFFE4_0007	8	UTILITY REG
0xFFE4_0007	0xFFE7_FFFF	256 K – 8	Reserved
0xFFE8_0000	0xFFE8_0007	8	UART CH 1
0xFFE8_0008	0xFFE8_000F	8	UART CH 2
0xFFE8_0010	0xFFEF_FFFF	512 K -16	Reserved

Table 2-6 : Address Map – Peripheral Devices Detail

For read or write accesses to the Peripheral Devices only 8 bit (byte) transfer sizes are allowed.

For the NVRAM / RTC register map please refer to the M48T59 (or compatible) device documentation.

For the UART register map please refer to the XR16C2550 documentation.

2.5 Address Map – Utility Register Detail

Address	Size (Byte)	Register Name
0xFFE4_0000	1	CONTROL
0xFFE4_0001	1	STATUS
0xFFE4_0002	1	INTERRUPT
0xFFE4_0003	1	LED
0xFFE4_0004	1	DIP_SWITCH
0xFFE4_0005	1	PMC_JTAG
0xFFE4_0006	1	Reserved
0xFFE4_0007	1	Reserved

Table 2-7 : Address Map – Utility Register Detail

2.5.1 Control Register

Bit	Name	Access	Reset	Function
0 (MSB)	BOARD_RST	R/W	0	0: Normal Board Operation 1: Assert Board Reset
1	I2C_EEP_WE	R/W	0	0: I2C EEPROM Writes Disabled 1: I2C EEPROM Writes Enabled
2	APP_FLASH_WE	R/W	0	0: Application Flash Writes Disabled 1: Application Flash Writes Enabled
3	BOOT_FLASH_WE	R/W	0	0: Boot Flash Writes Disabled 1: Boot Flash Writes Enabled
4	PMC_INT_MAP	R/W	0	0: Shared PMC PCI Interrupt Lines are routed to the MPC8245 Interrupt Controller 1: Shared PMC PCI Interrupt Lines are routed to both the MPC8245 Interrupt Controller and to the Universe-II LINT#[0:3] lines (per open-drain driver)
5	Reserved	-	-	Write as '0' Undefined for Reads
6				
7 (LSB)				

Table 2-8 : Control Register

A board reset will perform a general board hardware reset, PCI reset and CPU reset.

If the TVME8400 is the VME system controller, a board reset will also generate a VME system reset.

2.5.2 Status Register

Bit	Name	Access	Reset	Function
0 (MSB)	STARTUP_JMP	R	-	0: Startup Jumper Pos. 2-3 (Run from Boot Flash after board initialization) (Bug Monitor) 1: Startup Jumper Pos. 1-2 (or open) (Run from Application Flash after board initialization) (User Application)
1	PCI_EXP_PRSNT	R	-	0: PCI Expansion Board not Present 1: PCI Expansion Board Present
2	PMC1_PRSNT	R	-	0: PMC1 not Present 1: PMC1 Present
3	PMC2_PRSNT	R	-	0: PMC2 not Present 1: PMC2 Present
4	ABORT	R	-	0: ABORT Pushbutton Switch Open 1: ABORT Pushbutton Switch Closed
5	SYSCON	R	-	0: Not VME System Controller 1: VME System Controller
6	Reserved	-	-	Undefined for Reads
7 (LSB)				

Table 2-9 : Status Register

The Startup Jumper function is reserved by the (factory default) board initialization software.

2.5.3 Interrupt Register

Bit	Name	Access	Reset	Function
0 (MSB)	USR_INT	R/W	0	0: Clear User Interrupt 1: Assert User Interrupt
1	Reserved	-	-	Write as '0' Undefined for Reads
2				
3				
4				
5				
6				
7 (LSB)				

Table 2-10: Interrupt Register

The User Interrupt is mapped to serial interrupt channel 0 of the MPC8245 PIC.

2.5.4 LED Register

Bit	Name	Access	Reset	Function
0 (MSB)	FAIL_LED	R/W	0	0: Set Fail LED Off 1: Set Fail LED On
1	Reserved	-	-	Write as '0' Undefined for Reads
2				
3				
4				
5				
6				
7 (LSB)				

Table 2-11: LED Register

If the Fail LED (red) is set by the user, the activity LED (green) is turned off.

2.5.5 DIP Switch Register

Bit	Name	Access	Reset	Function
0 (MSB)	DIP_SW_POS_1	R	-	0: Switch Open (Off) 1: Switch Closed (On)
1	DIP_SW_POS_2	R	-	0: Switch Open (Off) 1: Switch Closed (On)
2	DIP_SW_POS_3	R	-	0: Switch Open (Off) 1: Switch Closed (On)
3	DIP_SW_POS_4	R	-	0: Switch Open (Off) 1: Switch Closed (On)
4	DIP_SW_POS_5	R	-	0: Switch Open (Off) 1: Switch Closed (On)
5	DIP_SW_POS_6	R	-	0: Switch Open (Off) 1: Switch Closed (On)
6	DIP_SW_POS_7	R	-	0: Switch Open (Off) 1: Switch Closed (On)
7 (LSB)	DIP_SW_POS_8	R	-	0: Switch Open (Off) 1: Switch Closed (On)

Table 2-12: DIP Switch Register

2.5.6 PMC JTAG Register

Bit	Name	Access	Reset	Function
0 (MSB)	PMC_TRST#	R/W	0	0: Set PMC TRST# JTAG Signal to Low 1: Set PMC TRST# JTAG Signal to High
1	PMC_TCK	R/W	0	0: Set PMC TCK JTAG Signal to Low 1: Set PMC TCK JTAG Signal to High
2	PMC_TMS	R/W	1	0: Set PMC TMS JTAG Signal to Low 1: Set PMC TMS JTAG Signal to High
3	PMC_TDI_OUT	R/W	0	0: Set PMC TDI JTAG Signal to Low 1: Set PMC TDI JTAG Signal to High
4	PMC_TDO_IN	R	-	0: PMC TDO JTAG Signal is Low 1: PMC TDO JTAG Signal is High
5	Reserved	-	-	Undefined for Reads. Write as 0.
6				
7 (LSB)				

Table 2-13: PMC JTAG Register

The PMC_TDI_OUT signal connects to the TDI pin on the PMC 1 J12 connector.

The PMC_TDO_IN signal connects to the TDO pin of the PMC 2 J22 connector.

3 MPC8245

The TVME8400 uses the MPC8245 in host mode with address map B.

The MPC8245 processor and peripheral logic are configured to operate in big endian mode.

3.1 Configuration Registers

Setting up the MPC8245 Configuration Registers is scope of the board initialization software.

Configuration Register settings are shown for information only and may not reflect the settings for the actual revision of the board initialization software.

3.1.1 Configuration Register Access

The MPC8245 Configuration Registers are accessed in two steps:

1. A 32 bit value 0x8000_00nn is written to the CONFIG_ADDR port at 0xFEC0_0000, where nn is the (word-aligned) register offset (e.g. 0x00, 0x04, 0x08, ...).
2. Data is accessed at the CONFIG_DATA port at 0xFEE0_000m, where m is the offset within the word-aligned address (depending on transfer size).

Data can be accessed multiple times at the CONFIG_DATA port until the CONFIG_ADDR port value is changed.

All of the MPC8245 Configuration Registers are intrinsically little endian. Therefore all of the following Configuration Register settings are shown in little endian order.

Since on the TVME8400 the MPC8245 processor and peripheral logic operates in big endian mode, software must either use byte reversed load / store instructions or byte-swap the values for the CONFIG_ADDR and CONFIG_DATA port access.

E.g. for reading the Device ID Register (offset 0x02) one should write 0x0000_0080 (0x00 is the word-aligned offset for 0x02) to 0xFEC0_0000 and read the half-word 0x0600 at 0xFEE0_0002.

E.g. for setting the Output Driver Control Register (offset 0x73) one should write 0x7000_0080 (0x70 is the word-aligned offset for 0x73) to 0xFEC0_0000 and write the byte 0xD5 to 0xFEE0_0003.

E.g. for setting the EUMBBAR Register (offset 0x78) to 0xFCF0_0000 one should write 0x78000080 to 0xFEC0_0000 and write the word 0x0000F0FC to 0xFEE0_0000.

3.1.2 Configuration Register Settings

Register Offset	Register Description	Size (Byte)	Access Type	Setting
0x00	Vendor ID	2	R	0x1057
0x02	Device ID	2	R	0x0006
0x04	PCI Command Register	2	R/W	0x0006
0x06	PCI Status Register	2	R/C	*status*
0x08	Revision ID	1	R	*revision*
0x09	Standard Programming Interface	1	R	0x00
0x0A	Subclass Code	1	R	0x00
0x0B	Class Code	1	R	0x06
0x0C	Cache Line Size	1	R/W	*reset_default*
0x0D	Latency Timer	1	R/W	*reset_default*
0x0E	Header Type	1	R	0x00
0x0F	BIST Control	1	R	0x00
0x10	Local Memory Base Address Register 0	4	R/W	*reset_default*
0x14	Peripheral Control Status Register Base Address Register	4	R/W	*reset_default*
0x18	Local Memory Base Address Register 1	4	R/W	*reset_default*
0x2C	Subsystem Vendor ID	2	R/W	0x0000
0x2E	Subsystem ID	2	R/W	0x0000
0x30	Expansion ROM Base Address	4	R	0x0000_0000
0x3C	Interrupt Line	1	R/W	*reset_default*
0x3D	Interrupt Pin	1	R	0x01
0x3E	MIN GNT	1	R	0x00
0x3F	MAX LAT	1	R	0x00
0x40	Bus Number	1	R/W	*reset_default*
0x41	Subordinate Bus Number	1	R/W	*reset_default*
0x44	PCI General Control Register	2	R/W	0x0000
0x46	PCI Arbiter Control Register	2	R/W	0x8400
0x70	Power Management Configuration Register 1	2	R/W	0xC001
0x72	Power Management Configuration Register 2	1	R/W	0x20
0x73	Output Driver Control Register	1	R/W	0xD5
0x74	Clock Driver Control Register	2	R/W	0x0000
0x76	Misc. I/O Control Register 1	1	R/W	0x00
0x77	Misc. I/O Control Register 2	1	R/W	0x20
0x78	Embedded Utilities Memory Block Base Address (EUMBBAR)	4	R/W	0xFCF0_0000
0x80, 0x84	Memory Starting Address Registers	4	R/W	64 Mbyte Opt. : 0x8080_8000, 0x8080_8080

Register Offset	Register Description	Size (Byte)	Access Type	Setting
				256 Mbyte Opt. : 0x0000_0000, 0x0000_0000
0x88, 0x8C	Extended Memory Starting Address Registers	4	R/W	64 Mbyte Opt. : 0x0000_0000, 0x0000_0000 256 Mbyte Opt. : 0x0101_0100, 0x0101_0101
0x90, 0x94	Memory Ending Address Registers	4	R/W	64 Mbyte Opt. : 0x8F8F_8F3F, 0x8F8F_8F8F 256 Mbyte Opt. : 0xFFFF_FFFF, 0xFFFF_FFFF
0x98, 0x9C	Extended Memory Ending Address Registers	4	R/W	64 Mbyte Opt. : 0x0000_0000, 0x0000_0000 256 Mbyte Opt. : 0x0101_0100, 0x0101_0101
0xA0	Memory Bank Enable Register	1	R/W	0x01
0xA3	Page Mode Register	1	R/W	0x00
0xA8	Processor Interface Configuration Register 1	4	R/W	0x0014_1B98
0xAC	Processor Interface Configuration Register 2	4	R/W	0x2000_0601
0xB8	ECC Single Bit Error Counter Register	1	R/W	*status*
0xB9	ECC Single Bit Error Trigger Register	1	R/W	*reset_default*
0xC0	Error Enabling Register 1	1	R/W	*reset_default*
0xC1	Error Detection Register 1	1	R/C	*status*
0xC3	Processor Internal Bus Error Status Register	1	R/C	*status*
0xC4	Error Enabling Register 2	1	R/W	*reset_default*
0xC5	Error Detection Register 2	1	R/C	*status*
0xC7	PCI Bus Error Status Register	1	R/C	*status*
0xC8	Processor/PCI Error Address Register	4	R	*status*
0xD0	Extended ROM Configuration Register 1	4	R/W	0x35FF_8000
0xD4	Extended ROM Configuration Register 2	4	R/W	0xB5FF_8000
0xD8	Extended ROM Configuration Register 3	4	R/W	0x0C00_000E
0xDC	Extended ROM Configuration Register 4	4	R/W	0x0000_000B
0xE0	Address Map B Options Register (AMBOR)	1	R/W	0xC1
0xE1	PCI/Memory Buffer Configuration Register	1	R/W	0x00
0xE2	PLL Configuration Register	1	R	0x08
0xF0	Memory Control Configuration Register 1 (MCCR1)	4	R/W	64 Mbyte Opt. : 0x0468_0000 256 Mbyte Opt. :

Register Offset	Register Description	Size (Byte)	Access Type	Setting
				0x0468_0002
0xF4	Memory Control Configuration Register 2 (MCCR2)	4	R/W	64 Mbyte Opt. : 0x0A60_1800 256 Mbyte Opt. : 0x0A60_0BC0
0xF8	Memory Control Configuration Register 3 (MCCR3)	4	R/W	0x0700_0000
0xFC	Memory Control Configuration Register 4 (MCCR4)	4	R/W	0x2730_2220

Table 3-1 : MPC8245 Configuration Register Settings

Board initialization software notes :

The MEMGO bit in the MCCR1 register (offset 0xF0) must not be set until all other memory configuration parameters have been appropriately configured.

The DLL_RESET bit in the AMBOR register (offset 0xE0) must be explicitly set and then cleared by software during initialization.

3.2 Programmable Interrupt Controller (PIC)

The TVME8400 uses the MPC8245 Programmable Interrupt Controller (PIC) in serial mode as the board interrupt controller.

3.2.1 PIC Serial Interrupt Assignment

All TVME8400 interrupt sources are mapped to serial channels of the MPC8245 PIC.

Please see the Interrupt Routing chapter in this manual for more details.

3.2.2 PIC Register Access

The PIC Registers are part of the MPC8245 Embedded Utility Memory Block (EUMB).

The EUMB base address is set in the EUMBBAR Register.

For the TVME8400 memory map the EUMB base address is set to 0xFCF0_0000.

3.2.3 PIC Register Settings

3.2.3.1 Global Configuration Register (GCR)

Offset from EUMBBAR: 0x4_1020

The mode bit in the GCR must be set for PIC mixed mode operation.

3.2.3.2 Interrupt Configuration Register (ICR)

Offset from EUMBBAR: 0x4_1030

The ICR clock ratio field should be set to 0x2 (value must be >= 0x2) (value of 0x2 sets the serial interrupt clock rate to approx. 25MHz).

The ICR SIE bit must be set to enable Serial Interrupt Mode.

3.2.3.3 Serial Interrupt Vector / Priority Registers (SVPR)

The polarity and sense bits in the SVPRs must be configured accordingly to the PIC Serial Interrupt Assignment table in the Interrupt Routing chapter.

3.2.4 PIC Register Programming

The PIC Programming Guidelines from the MPC8245 manual should be followed.

3.3 I2C Bus

The TVME8400 provides an on board I2C EEPROM for board specific data.

3.3.1 I2C EEPROM

EEPROM Offset	Description	Content
0x00	Check sum	See note below
0x01	Number Of Valid Bytes Following	0x06
0x02	Board Type (High Byte)	0x20D0 for TVME8400
0x03	Board Type (Low Byte)	
0x04	Board Option (High Byte)	e.g. 0x000A for TVME8400-10R
0x05	Board Option (Low Byte)	
0x06	Board Version (Major)	V <major>.<minor> e.g. 0x0100 = V1.0
0x07	Board Version (Minor)	
0x08 ... 0x0F	Factory Reserved	
0x10 ... 0xFF	Reserved	

Table 3-2 : I2C EEPROM Content

The address of the on board I2C EEPROM is 0b000.

Writes to the on board I2C EEPROM must be enabled in the Utility Control Register.

The check sum is the 2's-complement of the lower byte of the sum of all used locations of the I2C EEPROM, except the check sum byte.

4 Flash Programming

4.1 8 bit Wide Socket Boot Flash

The TVME8400 provides 1 Mbyte of 8 bit wide socket Boot Flash using two 512 K x 8 bit 32-pin PLCC Flash devices.

The Boot Flash address range is 0xFFF0_0000 to 0xFFFF_FFFF (1 Mbyte).

Boot Flash Socket XU1 is for the lower 512 Kbyte address range (0xFFF0_0000 to 0xFFF7_FFFF).

Boot Flash Socket XU2 is for the upper 512 Kbyte address range (0xFFF8_0000 to 0xFFFF_FFFF).

For writes to the Boot Flash, byte (8 bit) transfer sizes must be used.

Writes to the Boot Flash must be enabled in the Utility Control Register.

The 8 bit wide socket Boot Flash (Socket XU1) must always be installed and provide the board initialization code at the system reset vector (0xFFF0_0100).

Command Sequence	Cycles	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	RA	RD										
Reset	1	Base+ 0x000	0xF0										
Auto Select	4	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	Base+ 0x555	0x90	Base+ 0x000	MID				
								Base+ 0x001	DID				
Write	4	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	Base+ 0x555	0xA0	WA	WD				
Chip Erase	6	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	Base+ 0x555	0x80	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	Base+ 0x555	0x10
Sector Erase	6	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	Base+ 0x555	0x80	Base+ 0x555	0xAA	Base+ 0x2AA	0x55	SAx	0x30

Table 4-1 : Boot Flash Command Cycles

All Boot Flash command cycles are write cycles except the 1st cycle of the Read command and the 4th cycle of the Auto Select command (which are read cycles).

The base address for the lower 512 Kbyte Boot Flash device is 0xFFF0_0000.

The base address for the upper 512 Kbyte Boot Flash device is 0xFFF8_0000.

For Write commands poll for RD = WD from RA = WA after the 4th cycle.

For Erase commands poll for RD = 0xFF from the Boot Flash device base address for Chip Erase or from SAx for Sector Erase after the 6th cycle.

Symbols:

DID = Device ID, MID = Manufacturer ID, RA = Read Address, RD = Read Data,

SA = Sector Address, WA = Write Address, WD = Write Data

Manufacturer	Device	Manufacture ID	Device ID
AMD	29F040B	0x01	0xA4
ST	29F040B	0x20	0xE2

Table 4-2 : Boot Flash Auto Select Codes

Sector	Sector Size (Byte)	Sector Address Range
SA0	64 K	0xFFF0_0000 - 0xFFF0_FFFF
SA1	64 K	0xFFF1_0000 - 0xFFF1_FFFF
SA2	64 K	0xFFF2_0000 - 0xFFF2_FFFF
SA3	64 K	0xFFF3_0000 - 0xFFF3_FFFF
SA4	64 K	0xFFF4_0000 - 0xFFF4_FFFF
SA5	64 K	0xFFF5_0000 - 0xFFF5_FFFF
SA6	64 K	0xFFF6_0000 - 0xFFF6_FFFF
SA7	64 K	0xFFF7_0000 - 0xFFF7_FFFF
SA8	64 K	0xFFF8_0000 - 0xFFF8_FFFF
SA9	64 K	0xFFF9_0000 - 0xFFF9_FFFF
SA10	64 K	0xFFFA_0000 - 0xFFFA_FFFF
SA11	64 K	0xFFFB_0000 - 0xFFFB_FFFF
SA12	64 K	0xFFFC_0000 - 0xFFFC_FFFF
SA13	64 K	0xFFFD_0000 - 0xFFFD_FFFF
SA14	64 K	0xFFFE_0000 - 0xFFFE_FFFF
SA15	64 K	0xFFFF_0000 - 0xFFFF_FFFF

Table 4-3 : Boot Flash Sector Map

4.2 64 bit Wide On Board Application Flash

The TVME8400 provides 8 Mbyte of 64 bit wide board mounted Application Flash using four 1 M x 16 bit Flash devices.

The Application Flash address range is 0x7000_0000 to 0x707F_FFFF.

For writes to the Application Flash, double-word (64 bit) transfer sizes must be used.

Writes to the Application Flash must be enabled in the Utility Control Register.

For 64 bit writes to the Application Flash, the processor may issue a single-beat 64 bit write, using a caching-inhibited stfd (store floating point double), with the data in a Floating Point Register (FPR).

Cmd.-Seq.	#Cyc	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read	1	RA	RD										
Reset	1	Base + 0x0_0000	0x00F000F0 00F000F0										
Auto Select	4	Base + 0x2_AAA8	0x00AA00AA 00AA00AA	Base + 0x1_5550	0x00550055 00550055	Base + 0x2_AAA8	0x00900090 00900090	Base + 0x0_0000	MID				
								Base + 0x0_0008	DID				
Write	4	Base + 0x2_AAA8	0x00AA00AA 00AA00A	Base + 0x1_5550	0x00550055 00550055	Base + 0x2_AAA8	0x00A000A0 00A000A0	WA	WD				
Chip Erase	6	Base + 0x2_AAA8	0x00AA00AA 00AA00A	Base + 0x1_5550	0x00550055 00550055	Base + 0x2_AAA8	0x00800080 00800080	Base + 0x2_AAA8	0x00AA00AA 00AA00A	Base + 0x1_5550	0x00550055 00550055	Base + 0x2_AAA8	0x00100010 00100010
Sector Erase	6	Base + 0x2_AAA8	0x00AA00AA 00AA00A	Base + 0x1_5550	0x00550055 00550055	Base + 0x2_AAA8	0x00800080 00800080	Base + 0x2_AAA8	0x00AA00AA 00AA00A	Base + 0x1_5550	0x00550055 00550055	SAx	0x00300030 00300030

Table 4-4 : Application Flash Command Cycles

All the Application Flash command cycles are write cycles except the 1st cycle of the Read command and the 4th cycle of the Auto Select command (which are read cycles).

The Application Flash base address is 0x7000_0000.

For Write commands poll for RD = WD from RA = WA after the 4th cycle.

For Erase commands poll for RD = 0xFFFFFFFFFFFFFFFF from the Application Flash base address for Chip Erase or from SAx for Sector Erase after the 6th cycle.

Symbols:

DID = Device ID, MID = Manufacturer ID, RA = Read Address, RD = Read Data,

SA = Sector Address, WA = Write Address, WD = Write Data

Manufacturer	Device	Manufacturer ID	Device ID
SST	39VF160	0x00BF00BF00BF00BF	0x2782278227822782
SST	39VF1601	0x00BF00BF00BF00BF	0x234B234B234B234B
SST	39VF1602	0x00BF00BF00BF00BF	0x234A234A234A234A

Table 4-5 : Application Flash Auto Select Codes

Sector	Sector Size (Byte)	Sector Address Range
SST 39xF160x (Uniform)		
SA0	16 K	0x7000_0000 - 0x7000_3FFF
SA1	16 K	0x7000_4000 - 0x7000_7FFF
SA2	16 K	0x7000_8000 - 0x7000_BFFF
SA3	16 K	0x7000_C000 - 0x7000_FFFF
SA4	16 K	0x7001_0000 - 0x7001_3FFF
…	…	…
SA511	16 K	0x707F_C000 - 0x707F_FFFF

Table 4-6 : Application Flash Sector Map

5 VME Bus Interface

The Tundra Universe-II VME / PCI bridge is used as the TVME8400 VME / PCI bridge.

The Universe-II is accessible on both the VME bus and the TVME8400 PCI bus (device number 13).

Please refer to the Universe-II manual for a detailed description of the Universe-II VME / PCI bridge.

5.1 Universe-II PCI Header

Offset	PCI Configuration Register				Setting
	31 - 24	23 - 16	15 - 08	07 - 00	
0x00	Device ID		Vendor ID		0x0000_10E3
0x04	Status		Command		0x0200_0007
0x08	Class Code			Revision ID	0x0680_0002
0x0C	Reserved	Header	Latency	Cache Line	0x0000_xx00
0x10	PCI Base Address 0 (Configuration Register I/O Mapped)				0xFFFF_F001(1) (4 Kbyte)
0x14	PCI Base Address 1 (Configuration Register Memory Mapped)				0xFFFF_F000(1) (4 Kbyte)
0x18	PCI Unimplemented				0x0000_0000
0x1C	PCI Unimplemented				0x0000_0000
0x20	PCI Unimplemented				0x0000_0000
0x24	PCI Unimplemented				0x0000_0000
0x28	PCI Reserved				0x0000_0000
0x2C	PCI Reserved				0x0000_0000
0x30	PCI Unimplemented				0x0000_0000
0x34	PCI Reserved				0x0000_0000
0x38	PCI Reserved				0x0000_0000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	0x0003_0100

(1) Read back value after writing all 1's.

Table 5-1 : Universe-II PCI Header

5.2 Universe-II Power-Up Options

The TVME8400 uses the default Universe-II power-up option configuration.

Please see the Universe-II user manual for details.

5.3 Universe-II Reset Signals

The Universe-II PWRRST# input is controlled by the board power-up reset logic.

The Universe-II RST# input is connected to the PCI reset signal.

If the TVME8400 Universe-II is the VME bus System Controller, a board reset will also trigger the Universe-II VMERST# input, asserting a VME bus System Reset.

If the TVME8400 Universe-II is not the VME bus System Controller, a VME bus System Reset will also trigger a TVME8400 board reset (using the Universe-II LRST# output).

The Universe-II VRSYSRST# and VXSYSRST# signals are mapped to the VME bus SYSRST# signal.

Please see the Universe-II user manual for details.

5.4 Universe-II Interrupts

The Universe-II LINT#[0:3] interrupt pins are bidirectional and can be used as inputs or open drain outputs.

By default (after power-up or board reset) the Universe-II LINT#[0:3] pins are used as outputs routed to the MPC8245 PIC serial interrupt channels 5:8.

The TVME8400 Control Register (0xFFE40000) provides an option for routing the PMC and Expansion Slot PCI interrupts to both the MPC8245 Interrupt Controller and the Universe-II LINT#[0:3] pins. This option may be used to map TVME8400 PMC and PCI Expansion Slot interrupts to the VME bus.

See the Interrupt Routing chapter in this manual for more details.

The Universe-II LINT#[4:7] interrupt pins are not used.

5.5 Universe-II VME Bus Modes

The Universe-II supports VME bus A32/24/16 master and slave address modes and D32/16/8 master and slave data transfer modes.

Please see the Universe-II user manual for details.

6 Ethernet Interface

The Intel 82551 Fast Ethernet Controller is used for the TVME8400 Ethernet interface.

The 82551 is accessible on the TVME8400 PCI bus (device number 14).

The 82551 INT# interrupt output is mapped to serial channel no. 2 of the MPC8245 PIC.

The 82551 is reset by a PCI reset.

Please refer to the 82551 manual for a detailed description of the 82551 Fast Ethernet Controller.

6.1 82551 PCI Header

Offset	PCI Configuration Register				Setting
	31 - 24	23 - 16	15 - 08	07 - 00	
0x00	Device ID		Vendor ID		0x1209_8086
0x04	Status		Command		0x0290_0007
0x08	Class Code			Revision ID	0x0200_00xx
0x0C	BIST	Header	Latency	Cache Line	0x0000_xx00
0x10	PCI Base Address 0 (Memory Mapped Configuration Register)				0xFFFF_F000(1) (4 Kbyte)
0x14	PCI Base Address 0 (I/O Mapped Configuration Register)				0xFFFF_FF81(1) (64 Byte)
0x18	PCI Base Address 0 (Memory Mapped Flash Space)				0xFFFE_0000(1) (128 Kbyte)
0x1C	Reserved				0x0000_0000
0x20	Reserved				0x0000_0000
0x24	Reserved				0x0000_0000
0x28	Reserved				0x0000_0000
0x2C	Subsystem ID		Subsystem Vendor ID		0x1209_8086
0x30	Expansion ROM PCI Base Address				0x0000_0000
0x34	Reserved			Cap. Pointer	0x0000_00DC
0x38	Reserved				0x0000_0000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	0xxx08_0100
0xDC	Power Management Cap.		Next Cap.	Cap. ID	0x7E22_0001
0xE0	Reserved	Data	Power Management CSR		0x4B00_4000

(1) Read back Value after writing all 1's.

Table 6-1 : 82551 PCI Header

6.2 82551 Configuration EEPROM

EEPROM Address (16 bit Address)	Description	
	Bits 15 - 8	**Bits 07 - 00**
0x00	Ethernet Address Byte 1	Ethernet Address Byte 0
	0x01	0x00
0x01	Ethernet Address Byte 3	Ethernet Address Byte 2
	xx	0x06
0x02	Ethernet Address Byte 5	Ethernet Address Byte 4
	zz	*yy*
0x0A	EEPROM ID	
	0x4840	
0x0B	Subsystem ID	
	0x1209	
0x0C	Subsystem Vendor ID	
	0x8086	
0x0D	Reserved	
	Tbd.	
0x0E	Reserved	
	Tbd.	
0x0F	Reserved	
	Tbd.	
0x10 - 0x3E	Reserved	
	0x0000	
0x3F	EEPROM Checksum	
	variant	

Table 6-2 : 82551 Configuration EEPROM Settings

6.3 Media Capabilities

IEEE 802.3 10Base-T / 100Base-TX interface (available at a RJ45 front panel connector).

The TVME8400 Ethernet Interface requires that the on board Real-Time-Clock is running.

The TVME8400 boards are shipped with the Real-Time-Clock turned off.

7 PCI Bus Overview

PCI Device	Device Number	Device ID	Vendor ID	Subsys ID	Subsys Vendor ID	PCI Arbiter Line (MPC8245)	Required Memory Space (Byte)	Required I/O Space (Byte)
MPC8245 Integrated Host PPC	-	0x0006	0x1057	0x0000	0x0000	-	-	-
Universe-II VME / PCI Bridge	13	0x0000	0x10E3	-	-	0	4K + Appl. dep. PCI Target Images	4K
82551 Fast Ethernet Controller	14	0x1209	0x8086	0x0000	0x0000	1	4K	64
PMC Slot 1	16	Depends on PMC	Depends on PMC	Depends on PMC	Depends on PMC	2	Depends on PMC	Depends on PMC
PMC Slot 2	17	Depends on PMC	Depends on PMC	Depends on PMC	Depends on PMC	3	Depends on PMC	Depends on PMC
PCI Expansion Connector	Depends on PCI Exp. Card	Depends on PCI Exp. Card	Depends on PCI Exp. Card	Depends on PCI Exp. Card	Depends on PCI Exp. Card	4	Depends on PCI Exp. Card	Depends on PCI Exp. Card

Table 7-1 : PCI Bus Overview

8 Interrupt Routing

8.1 TVME8400 Interrupt Sources

The TVM8400 provides the following (MPC8245 external) interrupt sources:

- Utility Interrupt Register
- ABORT Switch
- 82551 (Fast Ethernet Controller)
- Alarm / Watchdog (NVRAM / RTC Device)
- PMC / EXP Slot INT0 (Shared)
- PMC / EXP Slot INT1 (Shared)
- PMC / EXP Slot INT2 (Shared)
- PMC / EXP Slot INT3 (Shared)
- Universe-II LINT0 (VME / PCI Bridge)
- Universe-II LINT1 (VME / PCI Bridge)
- Universe-II LINT2 (VME / PCI Bridge)
- Universe-II LINT3 (VME / PCI Bridge)
- UART Channel 1
- UART Channel 2

8.2 MPC8245 PIC Serial Interrupt Channel Assignment

The TVME8400 forwards all (MPC8245 external) interrupt sources to the MPC8245 Programmable Interrupt Controller (PIC).

The MPC8245 PIC is used in serial mode, so each interrupt source is mapped to a dedicated serial channel of the MOC8245 PIC.

PIC Serial Interrupt No.	Edge / Level Sensitive	Active Polarity	Interrupt Source
0	Level	Low	Utility Interrupt Register (User)
1	Edge	Low	ABORT Switch (User)
2	Level	Low	82551 (Ethernet)
3	Level	-	Not used
4	Level	-	Not used
5	Level	Low	Universe-II LINT0 Line (VME)
6	Level	Low	Universe-II LINT1 Line (VME)
7	Level	Low	Universe-II LINT2 Line (VME)
8	Level	Low	Universe-II LINT3 Line (VME)
9	Level	Low	Shared PMC/EXP Slot INT0 Line (PMC Slot 1 INTA#, PMC Slot 2 INTB#, PCI EXP Slot INTA#)
10	Level	Low	Shared PMC/EXP Slot INT1 Line (PMC Slot 1 INTB#, PMC Slot 2 INTC#, PCI EXP Slot INTB#)
11	Level	Low	Shared PMC/EXP Slot INT2 Line

			(PMC Slot 1 INTC#, PMC Slot 2 INTD#, PCI EXP Slot INTC#)
12	Level	Low	Shared PMC/EXP Slot INT3 Line (PMC Slot 1 INTD#, PMC Slot 2 INTA#, PCI EXP Slot INTD#)
13	Level	Low	Alarm / Watchdog (NVRAM)
14	Level	Low	UART Channel 1 (Serial 1)
15	Level	Low	UART Channel 2 (Serial 2)

Table 8-1 : MPC8245 PIC Serial Interrupt Channel Assignment

8.3 Universe-II Interrupt Mapping Features

The Universe-II VME/PCI bridge provides additional programming options related to the TVME8400 interrupt features.

The Universe-II LINT pins are bidirectional.

By programming the Universe-II configuration registers an active interrupt level on an LINT line may be mapped to the VME bus. In this case the LINT pin is used as an input.

By programming the Universe-II configuration registers a VME bus interrupt may also be mapped to an LINT line. In this case the LINT pin is used as an (open-drain) output.

8.4 Extended PMC/EXP Slot Interrupt Routing

By default (as a Single Board Computer) the TVME8400 supports using the Universe-II LINT#[0:3] pins as outputs. By programming the Universe-II configuration registers, VME bus interrupts (or a SW interrupt asserted by an external VME bus master) may be mapped to the TVME8400 MPC8245 PIC.

The TVME8400 also provides a programmable option for forwarding all the PMC / EXP Slot PCI interrupts to the Universe-II LINT#[0:3] pins. By programming the Universe-II configuration registers, TVME8400 PMC / EXP Slot interrupts may be mapped to the VME bus. In this case (on the VME bus) the TVME8400 would act as a VME bus Interrupter. This option is intended for using the TVME8400 as a passive PMC carrier and is controlled by the PMC_INT_MAP bit in the TVME8400 Control Register (0xFFE40000).

<table>
<tr><th>Control Register (0xFFE40000)
PMC_INT_MAP Bit</th><th>Description</th></tr>
<tr><td rowspan="10">0
(default)</td><td colspan="2">Default TVME8400 PMC and Expansion Slot Interrupt Line Routing.
PMC and PCI Expansion Slot Interrupts are forwarded to the MPC8245 Interrupt Controller and not to the Universe-II LINT lines. The Universe-II LINT# pins are used as outputs only.</td></tr>
<tr><td>Interrupt Source</td><td>Interrupt Destination</td></tr>
<tr><td>Universe-II LINT0#</td><td>MPC8245 Serial Interrupt No. 5</td></tr>
<tr><td>Universe-II LINT1#</td><td>MPC8245 Serial Interrupt No. 6</td></tr>
<tr><td>Universe-II LINT2#</td><td>MPC8245 Serial Interrupt No. 7</td></tr>
<tr><td>Universe-II LINT3#</td><td>MPC8245 Serial Interrupt No. 8</td></tr>
<tr><td>PMC Slot 1 INTA#, PMC Slot 2 INTB#,
PCI Expansion Slot INTA#</td><td>MPC8245 PIC Serial Int. no. 9</td></tr>
<tr><td>PMC Slot 1 INTB#, PMC Slot 2 INTC#,
PCI Expansion Slot INTB#</td><td>MPC8245 PIC Serial Int. no. 10</td></tr>
<tr><td>PMC Slot 1 INTC#, PMC Slot 2 INTD#,
PCI Expansion Slot INTC#</td><td>MPC8245 PIC Serial Int. no. 11</td></tr>
<tr><td>PMC Slot 1 INTD#, PMC Slot 2 INTA#,
PCI Expansion Slot INTD#</td><td>MPC8245 PIC Serial Int. no. 12</td></tr>
<tr><td rowspan="10">1</td><td colspan="2">Extended TVME8400 PMC and Expansion Slot Interrupt Line Routing.
PMC and PCI Expansion Slot Interrupts are forwarded to both the MPC8245 Interrupt Controller and to the Universe-II LINT lines. A Universe-II LINT# pin may be used as an input (for mapping TVME8400 PMC/EXP slot interrupts to the VME bus) if there are any actual PMC/EXP slot interrupts mapped to it. A Universe-II LINT# pin may still be used as an output (for mapping VME bus interrupts to the TVME8400 MPC8245 PIC/CPU) if there are no actual PMC/EXP slot interrupts mapped to it.</td></tr>
<tr><td>Interrupt Source</td><td>Interrupt Destination</td></tr>
<tr><td>Universe-II LINT0# Line</td><td>MPC8245 PIC Serial Int. no. 5</td></tr>
<tr><td>Universe-II LINT1# Line</td><td>MPC8245 PIC Serial Int. no. 6</td></tr>
<tr><td>Universe-II LINT2# Line</td><td>MPC8245 PIC Serial Int. no. 7</td></tr>
<tr><td>Universe-II LINT3# Line</td><td>MPC8245 PIC Serial Int. no. 8</td></tr>
<tr><td>PMC Slot 1 INTA#, PMC Slot 2 INTB#,
PCI Expansion Slot INTA#</td><td>MPC8245 PIC Serial Int. no. 9
& Universe-II LINT0# Line</td></tr>
<tr><td>PMC Slot 1 INTB#, PMC Slot 2 INTC#,
PCI Expansion Slot INTB#</td><td>MPC8245 PIC Serial Int. no. 10
& Universe-II LINT1# Line</td></tr>
<tr><td>PMC Slot 1 INTC#, PMC Slot 2 INTD#,
PCI Expansion Slot INTC#</td><td>MPC8245 PIC Serial Int. no. 11
& Universe-II LINT2# Line</td></tr>
<tr><td>PMC Slot 1 INTD#, PMC Slot 2 INTA#,
PCI Expansion Slot INTD#</td><td>MPC8245 PIC Serial Int. no. 12
& Universe-II LINT3# Line</td></tr>
</table>

Table 8-2 : TVME8400 PMC/EXP Slot Interrupt Routing

Example Scenario

Two PMC boards are installed in the TVME8400 PMC slots. Each of the PMC modules utilizes a single PCI interrupt line (INTA#). The TVME8400 PCI Expansion Slot is not used.

In this scenario (with PMC_INT_MAP bit = 1), the PMC 1 INTA# line is routed to both the MPC8245 PIC serial interrupt channel 9 and to the Universe-II LINT0 line. The PMC 2 INTA# line is routed to both the MPC8245 PIC serial interrupt channel 12 and to the Universe-II LINT3 line.

The Universe-II LINT0 and LINT3 lines are now reserved for mapping TVME8400 PMC / EXP slot interrupts to the VME bus and may not be used for mapping VME bus interrupts to the TVME8400 MPC8245 PIC. Both PMC interrupt lines may be mapped to the VME bus by programming the Universe-II configuration registers accordingly. The MPC8245 PIC serial interrupt channels 5, 8, 9, and 12 should not be enabled.

The Universe-II LINT1 and LINT2 lines are not driven by any TVME8400 PMC or EXP slot device and may be used for mapping VME bus interrupts to the MPC8245 PIC serial interrupt channels 6 and 7.

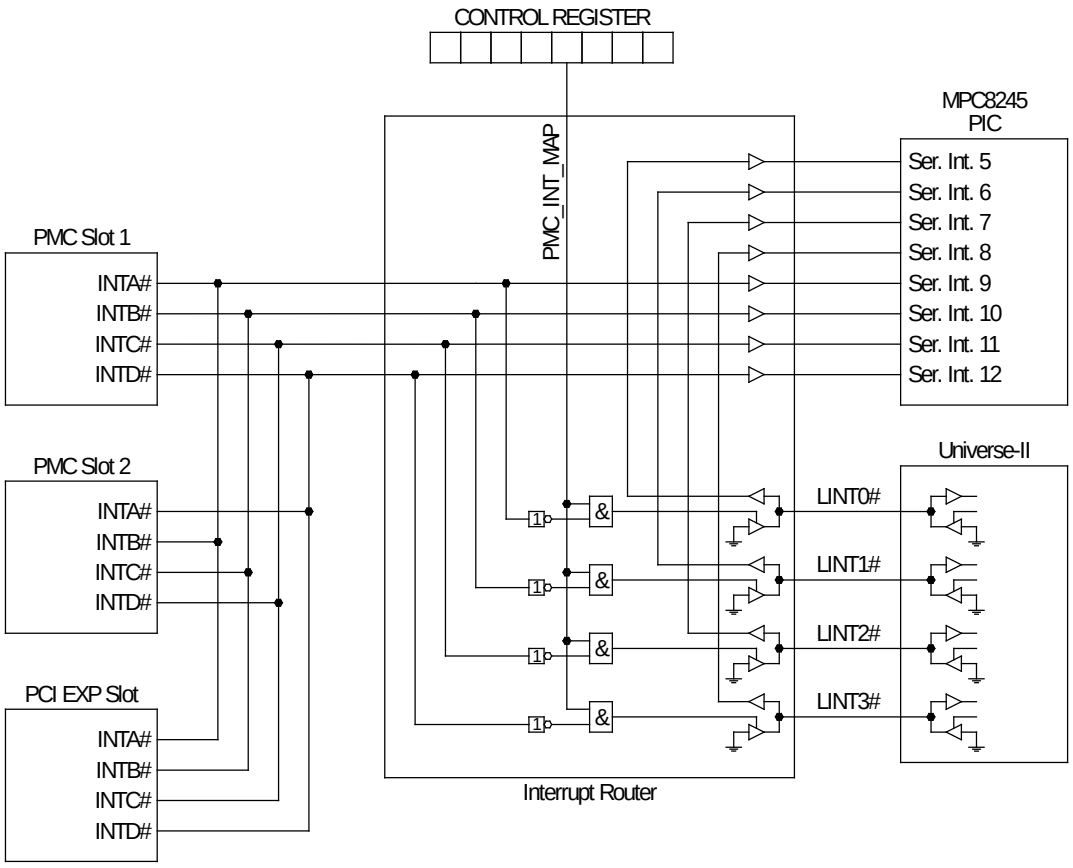

Figure 8-1 : TVME8400 PMC/EXP Slot Interrupt Routing Scheme

9 PMC Carrier Application

Besides using the TVME8400 as a Single Board Computer (SBC) with the option of adding PMC modules for I/O functionality, the TVME8400 could also be used as a PMC carrier on the VME bus.

9.1 TVME8400 as a passive PMC carrier

The TVME8400 could be used as a passive PMC carrier, e.g. for adding versatile I/O functionality to a VME bus system.

As a passive PMC carrier the TVME8400 would provide VME bus slave address space for external VME bus masters to access addressable regions of the installed PMC modules.

If the installed PMC modules provide interrupt capability, the interrupts from the TVME8400 PMC and PCI Expansion Slots could be mapped to the VME bus to be processed by external interrupt handlers on the VME bus.

Configuring the TVME8400 as a passive PMC carrier is mainly accomplished by programming the Universe-II VME/PCI bridge configuration registers accordingly. The TVME8400 bug monitor will provide commands for a user-friendly setup. Please refer to the TVME8400 PMON User Manual for more details.

9.2 TVME8400 as an active PMC carrier

The TVME8400 could also be used as an active (intelligent) PMC carrier, providing fast (local) access to the installed PMC modules while still providing useful information for external VME bus masters or slaves.

A typical scenario would be the need for additional I/O functionality, but communication between a CPU located on the VME bus and the PMC I/O modules located on a passive VME bus PMC carrier would lack performance (VME bus bottle-neck).

In this setup the TVME8400 PMC interrupts are usually mapped to the MPC8245 Interrupt Controller and not to the VME bus, so the TVME8400 PMC interrupts are handled by the MPC8245 CPU (not by an Interrupt Handler on the VME bus). However, the software running on the TVME8400 may still assert interrupt requests on the VME bus.

Communication with the VME bus is application specific. I/O data/messages could be buffered in the TVME8400 RAM area. The TVME8400 could act as a VME bus master, assert interrupts on the VME bus, provide a VME bus slave space for external VME bus masters, etc.

Please contact TEWS Technologies for a customized solution.

10 Installation and Use Notes

10.1 PMON Bug Monitor

The TVME8400 comes with a built-in bug monitor program (PMON) supporting various commands via a command line interface.

For using the PMON, the TVME8400 serial port 1 (RS232) must be properly connected to a remote RS232 serial port providing a terminal software (e.g. a common PC COM port) and the startup jumper J1 must be set to position 2-3 (marked “MON”).

These are the factory default settings for TVME8400 serial port 1:

Baudrate:	9600
Datawidth:	8 bit
Parity-Bit:	None
Stop-Bits:	1
Flow-Control:	None

After power-up or board reset, the on board CPU will start fetching and executing the general board initialization code from the on board Boot-Flash.

After general board initialization the setting of the startup jumper is checked. If the startup jumper is set to the 2-3 position (marked as “MON”), the TVME8400 bug monitor program (PMON) is started and comes up with some general information and the PMON prompt.

```
fxp0: interrupts polled, address 00:01:06:00:01:de
inphy0 at fxp0 phy 1: i82555 10/100 media interface, rev. 4
universe: system controller, sysfail is asserted

* PMON 2000 Professional *
Version: 1.1.1. Build date: May 26 2009 15:28:22
This software may be redistributed under the BSD copyright.
TVME8400 BSP Copyright 2004-2009, TEWS TECHNOLOGIES GmbH
CPU PowerPC MPC8245/603e @  300 MHz/100 MHz.
Memory size  64 MB.

PMON>
```

Usually, when the board is used for the first time, the initial step would be to enable the Real-Time Clock functions with the *date* command.

Please see the TVME8400 PMON User Manual for more details about the PMON commands and features.

10.2 NVRAM Real-Time Clock Control

The TVME8400 provides a M48T59 NVRAM / RTC device with a snaphat battery plugged on top. The snaphat battery provides power for the SRAM cells when the main power supply is off.

The TVME8400 is shipped with the snaphat battery installed on top of the M48T59 NVRAM device. The Real-Time Clock function of the M48T59 device is turned-off by default, to save battery energy.

If the M48T59 Real-Time Clock function has been turned-off (factory default), it must be enabled again, before using any other board resources (e.g. the Ethernet interface).

The PMON "date" command can be used to enable the Real-Time Clock function.

Setup / Start the Real-Time Clock operation:

```
PMON> date 200408101445.00
Tue Aug 10 14:45:00 2004
PMON> reboot
```

Stop the Real-Time Clock operation:

(This is recommended for TVME8400 board storage)

```
PMON> date -x
Clock is stopped...
PMON>
```

11 Board I/O

11.1 Board I/O Overview

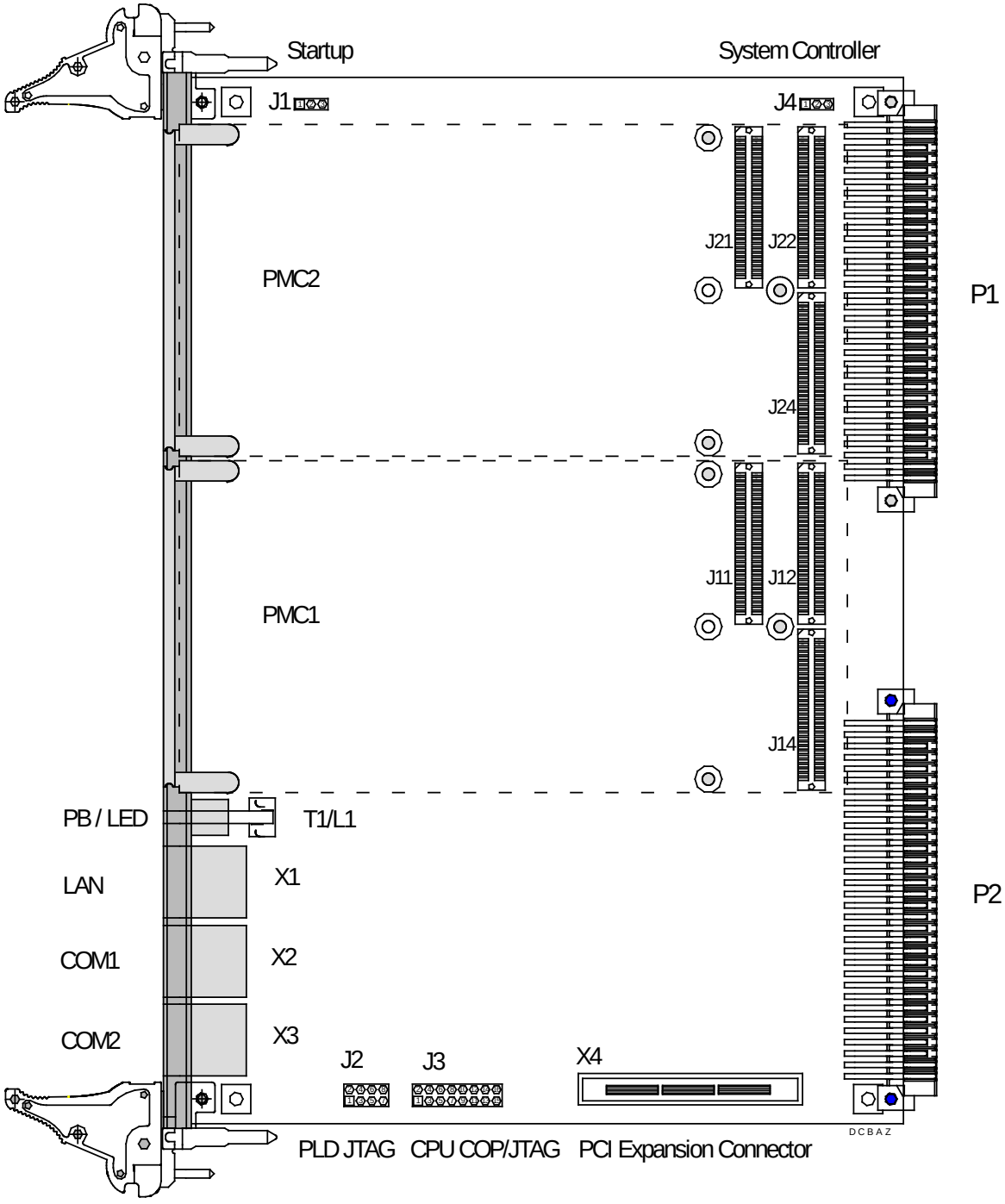

Figure 11-1: Board I/O Overview

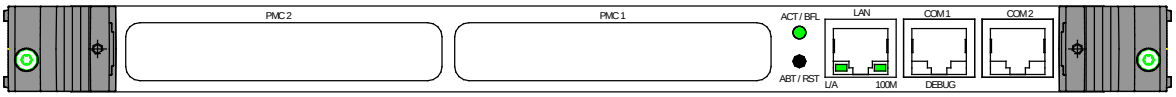

Figure 11-2 : Front Panel View

11.2 Jumper

11.2.1 Startup Jumper

The startup jumper status can be read in the Utility Status Register.

After basic board initialization, the (factory default) board initialization software checks the startup jumper status to decide if program execution continues from the Boot Flash (bug monitor), or from the Application Flash (user application). If used, the first instruction in the Application Flash must reside at address 0x7000_0100 (offset 0x100).

STARTUP JUMPER	
Jumper 1-2 Installed	Run from Application Flash after board initialization (User Application)
Jumper 2-3 Installed	Run from Boot Flash after board initialization (Bug Monitor)
No Jumper Installed	Run from Application Flash after board initialization (User Application)

Table 11-1: Boot Jumper

The startup jumper function is reserved by the (factory default) boot initialization software.

The 8 bit wide socket Boot Flash must always be installed (XU1 socket) and provide the board initialization code at the system reset vector (0xFFF0_0100).

The factory default bug monitor uses COM port 1.

If used with the (factory default) board initialization software, the first instruction in the Application Flash must reside at address 0x7000_0100 (offset 0x100).

11.2.2 VME System Controller Jumper

The VME system controller jumper is used to configure the VME system controller mode of the TVME8400 Universe-II VME to PCI bridge.

VME SYSTEM CONTROLLER JUMPER	
Jumper 1-2 Installed	Not VME System Controller
Jumper 2-3 Installed	VME System Controller Auto Configuration
No Jumper Installed	VME System Controller

Table 11-2: VME System Controller Jumper

The VME system controller jumper controls the Universe-II BGIN3# input signal, which the Universe-II samples at power-up to determine the VME system controller mode.

If the TVME8400 is the VME system controller, a board reset will also generate a VME system reset. If the TVME8400 is not the VME system controller, a VME system reset will also generate a TVME8400 board reset.

11.3 DIP Switch

The TVME8400 provides an 8 position user DIP Switch.

The status of the user DIP Switch can be read in the Utility DIP Switch Register.

Please see the DIP Switch Register description in the Address Maps section for more details.

11.4 LEDs

The TVME8400 provides a bi-color (green/red) LED at the front panel.

Green LED	Red LED	Indication
Off	Off	No failure indication, No board activity
Off	On	Failure indication (Utility LED Register bit) (set by user)
On	Off	Board activity (Local Memory Bus, PCI Bus) (set by board hardware)
Both On (Orange)		Board reset phase

Table 11-3: LED Indication

The TVME8400 RJ45 LAN connector provides two LEDs for Speed and Link/Activity indication.

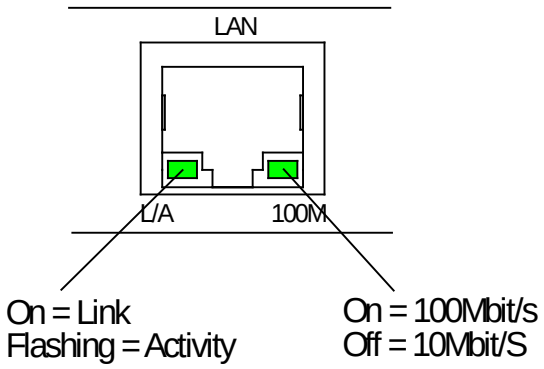

Figure 11-3: LAN LEDs on RJ45 Connector

11.5 Push button Switch

The TVME8400 provides a single two-function push button switch at the front panel.

The two push button functions are Abort or Board Reset.

If the push button switch is held active for less than (appr.) 3.2 sec, this will generate an Abort interrupt to the MPC8245 CPU. The Abort interrupt is mapped to serial interrupt channel 1 of the MPC8245 PIC. Serial interrupt channel 1 must be configured as edge sensitive.

If the push button switch is held active for more than (appr.) 3.2 sec, this will generate a board reset.

A board reset is also performed at power-up.

A board reset can also be asserted by software, programming the Utility Control Register.

A board reset will perform a general board hardware reset, PCI reset and CPU reset. If the TVME8400 is the VME system controller, a board reset will also generate a VME system reset.

11.6 Connectors

11.6.1 VME Interface Connectors

11.6.1.1 VME P1 Connector

Pin	Row Z	Row A	Row B	Row C	Row D
1	-	VME_D0	VME_BBSY#	VME_D8	+5V
2	GND	VME_D1	VME_BCLR#	VME_D9	GND
3	-	VME_D2	VME_ACFAIL#	VME_D10	-
4	GND	VME_D3	VME_BGIN0#	VME_D11	-
5	-	VME_D4	VME_BGOUT0#	VME_D12	-
6	GND	VME_D5	VME_BGIN1#	VME_D13	-
7	-	VME_D6	VME_BGOUT1#	VME_D14	-
8	GND	VME_D7	VME_BGIN2#	VME_D15	-
9	-	GND	VME_BGOUT2#	GND	-
10	GND	VME_SYSCLK	VME_BGIN3#	VME_SYSFAIL#	-
11	-	GND	VME_BGOUT3#	VME_BERR#	-
12	GND	VME_DS1#	VME_BR0#	VME_SYSRST#	-
13	-	VME_DS0#	VME_BR1#	VME_LWORD#	-
14	GND	VME_WRITE#	VME_BR2#	VME_AM5	-
15	-	GND	VME_BR3#	VME_A23	-
16	GND	VME_DTACK#	VME_AM0	VME_A22	-
17	-	GND	VME_AM1	VME_A21	-
18	GND	VME_AS#	VME_AM2	VME_A20	-
19	-	GND	VME_AM3	VME_A19	-
20	GND	VME_IACK#	GND	VME_A18	-
21	-	VME_IACKIN#	-	VME_A17	-
22	GND	VME_IACKOUT#	-	VME_A16	-
23	-	VME_AM4	GND	VME_A15	-
24	GND	VME_A7	VME_IRQ7#	VME_A14	-
25	-	VME_A6	VME_IRQ6#	VME_A13	-
26	GND	VME_A5	VME_IRQ5#	VME_A12	-
27	-	VME_A4	VME_IRQ4#	VME_A11	-
28	GND	VME_A3	VME_IRQ3#	VME_A10	-
29	-	VME_A2	VME_IRQ2#	VME_A9	-
30	GND	VME_A1	VME_IRQ1#	VME_A8	-
31	-	-12V	-	+12V	GND
32	GND	+5V	+5V	+5V	+5V

Table 11-4: VME P1 Connector

11.6.1.2 VME P2 Connector

Pin	Row Z	Row A	Row B	Row C	Row D
1	PMC2_IO02	PMC1_IO02	+5V	PMC1_IO01	PMC2_IO01
2	GND	PMC1_IO04	GND	PMC1_IO03	PMC2_IO03
3	PMC2_IO05	PMC1_IO06	-	PMC1_IO05	PMC2_IO04
4	GND	PMC1_IO08	VME_A24	PMC1_IO07	PMC2_IO06
5	PMC2_IO08	PMC1_IO10	VME_A25	PMC1_IO09	PMC2_IO07
6	GND	PMC1_IO12	VME_A26	PMC1_IO11	PMC2_IO09
7	PMC2_IO11	PMC1_IO14	VME_A27	PMC1_IO13	PMC2_IO10
8	GND	PMC1_IO16	VME_A28	PMC1_IO15	PMC2_IO12
9	PMC2_IO14	PMC1_IO18	VME_A29	PMC1_IO17	PMC2_IO13
10	GND	PMC1_IO20	VME_A30	PMC1_IO19	PMC2_IO15
11	PMC2_IO17	PMC1_IO22	VME_A31	PMC1_IO21	PMC2_IO16
12	GND	PMC1_IO24	GND	PMC1_IO23	PMC2_IO18
13	PMC2_IO20	PMC1_IO26	+5V	PMC1_IO25	PMC2_IO19
14	GND	PMC1_IO28	VME_D16	PMC1_IO27	PMC2_IO21
15	PMC2_IO23	PMC1_IO30	VME_D17	PMC1_IO29	PMC2_IO22
16	GND	PMC1_IO32	VME_D18	PMC1_IO31	PMC2_IO24
17	PMC2_IO26	PMC1_IO34	VME_D19	PMC1_IO33	PMC2_IO25
18	GND	PMC1_IO36	VME_D20	PMC1_IO35	PMC2_IO27
19	PMC2_IO29	PMC1_IO38	VME_D21	PMC1_IO37	PMC2_IO28
20	GND	PMC1_IO40	VME_D22	PMC1_IO39	PMC2_IO30
21	PMC2_IO32	PMC1_IO42	VME_D23	PMC1_IO41	PMC2_IO31
22	GND	PMC1_IO44	GND	PMC1_IO43	PMC2_IO33
23	PMC2_IO35	PMC1_IO46	VME_D24	PMC1_IO45	PMC2_IO34
24	GND	PMC1_IO48	VME_D25	PMC1_IO47	PMC2_IO36
25	PMC2_IO38	PMC1_IO50	VME_D26	PMC1_IO49	PMC2_IO37
26	GND	PMC1_IO52	VME_D27	PMC1_IO51	PMC2_IO39
27	PMC2_IO41	PMC1_IO54	VME_D28	PMC1_IO53	PMC2_IO40
28	GND	PMC1_IO56	VME_D29	PMC1_IO55	PMC2_IO42
29	PMC2_IO44	PMC1_IO58	VME_D30	PMC1_IO57	PMC2_IO43
30	GND	PMC1_IO60	VME_D31	PMC1_IO59	PMC2_IO45
31	PMC2_IO46	PMC1_IO62	GND	PMC1_IO61	GND
32	GND	PMC1_IO64	+5V	PMC1_IO63	+5V

Table 11-5: VME P2 Connector

11.6.1.3 VME P0 Connector

	A	B	C	D	E	F
1	NC	NC	NC	NC	NC	GND
2	NC	NC	NC	NC	NC	GND
3	NC	NC	NC	NC	NC	GND
4	NC	NC	NC	NC	NC	GND
5	NC	NC	NC	NC	NC	GND
6	NC	NC	NC	NC	NC	GND
7	NC	NC	NC	NC	NC	GND
8	NC	NC	NC	NC	NC	GND
9	NC	NC	NC	NC	NC	GND
10	NC	NC	NC	NC	NC	GND
11	NC	NC	NC	NC	NC	GND
12	NC	NC	NC	NC	NC	GND
13	NC	NC	NC	NC	NC	GND
14	NC	NC	NC	NC	NC	GND
15	NC	NC	NC	NC	NC	GND
16	PMC2_IO50	PMC2_IO49	PMC2_IO48	PMC2_IO47	NC	GND
17	PMC2_IO55	PMC2_IO54	PMC2_IO53	PMC2_IO52	PMC2_IO51	GND
18	PMC2_IO60	PMC2_IO59	PMC2_IO58	PMC2_IO57	PMC2_IO56	GND
19	NC	PMC2_IO64	PMC2_IO63	PMC2_IO62	PMC2_IO61	GND

Table 11-6: VME P0 Connector

The VME P0 connector is only available for TVME8400-x1 board options.

11.6.2 PMC Interface Connectors

11.6.2.1 PMC 1 - J11 Connector (PCI, +5V)

Pin	Signal		Signal	Pin
1	TCK		-12V	2
3	GND		INT_A#	4
5	INT_B#		INT_C#	6
7	PMC1_PRSNT#		+5V	8
9	INT_D#		-	10
11	GND		-	12
13	CLK		GND	14
15	GND		PMC1_GNT#	16
17	PMC1_REQ#		+5V	18
19	+5V (VIO)		AD31	20
21	AD28		AD27	22
23	AD25		GND	24
25	GND		C/BE3#	26
27	AD22		AD21	28
29	AD19		+5V	30
31	+5V (VIO)		AD17	32
33	FRAME#		GND	34
35	GND		IRDY#	36
37	DEVSEL#		+5V	38
39	GND		LOCK#	40
41	Pull-up (+3.3V)		Pull-up (+3.3V)	42
43	PAR		GND	44
45	+5V (VIO)		AD15	46
47	AD12		AD11	48
49	AD09		+5V	50
51	GND		C/BE0#	52
53	AD06		AD05	54
55	AD04		GND	56
57	+5V (VIO)		AD03	58
59	AD02		AD01	60
61	AD00		+5V	62
63	GND		Pull-up (+3.3V)	64

Table 11-7: PMC 1 - J11 Connector

11.6.2.2 PMC 1 - J12 Connector (PCI, +3.3V)

Pin	Signal		Signal	Pin
1	+12V		TRST#	2
3	TMS		TDO	4
5	TDI		GND	6
7	GND		-	8
9	-		-	10
11	Pull-up (+3.3V)		+3.3V	12
13	RST#		Pull-down (GND)	14
15	+3.3V		Pull-down (GND)	16
17	-		GND	18
19	AD30		AD29	20
21	GND		AD26	22
23	AD24		+3.3V	24
25	PMC1_IDSEL		AD23	26
27	+3.3V		AD20	28
29	AD18		GND	30
31	AD16		C/BE2#	32
33	GND		-	34
35	TRDY#		+3.3V	36
37	GND		STOP#	38
39	PERR#		GND	40
41	+3.3V		SERR#	42
43	C/BE1#		GND	44
45	AD14		AD13	46
47	GND		AD10	48
49	AD08		+3.3V	50
51	AD07		-	52
53	+3.3V		-	54
55	-		GND	56
57	-		-	58
59	GND		-	60
61	Pull-up (+3.3V)		+3.3V	62
63	GND		-	64

Table 11-8: PMC 1 - J12 Connector

11.6.2.3 PMC 1 - J14 Connector (I/O)

Pin	Signal		Signal	Pin
1	PMC1_IO01		PMC1_IO02	2
3	PMC1_IO03		PMC1_IO04	4
5	PMC1_IO05		PMC1_IO06	6
7	PMC1_IO07		PMC1_IO08	8
9	PMC1_IO09		PMC1_IO10	10
11	PMC1_IO11		PMC1_IO12	12
13	PMC1_IO13		PMC1_IO14	14
15	PMC1_IO15		PMC1_IO16	16
17	PMC1_IO17		PMC1_IO18	18
19	PMC1_IO19		PMC1_IO20	20
21	PMC1_IO21		PMC1_IO22	22
23	PMC1_IO23		PMC1_IO24	24
25	PMC1_IO25		PMC1_IO26	26
27	PMC1_IO27		PMC1_IO28	28
29	PMC1_IO29		PMC1_IO30	30
31	PMC1_IO31		PMC1_IO32	32
33	PMC1_IO33		PMC1_IO34	34
35	PMC1_IO35		PMC1_IO36	36
37	PMC1_IO37		PMC1_IO38	38
39	PMC1_IO39		PMC1_IO40	40
41	PMC1_IO41		PMC1_IO42	42
43	PMC1_IO43		PMC1_IO44	44
45	PMC1_IO45		PMC1_IO46	46
47	PMC1_IO47		PMC1_IO48	48
49	PMC1_IO49		PMC1_IO50	50
51	PMC1_IO51		PMC1_IO52	52
53	PMC1_IO53		PMC1_IO54	54
55	PMC1_IO55		PMC1_IO56	56
57	PMC1_IO57		PMC1_IO58	58
59	PMC1_IO59		PMC1_IO60	60
61	PMC1_IO61		PMC1_IO62	62
63	PMC1_IO63		PMC1_IO64	64

Table 11-9: PMC 1 - J14 Connector

11.6.2.4 PMC 2 - J21 Connector (PCI, +5V)

Pin	Signal		Signal	Pin
1	TCK		-12V	2
3	GND		INT_D#	4
5	INT_A#		INT_B#	6
7	PMC2_PRSNT#		+5V	8
9	INT_C#		-	10
11	GND		-	12
13	CLK		GND	14
15	GND		PMC2_GNT#	16
17	PMC2_REQ#		+5V	18
19	+5V (VIO)		AD31	20
21	AD28		AD27	22
23	AD25		GND	24
25	GND		C/BE3#	26
27	AD22		AD21	28
29	AD19		+5V	30
31	+5V (VIO)		AD17	32
33	FRAME#		GND	34
35	GND		IRDY#	36
37	DEVSEL#		+5V	38
39	GND		LOCK#	40
41	Pull-up (+3.3V)		Pull-up (+3.3V)	42
43	PAR		GND	44
45	+5V (VIO)		AD15	46
47	AD12		AD11	48
49	AD09		+5V	50
51	GND		C/BE0#	52
53	AD06		AD05	54
55	AD04		GND	56
57	+5V (VIO)		AD03	58
59	AD02		AD01	60
61	AD00		+5V	62
63	GND		Pull-up (+3.3V)	64

Table 11-10: PMC 2 - J21 Connector

11.6.2.5 PMC 2 - J22 Connector (PCI, +3.3V)

Pin	Signal		Signal	Pin
1	+12V		TRST#	2
3	TMS		TDO	4
5	TDI		GND	6
7	GND		-	8
9	-		-	10
11	Pull-up (+3.3V)		+3.3V	12
13	RST#		Pull-down (GND)	14
15	+3.3V		Pull-down (GND)	16
17	-		GND	18
19	AD30		AD29	20
21	GND		AD26	22
23	AD24		+3.3V	24
25	PMC2_IDSEL		AD23	26
27	+3.3V		AD20	28
29	AD18		GND	30
31	AD16		C/BE2#	32
33	GND		-	34
35	TRDY#		+3.3V	36
37	GND		STOP#	38
39	PERR#		GND	40
41	+3.3V		SERR#	42
43	C/BE1#		GND	44
45	AD14		AD13	46
47	GND		AD10	48
49	AD08		+3.3V	50
51	AD07		-	52
53	+3.3V		-	54
55	-		GND	56
57	-		-	58
59	GND		-	60
61	Pull-up (+3.3V)		+3.3V	62
63	GND		-	64

Table 11-11: PMC 2 - J22 Connector

11.6.2.6 PMC 2 - J24 Connector (I/O)

Pin	Signal		Signal	Pin
1	PMC2_IO01		PMC2_IO02	2
3	PMC2_IO03		PMC2_IO04	4
5	PMC2_IO05		PMC2_IO06	6
7	PMC2_IO07		PMC2_IO08	8
9	PMC2_IO09		PMC2_IO10	10
11	PMC2_IO11		PMC2_IO12	12
13	PMC2_IO13		PMC2_IO14	14
15	PMC2_IO15		PMC2_IO16	16
17	PMC2_IO17		PMC2_IO18	18
19	PMC2_IO19		PMC2_IO20	20
21	PMC2_IO21		PMC2_IO22	22
23	PMC2_IO23		PMC2_IO24	24
25	PMC2_IO25		PMC2_IO26	26
27	PMC2_IO27		PMC2_IO28	28
29	PMC2_IO29		PMC2_IO30	30
31	PMC2_IO31		PMC2_IO32	32
33	PMC2_IO33		PMC2_IO34	34
35	PMC2_IO35		PMC2_IO36	36
37	PMC2_IO37		PMC2_IO38	38
39	PMC2_IO39		PMC2_IO40	40
41	PMC2_IO41		PMC2_IO42	42
43	PMC2_IO43		PMC2_IO44	44
45	PMC2_IO45		PMC2_IO46	46
47	PMC2_IO47		PMC2_IO48	48
49	PMC2_IO49		PMC2_IO50	50
51	PMC2_IO51		PMC2_IO52	52
53	PMC2_IO53		PMC2_IO54	54
55	PMC2_IO55		PMC2_IO56	56
57	PMC2_IO57		PMC2_IO58	58
59	PMC2_IO59		PMC2_IO60	60
61	PMC2_IO61		PMC2_IO62	62
63	PMC2_IO63		PMC2_IO64	64

Table 11-12: PMC 2 - J24 Connector

11.6.3 PCI Expansion Connector

Pin	Signal		Pin	Signal
1	+3.3V		2	+3.3V
3	CLK		4	INTA#
5	GND		6	INTB#
7	PWRRST#		8	INTC#
9	HRST#		10	INTD#
11	Pull-up (+3.3V)		12	Pull-up (+3.3V)
13	Pull-up (+3.3V)		14	Pull-down (GND)
15	Pull-down (GND)		16	PRSNT#
17	GNT#		18	REQ#
19	+12V	GND	20	-12V
21	PERR#		22	SERR#
23	LOCK#		24	Pull-up (+3.3V)
25	DEVSEL#		26	Pull-up (+3.3V)
27	GND		28	GND
29	TRDY#		30	IRDY#
31	STOP#		32	FRAME#
33	GND		34	GND
35	Pull-up (+3.3V)		36	-
37	Pull-up (+3.3V)		38	-
39	PAR		40	RST#
41	C/BE1#		42	C/BE0#
43	C/BE3#		44	C/BE2#
45	AD1		46	AD0
47	AD3		48	AD2
49	AD5		50	AD4
51	AD7		52	AD6
53	AD9		54	AD8
55	AD11		56	AD10
57	AD13	+5V	58	AD12
59	AD15		60	AD14
61	AD17		62	AD16
63	AD19		64	AD18
65	AD21		66	AD20
67	AD23		68	AD22
69	AD25		70	AD24
71	AD27		72	AD26
73	AD29		74	AD28
75	AD31		76	AD30
77	-		78	-
79	-		80	-
81	-		82	-
83	-		84	-
85	-	GND	86	-
87	-		88	-
89	-		90	-

Pin	Signal		Pin	Signal
91	-		92	-
93	-		94	-
95	-		96	-
97	-		98	-
99	-		100	-
101	-		102	-
103	-		104	-
105	-		106	-
107	-		108	-
109	-		110	-
111	-		112	-
113	-		114	-

Table 11-13: PCI Expansion Connector

The PCI Expansion Connector type used is AMP 2-767004-4 (or compatible).

11.6.4 Serial Interface Connectors

11.6.4.1 Serial Port 1

Pin	Signal	Level
1	DCD_1 (Input)	RS232
2	RTS_1 (Output)	RS232
3	C_GND	
4	TXD_1 (Output)	RS232
5	RXD_1 (Input)	RS232
6	C_GND	
7	CTS_1 (Input)	RS232
8	DTR_1 (Output)	RS232

Table 11-14: Serial Port 1 (RS232) (RJ45 Connector)

11.6.4.2 Serial Port 2

Pin	Signal	Level
1	DCD_2 (Input)	RS232
2	RTS_2 (Output)	RS232
3	C_GND	
4	TXD_2 (Output)	RS232
5	RXD_2 (Input)	RS232
6	C_GND	
7	CTS_2 (Input)	RS232
8	DTR_2 (Output)	RS232

Table 11-15: Serial Port 2 (RS232) (RJ45 Connector)

The serial port signals are shown in the TVME8400 pin function (e.g. the TXD output signal of the external device must be connected to pin 5 (RXD input) of the serial port connector, not to pin 4 (TXD output)).

The TVME8400 factory default bug monitor software (PMON) uses Serial Port 1.

The Serial Interface Connector type used is AMP 558250-1 (or compatible).

11.6.5 Ethernet Interface Connector

Pin	Signal
1	TD+
2	TD-
3	RD+
4	AC Termination
5	AC Termination
6	RD-
7	AC Termination
8	AC Termination

Table 11-16: Ethernet Connector (RJ45 Connector)

The Ethernet Interface Connector type used is HALO HFJ11-2450E-L11 (or compatible).

12 Technical Information

12.1 Processor

- Motorola MPC8245 Integrated Host PPC (300 MHz Core Frequency)
- Embedded Version MPC603e (G2) Processor Core
- Floating Point Unit
- DMA Controller
- 16 Kbyte I-Cache, 16 Kbyte D-Cache
- Four cascadable 31 bit timer

12.2 Memory

- TVME8400-10R/-11R : 64 Mbyte 64 bit wide SDRAM (100 MHz)
  TVME8400-20R/-21R : 256 Mbyte 64 bit wide SDRAM (100 MHz)
- 8 Mbyte 64 bit wide Flash Memory

12.3 Other Devices

- 8 Kbyte NVRAM (M48T59 or compatible) with exchangeable battery
- 1 Mbyte 8 bit wide Boot-Flash (2 PLCC sockets)

12.4 VME Interface

- Tundra Universe-II VME / PCI bridge
- A16-A32 Master/Slave Address Modes; D08-D64 Master/Slave Data Transfer Modes
- RR/PRI VME bus Arbiter
- IRQ 1-7 (any of seven IRQs)
- System Controller Jumper (Yes, No, Auto Detect)
- Four Location Monitors
- DMA Controller

12.5 Ethernet Interface

- Intel 82551 Controller
- PCI DMA support
- 10Base-T / 100Base-TX Interface
- RJ45 front panel connector, Link/Activity & Speed LED

12.6 Asynchronous Serial Interface

- Dual 16C550 compatible UART (1.8432 MHz clock source)
- Two RS232 ports (two RJ45 front panel connectors)
- Max baud rate 115 kbps

12.7 PCI Expansion Connector

- 32 bit 33 MHz PCI Interface (114-pin connector)
- 5V PCI Signaling Voltage (PCI Expansion Board may drive 3.3V or 5V PCI signal levels, PCI Expansion Board must tolerate 5V PCI signal levels)
- Supports Motorola's PMC-Span, TEWS' IP-Span (TVME230)

12.8 PMC Interface

- Two 32 bit 33 MHz PCI PMC Slots (two single wide or one double wide PMC)
- 5V PCI Signaling Voltage (PMCs may drive 3.3V or 5V PCI signal levels, PMCs must tolerate 5V PCI signal levels)
- Power : +3.3V, +5V, ±12V, max 7.5W total per PMC slot
- Front panel and/or VME P2/P0 I/O

VME P2 I/O	PMC slot 1 I/O lines 1-64, PMC slot 2 I/O lines 1-46
VME P0 I/O (TVME8400-x1 options only)	PMC slot 2 I/O lines 47-64

- Max 0.5A continuous dc current per PMC VME P2/P0 I/O line

12.9 Power Requirements

(Not including power required by PMC modules or PCI expansion board)

- +5V : max 3.5A (includes TVME8400 on board 3.3V power supply requirements)
- ±12V : not used (available on PMC slots and PCI expansion connector)

The 3.3V power supply for TVME8400 board devices and the PMC slots is generated on board the TVME8400 using the +5V power supply.

12.10 Physical Data

12.10.1 MTBF

TVME8400 Board Option	MTBF*
-10R / -2R0	241000 h
--11R / -21R	232000 h
-10R-ET / -20R-ET	204000 h
-11R-ET / -21R-ET	196000 h

Table 12-1: MTBF Data

*MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.

12.10.2 Temperature

TVME8400 Board Option	Temperature Range
Operating	
-10R / -11R/ -20R / -21R	0°C to 55°C (forced air cooling)
-xxR-ET	-40°C to +85°C (forced air cooling)
Non-Operating	
all	-40°C to +85°C

Table 12-2: Temperature Range

12.10.3 Weight

TVME8400 Board Option	Weight
-10R / -10R-ET / -20R / -20R-ET	330 g
-11R / -11R-ET / -21R / -21R-ET	380 g

Table 12-3: Weight

12.10.4 Humidity

- 5% to 90% (Non-Condensing)

12.10.5 Form Factor

- Standard one slot 6U VME
- 5-row (z, a, b, c, d) VME P1 & P2 connectors

(PCI expansion board occupies an additional VME slot if installed)