The Embedded I/O Company

TEWS TECHNOLOGIES

TXMC387

Conduction Cooled, 2x 100/1000/10000 Mbit/s Ethernet Adapter

Version 1.0

User Manual

Issue 1.0.0

July 2013

TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

TXMC387-10R

Conduction Cooled, Two channel 100/1000/10000 Mbit/s Ethernet interface back I/O, X12d mapping per VITA46.9, extended temperature range
(RoHS compliant)

TXMC387-20R

Conduction Cooled, Two channel 100/1000/10000 Mbit/s Ethernet interface back I/O, X8d mapping per VITA46.9, extended temperature range
(RoHS compliant)

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial issue	July 2013

Table of Contents

List of Figures

List of Tables

1 Product Description

The TXMC387 is a Conduction Cooled Switched Mezzanine Card (CCXMC) compatible module providing a two channel Ethernet 100BASE-TX / 1000BASE-T / 10GBASE-T interface.

The XMC-Connector P15 provides access to the Intel™ X540 dual port 10GbE controller via an x8 PCIe link. Both Ethernet interfaces support 100, 1000 Mbit/s and 10 Gbit/s transmission rates at full duplex operation. The controller is equipped with a 16 Mbit serial flash memory which is accessed by hardware at power-up, which has a firmware area and which can be accessed by software.

The two Ethernet interfaces of the TXMC387 are capable of performing an auto-negotiation algorithm which allows the link-partners to determine the best link parameters. The Ethernet controller on the TXMC387 is user configurable via configuration and register accesses over the PCIe interface.

LEDs indicate the different network activities.

The TXMC387 routes both Ethernet ports which are galvanically isolated from the Ethernet controllers to the XMC back I/O P16 connector. On the TXMC387-10R the Ethernet ports are mapped in the X12d range specified in VITA46.9 standard. The TXMC387-20R maps both Ethernet ports in the X8d range specified in VITA46.9 standard.

The module meets the requirements to operate in extended temperature range from -40°C to +85°C (Card Edge Temperature).

Software support:

- Software support for Intel™ X540 at www.intel.com
- For operating systems not supported by Intel™, please contact TEWS.

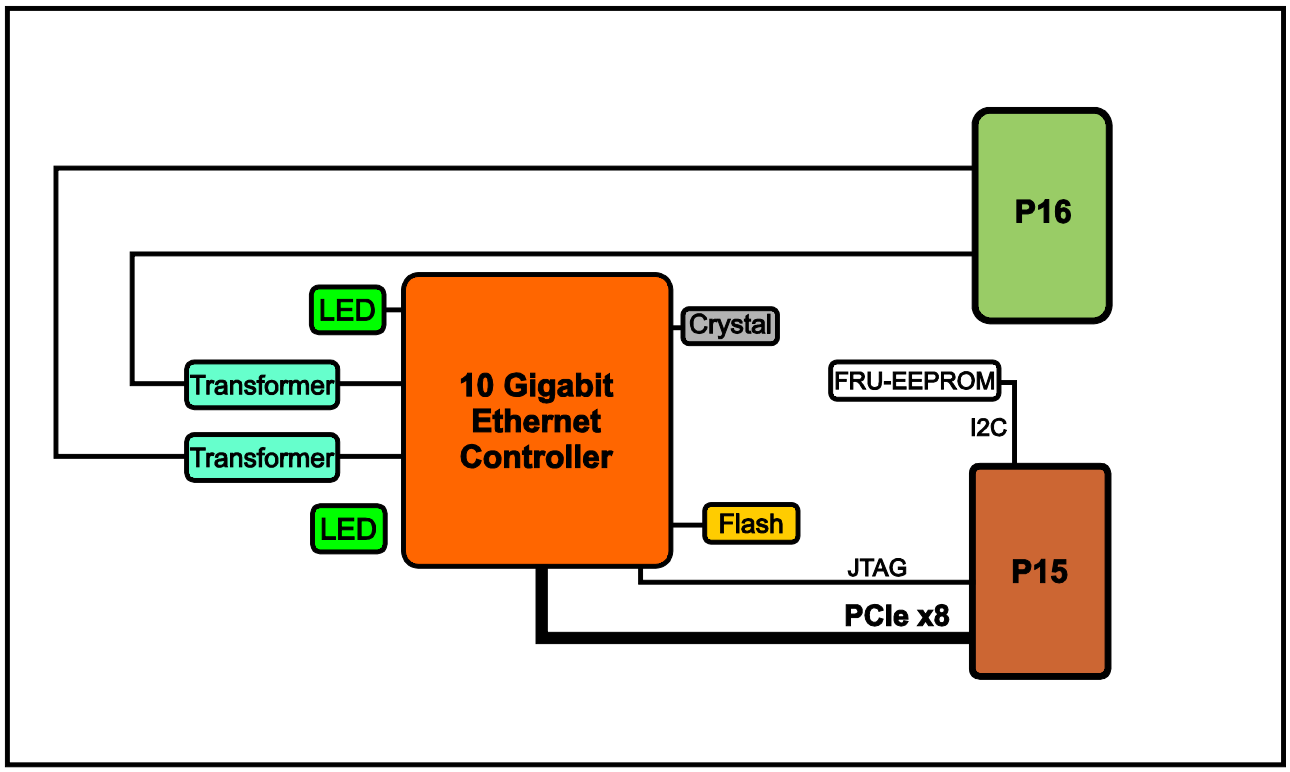

Figure 1-1 : Block Diagram

2 Technical Specification

XMC Interface		
Mechanical Interface	Conduction Cooled Switched Mezzanine Card (CCXMC) Interface conforming to ANSI/VITA 42.0-2008 (Auxiliary Standard) Standard single-width (143.75mm x 74mm)	
Electrical Interface	PCI Express (Base Specification 2.1) up to x8 compliant interface conforming to ANSI/VITA 42.3-2006 (XMC PCI Express Protocol Layer Standard)	
On Board Devices		
10 Gigabit Ethernet Controller	X540 (Intel)	
IPMI resource FRU Data EEPROM	M24C02 (STMicroelectronics)	
Ethernet Interface		
Number of Interfaces	2	
Link	100Base-TX / 1000Base-T / 10GBase-T	
I/O Connector	XMC P16 back I/O (Samtec ASP-105885-01 or compatible)	
Physical Data		
Power Requirements	450mA typical @ VPWR = +12V DC (no link) app. -40mA per 100Mbit/s link app. additional 65mA per 1Gbit/s link app. additional 300mA per 10Gbit/s link 1000mA typical @ VPWR = +5V DC (no link) app. -80mA per 100Mbit/s link app. additional 175mA per 1Gbit/s link app. additional 800mA per 10Gbit/s link 1mA typical @ +3.3V DC	
Temperature Range	Operating Storage	-40°C to +85°C (Card Edge Temperature) -40°C to +85°C
MTBF	592000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.	
Humidity	5 – 95 % non-condensing	
Weight	88 g	

Table 2-1 : Technical Specification

3 10 Gigabit Ethernet Controller

3.1 PCI Bus Topology

The Intel X540 10 Gigabit Ethernet Controller is represented by a multifunctional device on the PCI bus. The two different Ethernet Channels can be identified by the corresponding function of the device.

Multifunctional device (Intel Corporation)

Bus : Device : **Function 0x00**

Ethernet Controller	
Vendor ID	0x8086 (Intel Corporation)
Device ID	0x1528 (Ethernet Controller 10-Gigabit X540-AT2

Bus : Device : **Function 0x01**

Ethernet Controller	
Vendor ID	0x8086 (Intel Corporation)
Device ID	0x1528 (Ethernet Controller 10-Gigabit X540-AT2

3.2 Intel X540 Function PCI Header

PCI CFG Register Address	Write '0' to all unused (Reserved) bits								PCI writeable	Initial Values (Hex Values)
	31	24	23	16	15	8	7	0		
0x00	Device ID				Vendor ID				N	1528 8086
0x04	Status Register				Command Register				Y	0010 0406
0x08	Class Code		Subclass		Programming Interface		Revision ID		Y[7:0]	02 00 00 10
0x0C	BIST		Header Type		Latency Timer		Cache Line Size		Y[7:0]	00 80 00 10
0x10	Base Address Register 0								Y	F000000C
0x14	Base Address Register 1								Y	00000000
0x18	Base Address Register 2								Y	00000000
0x1C	Base Address Register 3								Y	00000000
0x20	Base Address Register 4								Y	F040000C
0x24	Base Address Register 5								Y	00000000
0x28	CardBus CIS								N	00000000
0x2C	Subsystem Device ID				Subsystem Vendor ID				N	0001 8086
0x30	Expansion ROM								Y	00000000
0x34	Reserved						Capabilities Pointer		N	000000 40
0x38	Reserved								N	00000000
0x3C	Max_Lat		Min_Gnt		Interrupt Pin		Interrupt Line		Y[7:0]	00 00 **01/02** 00
0x40	PMC				Next_Item_Ptr		Cap_ID		N	4823 50 01
0x44	Data Register		PMCSR_BSE		PMCSR				Y	00 00 1E00

Table 3-1 : Intel X540 PCI Header

4 LEDs

The TXMC387 provides a **Link/Activity LED** and a **Speed LED** for each of the two channels for quick visual inspection and debugging.

LED indicators are visible on the back side of the TXMC387 due to the fact that XMCs are mounted headfirst on the carrier card. A marking is placed close to each LED to indicate the Ethernet Port that corresponds to the LED.

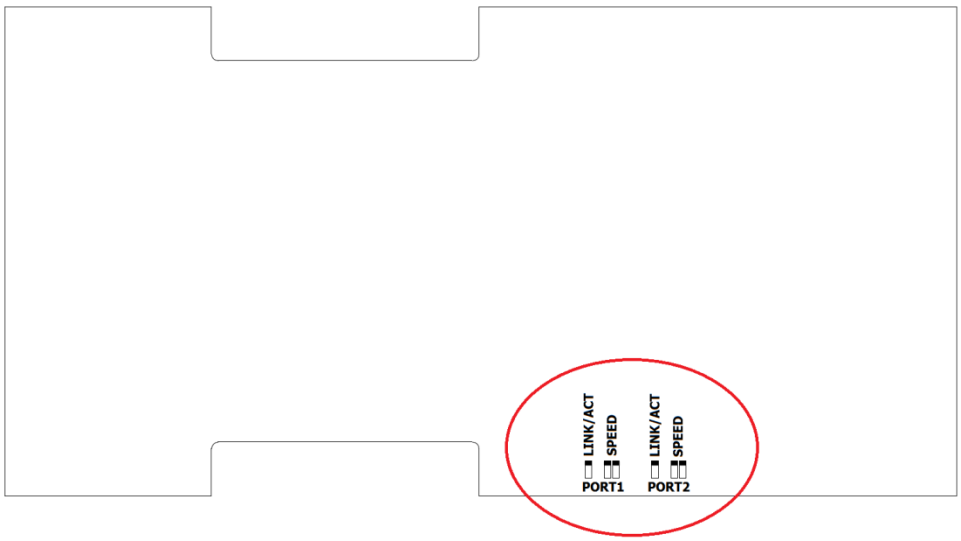

Figure 4-1 : LEDs (TXMC387 bottom view)

Link/Activity LED (green)	Description
OFF	No cable is connected or no link is established
ON	A link is established at the corresponding Ethernet Port
BLINKING	Indicates activity: The Ethernet Port transmits or receives data

Speed LED (multicolor)	Description
OFF	The speed of the link is 100 Mbit/s
ORANGE	The speed of the link is 1 Gbit/s
GREEN	The speed of the link is 10 Gbit/s

Table 4-1 : LED Status

5 Temperature Range

To be able to operate the TXMC387 at the specified maximum card edge temperature its thermal connection to the thermal interface of the carrier board has to be as good as possible.

Both, the Primary Thermal Interface and the Secondary Thermal Interface should be connected to the carrier board and if possible the whole heat sink of the TXMC387 should be thermally connected to the thermal interface of the carrier.

6 Pin Assignment – I/O Connector

6.1 XMC Connector P15

	A	B	C	D	E	F
1	PET0p0	PET0n0	3.3V	PET0p1	PET0n1	VPWR
2	GND	GND	$\overline{TRST}$	GND	GND	$\overline{PERST}$
3	PET0p2	PET0n2	3.3V	PET0p3	PET0n3	VPWR
4	GND	GND	TCK	GND	GND	$\overline{MRSTO}$
5	PET0p4	PET0n4	3.3V	PET0p5	PET0n5	VPWR
6	GND	GND	TMS	GND	GND	+12V
7	PET0p6	PET0n6	3.3V	PET0p7	PET0n7	VPWR
8	GND	GND	TDI	GND	GND	-12V
9	Reserved	Reserved	Reserved	Reserved	Reserved	VPWR
10	GND	GND	TDO	GND	GND	GA0
11	PER0p0	PER0n0	$\overline{MBIST}$	PER0p1	PER0n1	VPWR
12	GND	GND	GA1	GND	GND	$\overline{MPRESENT}$
13	PER0p2	PER0n2	3.3V AUX	PER0p3	PER0n3	VPWR
14	GND	GND	GA2	GND	GND	MSDA
15	PER0p4	PER0n4	Reserved	PER0p5	PER0n5	VPWR
16	GND	GND	MVMRO	GND	GND	MSCL
17	PER0p6	PER0n6	Reserved	PER0p7	PER0n7	Reserved
18	GND	GND	Reserved	GND	GND	Reserved
19	REFCLK+0	REFCLK-0	Reserved	$\overline{WAKE}$	$\overline{ROOT0}$	Reserved

Table 6-1 : XMC Connector P15

6.2 TXMC387-10 Back I/O Connector P16 (X12d)

	A	B	C	D	E	F
1	NC	NC	NC	NC	NC	NC
2	NC	NC	NC	NC	NC	NC
3	NC	NC	NC	NC	NC	NC
4	NC	NC	NC	NC	NC	NC
5	PORT1_MDI0+	PORT1_MDI0-	NC	PORT1_MDI1+	PORT1_MDI1-	NC
6	NC	NC	NC	NC	NC	NC
7	PORT1_MDI2+	PORT1_MDI2-	NC	PORT1_MDI3+	PORT1_MDI3-	NC
8	NC	NC	NC	NC	NC	NC
9	NC	NC	NC	NC	NC	NC
10	NC	NC	NC	NC	NC	NC
11	NC	NC	NC	NC	NC	NC
12	NC	NC	NC	NC	NC	NC
13	NC	NC	NC	NC	NC	NC
14	NC	NC	NC	NC	NC	NC
15	PORT2_MDI0+	PORT2_MDI0-	NC	PORT2_MDI1+	PORT2_MDI1-	NC
16	NC	NC	NC	NC	NC	NC
17	PORT2_MDI2+	PORT2_MDI2-	NC	PORT2_MDI3+	PORT2_MDI3-	NC
18	NC	NC	NC	NC	NC	NC
19	NC	NC	NC	NC	NC	NC

Table 6-2 : TXMC387-10 Back I/O Connector P16 (X12d mapping per VITA46.9)

6.3 TXMC387-20 Back I/O Connector P16 (X8d)

	A	B	C	D	E	F
1	PORT1_MDI0+	PORT1_MDI0-	NC	PORT1_MDI1+	PORT1_MDI1-	NC
2	NC	NC	NC	NC	NC	NC
3	PORT1_MDI2+	PORT1_MDI2-	NC	PORT1_MDI3+	PORT1_MDI3-	NC
4	NC	NC	NC	NC	NC	NC
5	NC	NC	NC	NC	NC	NC
6	NC	NC	NC	NC	NC	NC
7	NC	NC	NC	NC	NC	NC
8	NC	NC	NC	NC	NC	NC
9	NC	NC	NC	NC	NC	NC
10	NC	NC	NC	NC	NC	NC
11	PORT2_MDI0+	PORT2_MDI0-	NC	PORT2_MDI1+	PORT2_MDI1-	NC
12	NC	NC	NC	NC	NC	NC
13	PORT2_MDI2+	PORT2_MDI2-	NC	PORT2_MDI3+	PORT2_MDI3-	NC
14	NC	NC	NC	NC	NC	NC
15	NC	NC	NC	NC	NC	NC
16	NC	NC	NC	NC	NC	NC
17	NC	NC	NC	NC	NC	NC
18	NC	NC	NC	NC	NC	NC
19	NC	NC	NC	NC	NC	NC

Table 6-3 : TXMC387-20 Back I/O Connector P16 (X8d mapping per VITA46.9)