The Embedded I/O Company

TEWS TECHNOLOGIES

TXMC391

Conduction Cooled, 4 Channel 1000BASE-KX Ethernet

Version 1.0

User Manual

Issue 1.0.1

March 2026

TEWS Technologies GmbH
Eggerstedter Weg 14, 25421 Pinneberg, Germany
Phone: +49 (0) 4101 4058 0
info@tews.com www.tews.com

TXMC391-10R

4 Channel 1000BASE-KX Ethernet; P16 Back I/O (X12d); Conduction Cooled; IEEE 1588 auxiliary devices via single-ended Back I/O

(RoHS compliant)

TXMC391-20R

4 Channel 1000BASE-KX Ethernet; P16 Back I/O (X12d); Conduction Cooled; IEEE 1588 auxiliary devices via differential Back I/O

(RoHS compliant)

Document History

Issue	Description	Date
1.0.0	Initial Issue	May 2025
1.0.1	Variant -20R added supporting IEEE 1588 auxiliary devices via differential Back I/O	March 2026

Table of Contents

List of Figures

List of Tables

1 Product Description

The TXMC391 is a Conduction Cooled Switched Mezzanine Card (CCXMC) compatible module providing a four channel 1000Base-KX Ethernet interface.

A PCIe Switch provides access to the Intel I210IS Gigabit Ethernet controllers. Each Ethernet interface supports 1000 Mbit/s transmission rate and is equipped with a 16 Mbit Serial Flash to support PXE and iSCSI boot.

The TXMC391 routes four Ethernet ports to the Back I/O P16 connector. All ports are mapped in the X12d range specified in VITA46.9 standard.

LEDs on the board indicate the different network activities.

The TXMC391 supports IEEE 1588/802.1AS Precision Time Protocol (PTP) and IEEE 802.1Qav Audio/Video Bridging (AVB) traffic shaping (with software extensions).

The SDP (Software Definable Pins) of each Ethernet Controller are connected to the Back I/O P16 connector for IEEE 1588 auxiliary device connections.

The TXMC391-10R routes these SDP directly to the Back I/O P16 connector. The TXMC391-20R has M-LVDS Transceivers between the Ethernet Controllers' SDP and the Back I/O P16 connector to allow differential IEEE 1588 auxiliary device connections, the direction of these Transceivers is configured by the SDP.

The TXMC391 has an I²C board temperature sensor to facilitate measurement of the board heat near the Primary Thermal Interface of the Conduction Cooled Frame.

The module meets the requirements to operate in extended temperature range from -40°C to +85°C (Card Edge Temperature).

Software Support:

- Software support for Intel I210IS at www.intel.com
- For operating systems not supported by Intel, please contact TEWS.

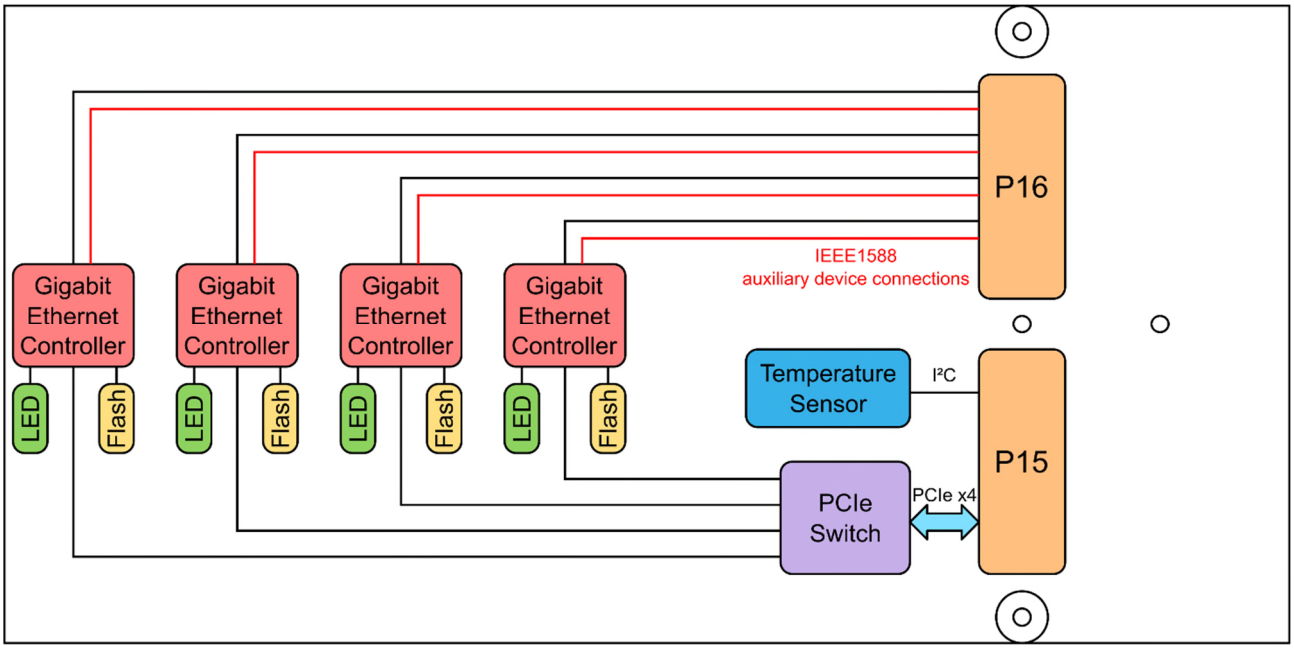

Figure 1-1 : Block Diagram

2 Technical Specification

General	
Mechanical Interface	Conduction Cooled Switched Mezzanine Card (CCXMC) Interface conforming to ANSI/VITA 42.0 and ANSI/VITA 20 Standard single-width (143.75 mm x 74 mm)
Electrical Interface	x4 PCI Express (Specification 2.1) compliant interface conforming to ANSI/VITA 42.3

Main On Board Devices	
PCIe Switch	PI7C9X2G608GP (Diodes Incorporated)
Gigabit Ethernet Controllers	For each interface: I210-IS (Intel)
16 Mbit Serial Flashes for Boot ROM	For each interface: W25Q16JV (Winbond)
Temperature Sensor	PCT2075 (NXP Semiconductors)
FRU Records EEPROM	M24C02-R (STMicroelectronics)
M-LVDS Transceivers (TXMC391-20R)	SN65MLVD204B (Texas Instruments)

I/O Interface	
Number of Channels	4
I/O Standard	1000Base-KX
I/O Connector	Back I/O P16 (Samtec ASP-103614-04 or compatible) All ports mapped in X12d range (VITA46.9)

Physical Data	
Power Requirements	650mA typical @ VPWR = +5V (four channel, no link) 300mA typical @ VPWR = +12V (four channel, no link)
Temperature Range	Operating -40 °C to +85 °C (Card Edge Temperature) Storage -40 °C to +85 °C
MTBF	TXMC391-10R: 943000 h TXMC391-20R: 908000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	63 g

Table 2-1 : Technical Specification

3 Handling and Operation Instructions

3.1 ESD Protection

This CCXMC module is sensitive to static electricity.
Packing, unpacking and all other module handling has to be done with appropriate care!

3.2 Conduction Cooling

This CCXMC module generates noticeable heat and requires adequate conduction cooling!

4 PCI Express Interface

4.1 PCI Express Device Topology

The TXMC391 uses four Gigabit Ethernet Controllers (Intel I210-IS) each communicating via a PCIe Rev. 2.1 compliant x1 Interface at 2.5 GT/s.

To be able to access the Ethernet controllers they are connected to the x1 Downstream Ports of a Gen 2 PCIe Switch (Diodes Incorporated PI7C9X2G608GP).

The x4 Upstream Port of the PCIe Switch is connected to the host system.

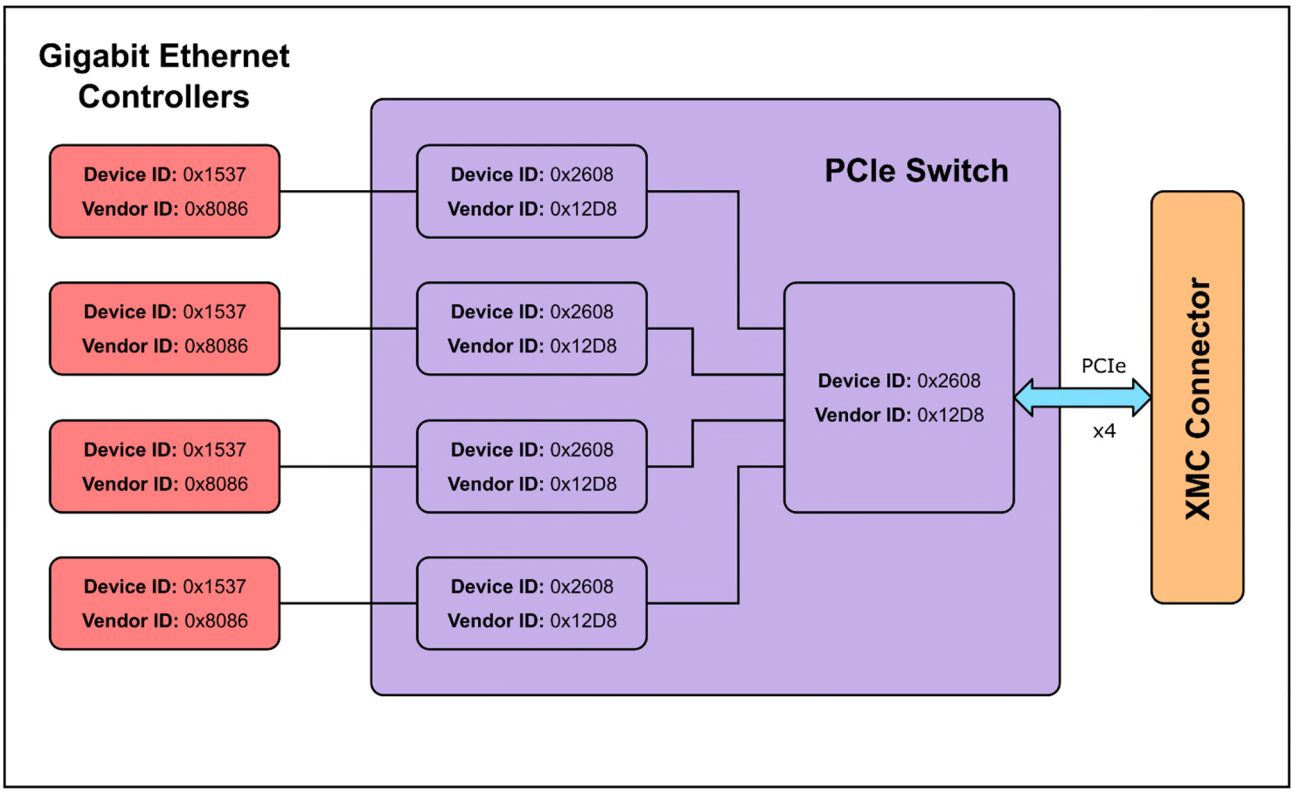

Figure 4-1 : PCI Express Device Topology

4.2 PCI Express Memory and I/O Size Requirements

PCIe Space Mapping	Four Channel (Byte)
MEM	4M
I/O	16K

Table 4-1 : PCI Express Memory and I/O Size Requirements

4.3 I210 PCI Express Identifiers

Vendor-ID	0x8086 (Intel)
Device-ID	0x1537 (I210-IS 1000BASE-KX backplane)
Class Code	0x020000 (Ethernet Controller)
Subsystem Vendor-ID	0xFFFF
Subsystem Device-ID	0x0000

Table 4-2 : I210 PCI Express Identifiers

4.4 I210 PCI Express Base Address Register Configuration

PCIe Base Address Register (Offset in PCIe Configuration Space)	PCIe Space Mapping	Size (Byte)	Description
0 (0x10)	MEM	128K	Internal Registers
1 (0x14)	-	-	-
2 (0x18)	I/O	32	Internal Registers via I/O Space
3 (0x1C)	MEM	16K	MSI-X

Table 4-3 : I210 PCI Express Base Address Register Configuration

5 Ethernet Interface Status LEDs

The TXMC391 provides an individual Status LED for every Ethernet Interface. Due to the fact that CCXMCs are mounted upside-down on the carrier card the Status LEDs are visible on the back side of the TXMC391. A marking is placed close to each Status LED to indicate the Ethernet Port it corresponds to.

See table below for more details:

Status LED	Description
OFF	No cable is connected or no link is established
ON	A link is established
BLINKING	Activity (the Ethernet Port transmits or receives data)

Table 5-1 : Status LED

6 Synchronization with IEEE 1588 Auxiliary Devices

The TXMC391 supports IEEE 1588/802.1AS Precision Time Protocol (PTP).

If you additionally want to synchronize with IEEE 1588 auxiliary devices, this can be realized via the Ethernet Controllers' GPIO Software-Definable Pins (SDPx) that are connected to the Back I/O P16 connector.

6.1 TXMC391-10R

On the TXMC391-10R all four of the Ethernet Controllers' GPIO Software-Definable Pins (SDP0 to SDP3) are directly connected to the Back I/O P16 connector.

The electrical characteristics of the Ethernet Controllers' GPIO Pins are listed in the following table:

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output High Voltage	I_{OH} = -8 mA; VCC3P3 = Min	2.4		V
		I_{OH} = -100 µA; VCC3P3 = Min	VCC3P3 - 0.2		V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA; VCC = Min		0.4	V
		I_{OL} = 100 µA; VCC = Min		0.2	V
V_{IH}	Input High Voltage		0.7 * VCC3P3	VCC3P3 + 0.4	V
V_{IL}	Input Low Voltage		-0.4	0.3 * VCC3P3	V

Table 6-1 : Electrical characteristics of Ethernet Controllers' GPIO Pins

6.2 TXMC391-20R

On the TXMC391-20R two of the Ethernet Controllers' GPIO Software-Definable Pins (SDP0 and SDP1) are connected to the Back I/O P16 connector via M-LVDS Transceivers.

The other two of the Ethernet Controllers' GPIO Software-Definable Pins (SDP2 and SDP3) are used to configure the direction of the M-LVDS Transceivers.

GPIO	Connection	Low	High
SDP0	ETHERNET_x_SDP0+ ETHERNET_x_SDP0-		
SDP1	ETHERNET_x_SDP1+ ETHERNET_x_SDP1-		
SDP2	ETHERNET_x_SDP0_DIR	SDP0 is an Input	SDP0 is an Output
SDP3	ETHERNET_x_SDP1_DIR	SDP1 is an Input	SDP1 is an Output

Table 6-2 : SDPx Pin Connection

At power-up SDP2 and SDP3 configure the M-LVDS Transceivers to operate as Inputs, driving data from the differential M-LVDS interface at the Back I/O P16 connector to the SDP0 and SDP1 pins of the Ethernet Controllers.

7 Pin Assignment – I/O Connectors

7.1 Back I/O P16 Connector (TXMC391-10R)

7.1.1 Connector Type

Pin-Count	114
Connector Type	XMC Connector 114-pol Male
Source & Order Info	Samtec ASP-103614-04 or compatible

Table 7-1 : Back I/O P16 Connector Type

7.1.2 Pin Assignment

	A	B	C	D	E	F
19	ETHERNET_2_TX-	ETHERNET_2_TX+	ETHERNET_2_SDP0	ETHERNET_2_RX-	ETHERNET_2_RX+	ETHERNET_2_SDP1
18	GND	GND	ETHERNET_2_SDP2	GND	GND	ETHERNET_2_SDP3
17	ETHERNET_3_TX-	ETHERNET_3_TX+	ETHERNET_3_SDP0	ETHERNET_3_RX-	ETHERNET_3_RX+	ETHERNET_3_SDP1
16	GND	GND	ETHERNET_3_SDP2	GND	GND	ETHERNET_3_SDP3
15	ETHERNET_4_TX-	ETHERNET_4_TX+	ETHERNET_4_SDP0	ETHERNET_4_RX-	ETHERNET_4_RX+	ETHERNET_4_SDP1
14	GND	GND	ETHERNET_4_SDP2	GND	GND	ETHERNET_4_SDP3
13	NC	NC	NC	NC	NC	NC
12	GND	GND	NC	GND	GND	NC
11	NC	NC	NC	NC	NC	NC
10	GND	GND	NC	GND	GND	NC
9	ETHERNET_1_TX-	ETHERNET_1_TX+	ETHERNET_1_SDP0	ETHERNET_1_RX-	ETHERNET_1_RX+	ETHERNET_1_SDP1
8	GND	GND	ETHERNET_1_SDP2	GND	GND	ETHERNET_1_SDP3
7	NC	NC	NC	NC	NC	NC
6	GND	GND	NC	GND	GND	NC
5	NC	NC	NC	NC	NC	NC
4	GND	GND	NC	GND	GND	NC
3	NC	NC	NC	NC	NC	NC
2	GND	GND	NC	GND	GND	NC
1	NC	NC	NC	NC	NC	NC

Table 7-2 : Back I/O P16 Pin Assignment (TXMC391-10R)

All ports lie within the X12d mapping (VITA46.9)

7.2 Back I/O P16 Connector (TXMC391-20R)

7.2.1 Connector Type

Pin-Count	114
Connector Type	XMC Connector 114-pol Male
Source & Order Info	Samtec ASP-103614-04 or compatible

Table 7-3 : Back I/O P16 Connector Type

7.2.2 Pin Assignment

	A	B	C	D	E	F
19	ETHERNET_2_TX-	ETHERNET_2_TX+	ETHERNET_2_SDP0+	ETHERNET_2_RX-	ETHERNET_2_RX+	ETHERNET_2_SDP1+
18	GND	GND	ETHERNET_2_SDP0-	GND	GND	ETHERNET_2_SDP1-
17	ETHERNET_3_TX-	ETHERNET_3_TX+	ETHERNET_3_SDP0+	ETHERNET_3_RX-	ETHERNET_3_RX+	ETHERNET_3_SDP1+
16	GND	GND	ETHERNET_3_SDP0-	GND	GND	ETHERNET_3_SDP1-
15	ETHERNET_4_TX-	ETHERNET_4_TX+	ETHERNET_4_SDP0+	ETHERNET_4_RX-	ETHERNET_4_RX+	ETHERNET_4_SDP1+
14	GND	GND	ETHERNET_4_SDP0-	GND	GND	ETHERNET_4_SDP1-
13	NC	NC	NC	NC	NC	NC
12	GND	GND	NC	GND	GND	NC
11	NC	NC	NC	NC	NC	NC
10	GND	GND	NC	GND	GND	NC
9	ETHERNET_1_TX-	ETHERNET_1_TX+	ETHERNET_1_SDP0+	ETHERNET_1_RX-	ETHERNET_1_RX+	ETHERNET_1_SDP1+
8	GND	GND	ETHERNET_1_SDP0-	GND	GND	ETHERNET_1_SDP1-
7	NC	NC	NC	NC	NC	NC
6	GND	GND	NC	GND	GND	NC
5	NC	NC	NC	NC	NC	NC
4	GND	GND	NC	GND	GND	NC
3	NC	NC	NC	NC	NC	NC
2	GND	GND	NC	GND	GND	NC
1	NC	NC	NC	NC	NC	NC

Table 7-4 : Back I/O P16 Pin Assignment (TXMC391-20R)

All ports lie within the X12d mapping (VITA46.9)