The Embedded I/O Company

TEWS TECHNOLOGIES

TXMC463

4 Channel Serial Interface RS232/RS422

Version 1.0

User Manual

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TXMC463-10R

4 Channel Serial RS232, front panel I/O

TXMC463-11R

4 Channel Serial RS422, front panel I/O

TXMC463-12R

2 Channel Serial RS232, 2 Channel Serial RS422, front panel I/O

TXMC463-15R

4 Channel Serial RS232, front panel I/O, with non-standard RJ45 I/O pinout

Additional P14 or P16 back I/O is available on request.

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	Initial Issue	July 2015
1.0.1	Clarified “x1” PCIe Interface	February 2016

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1 Product Description

The TXMC463 is a standard Switched Mezzanine Card (XMC) compatible module offering 4 channels of high performance asynchronous serial interface.

All modules offer front panel I/O with four RJ45 connectors. Four different standard modules are available: The TXMC463-10R and -15R provide 4 RS232 interfaces. The TXMC463-11R provides 4 RS422 interfaces. The TXMC463-12R provides 2 RS232 and 2 RS422 interfaces. The TXMC463-15R uses a non-standard RJ45 I/O pinout (as used on Motorola CPU boards).

Other configurations are available as factory build option on a per channel base.

Each RS232 channel supports TxD, RxD, CTS, RTS, DTR, CD, DSR/RI and GND. Each RS422 channel supports RxD+/-, TxD+/- and GND.

Each channel has 256 byte transmit and receive FIFOs to significantly reduce the overhead required to provide data to and get data from the transmitters and receivers. The FIFO trigger levels are programmable and the baud rate is individually programmable up to 1 Mbps for RS232 channels and 16 Mbps for RS422 channels. The UART offers readable FIFO levels.

All serial channels use ESD protected transceivers. ESD protection is up to ±15KV.

Software Support (TDRV002-SW-xx) for different operating systems is available.

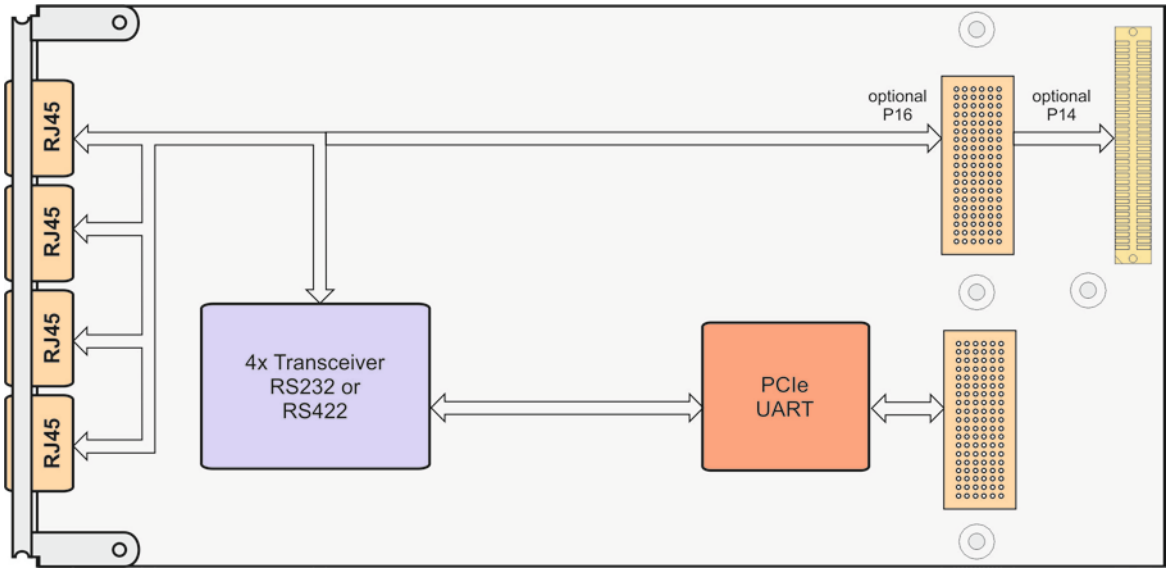


Figure 1-1 : Block Diagram

2 Technical Specification

XMC Interface		
Mechanical Interface	Switched Mezzanine Card (XMC) Interface confirming to ANSI/VITA 42.0-2008 and ANSI/VITA 20-2001 (R2005) Standard single-width (149mm x 74mm)	
Electrical Interface	x1 PCI Express (Base Specification 2.0 Gen 1) compliant interface conforming to ANSI/VITA 42.3-2006 (XMC PCI Express Protocol Layer Standard)	
On Board Devices		
PCIe Target Chip	XR17V354 (Exar)	
Transceiver	RS232: MAX3245E (or equivalent) RS422: MAX3077E (or equivalent)	
IPMI Support	per serial EEPROM, as defined in ANSI/VITA 42.0-2008	
I/O Interface		
Interface Type	Asynchronous serial interface	
Number of Channels	4	
Physical Interface	TXMC463-10R: 4 RS232 TXMC463-11R: 4 RS422 TXMC463-12R: 2 RS232, 2 RS422 TXMC463-15R: 4 RS232 (Motorola compatible pinout)	
Serial Channel I/O Signals	RS232: TxD, RxD, RTS, CTS, DTR, CD, DSR/RI, GND RS422: TxD+/-, RxD+/-, GND	
Termination	RS422: 120Ω between RxD+/- of each channel	
Programmable Baud Rates	RS232: up to 1 Mbps RS422: up to 16 Mbps	
ESD Protection	RS232: ±15kV—Human Body Model ±8kV—IEC 1000-4-2, Contact Discharge ±15kV—IEC 1000-4-2, Air-Gap Discharge RS422: ±15kV—Human Body Model	
I/O Connector	4x RJ45 Modular Jack (e.g. AMP# 406 732-1)	
Physical Data		
Power Requirements	VPWR is not used TXMC463-10R: 70 mA typical @ +3.3V DC TXMC463-11R: 110 mA typical @ +3.3V DC (no load) TXMC463-12R: 90 mA typical @ +3.3V DC (no load) TXMC463-15R: 70 mA typical @ +3.3V DC (no load)	
Temperature Range	Operating Storage	-40 °C to +85 °C -40 °C to +85 °C

MTBF	740.000 h MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C. The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.
Humidity	5 – 95 % non-condensing
Weight	66 g

Table 2-1 : Technical Specification

2.1 Compatibility Identification Block

The ANSI/VITA 42.0 specification demands that a compatibility identification block is published, which identifies supported protocols for each implemented XMC connector.

Standard XMC.3		
P15		
PCIe		
Standard		
1 Lane	Link 0	2.5Gb/s

3 Local Space Addressing

3.1 XR17V354 Local Space Configuration

The local on board addressable regions are accessed from the PCI side by using the XR17V354 local space.

XR17V354 PCI Base Address (Offset in PCI Configuration Space)	PCI Space Mapping	Size (Byte)	Port Width (Bit)	Endian Mode	Description
0 (0x10)	MEM	16k	32	BIG	Device Configuration Space

Table 3-1 : XR17V354 Local Space Configuration

3.2 Device Configuration Space

PCI Base Address: XR17V354 PCI Base Address 0 (Offset 0x10 in PCI Configuration Space).

The TXMC463 uses the Exar XR17V354 Quad UART to provide and control the 4 channels.

Device Configuration Space Content	PCI Address	Size (Bit)
UART 0 Register Set	PCI Base Address 0 + (0x0000 to 0x03FF)	32
UART 1 Register Set	PCI Base Address 0 + (0x0400 to 0x07FF)	32
UART 2 Register Set	PCI Base Address 0 + (0x0800 to 0x0BFF)	32
UART 3 Register Set	PCI Base Address 0 + (0x0C00 to 0x0FFF)	32

Table 3-2 : Device Configuration Space

All registers can be accessed in 8, 16, 24 or 32 bit width with exception to one special case: When reading the receive data together with its LSR register content, the host must read them in 16 or 32 bits format in order to maintain integrity of the data byte with its associated error flags.

3.2.1 UART Register Sets

The Device Configuration Space provides a register set for each of the 4 UARTs.

UART Register Set	Register Set Offset
Serial Channel 0	0x0000
Serial Channel 1	0x0400
Serial Channel 2	0x0800
Serial Channel 3	0x0C00

Table 3-3 : UART Register Set Offset

Offset Address	Description	Access	Data Width
0x0000 – 0x000F	UART Channel Configuration Registers First 8 registers are 16550 compatible	R/W	8, 16, 24, 32
0x0010 – 0x007F	Reserved	-	-
0x0080 – 0x009A	Device Configuration Registers	R/W	8, 16, 24, 32
0x009B – 0x00FF	Reserved	-	-
0x0100 – 0x01FF	Read FIFO – 256 bytes of RX FIFO data	R	8, 16, 24, 32
	Write FIFO – 256 bytes of TX FIFO data	W	8, 16, 24, 32
0x0200 – 0x03FF	Read FIFO with errors – 256 bytes of RX FIFO data + LSR	R	16, 32

Table 3-4 : UART Register Set

3.2.2 Device Configuration Registers

The Device Configuration Registers control general operating conditions and monitor the status of various functions. This includes a 16 bit general purpose counter, multipurpose input/outputs (not supported by the TXMC463), sleep mode, soft-reset and device identification, and revision. They are embedded inside the UART register sets. Some registers are accessible from the Device Configuration Registers in all UART register sets, but control only the bit for that channel.

Address	Register	Description	Access	Reset Value
0x080	INT0 [7:0]	Channel Interrupt Indicator	R	0x00
0x081	INT1 [15:8]	Interrupt Source Details	R	0x00
0x082	INT2 [23:16]		R	0x00
0x083	INT3 [31:24]		R	0x00
0x084	TIMERCNTL	Timer Control Register	R/W	0x00
0x085	REGA	Reserved	-	0x00
0x086	TIMERLSB	Programmable Timer Value	R/W	0x00
0x087	TIMERMSB		R/W	0x00
0x088	8XMODE	8X Sampling Rate Enable	R/W	0x00
0x089	4XMODE	4X Sampling Rate Enable	R/W	0x00
0x08A	RESET	UART Reset	W	0x00
0x08B	SLEEP	UART Sleep Mode Enable	R/W	0x00
0x08C	DREV	Device Revision	R	Rev.
0x08D	DVID	Device Identification	R	0x88
0x08E	REGB	Simultaneous UART Write & EEPROM Interface	R/W	0x00
0x08F	MPIOINT	MPIO[7:0] Interrupt Mask	R/W	0x00
0x090	MPIOLVL	MPIO[7:0] Level Control	R/W	0x00
0x091	MPIO3T	MPIO[7:0] Output Pin Tri-state Control	R/W	0x00
0x092	MPIOINV	MPIO[7:0] Input Polarity Select	R/W	0x00
0x093	MPIOSEL	MPIO[7:0] Input/Output Select	R/W	0xFF
0x094	MPIOOD	MPIO[7:0] Open Drain Output Control	R/W	0x00
0x095	MPIOINT	MPIO[15:8] Interrupt Mask	R/W	0x00
0x096	MPIOLVL	MPIO[15:8] Level Control	R/W	0x00
0x097	MPIO3T	MPIO[15:8] Output Pin Tri-state Control	R/W	0x00
0x098	MPIOINV	MPIO[15:8] Input Polarity Select	R/W	0x00
0x099	MPIOSEL	MPIO[15:8] Input/Output Select	R/W	0xFF
0x09A	MPIOD	MPIO[15:8] Open Drain Output Control	R/W	0x00
0x09B	Reserved		-	0x00

Table 3-5 : Device Configuration Registers

For a detailed description of the Device Configuration Registers please refer to the XR17V354 data sheet which is available on the Exar website (www.exar.com).

3.2.3 UART Channel Configuration Registers

Each UART channel has its own set of internal UART configuration registers for its own operation control and status reporting. The following table provides the register offsets within a register set, access types and access control:

Register Offset	Comment	Register	Access	Reset Value
16550 Compatible				
0x00	LCR[7] = 0	RHR – Receive Holding Register THR – Transmit Holding Register	R W	0xXX
	LCR[7] = 1	DLL – Baud Rate Generator Divisor Latch Low	R/W	0xXX
0x01	LCR[7] = 0	IER – Interrupt Enable Register	R/W	0x00
	LCR[7] = 1	DLM – Baud Rate Generator Divisor Latch High	R/W	0xXX
0x02	LCR[7] = 0	ISR – Interrupt Status Register FCR – FIFO Control Register	R W	0x01 0x00
	LCR[7] = 1	DLD – Divisor Fractional	R/W	0xXX
0x03		LCR – Line Control Register	R/W	0x00
0x04		MCR – Modem Control Register	R/W	0x00
0x05		LSR – Line Status Register Reserved	R W	0x60
0x06		MSR – Modem Status Register – Auto RS485 Delay (not supported by the TXMC463)	R W	0xX0
0x07	User Data	SPR – Scratch Pad Register	R/W	0xFF
Enhanced Registers				
0x08		FCTR – Feature Control Register	R/W	0x00
0x09		EFR – Enhanced Function Register	R/W	0x00
0x0A		TXCNT – Transmit FIFO Level Counter TXTRG – Transmit FIFO Trigger Level	R W	0x00
0x0B		RXCNT – Receiver FIFO Level Counter RXTRG – Receiver FIFO Trigger Level	R W	0x00
0x0C		Xchar – Xon, Xoff Received Flags Xoff-1 – Xoff Character 1	R W	0x00
0x0D		Reserved Xoff-2 – Xoff Character 2	R W	0x00
0x0E		Reserved Xon-1 – Xon Character 1	R W	0x00
0x0F		Reserved Xon-2 – Xon Character 2	R W	0x00

Table 3-6 : UART Channel Configuration Registers

The address for a UART Channel Configuration Register x in a UART Register Set for channel y is:

PCI Base Address 0 (PCI Base Address for the UART Register Space)

+ UART Register Set Offset for channel y

+ Register Offset for register x

Addressing example:

The address for the LCR register of UART channel 2 is:

PCI Base Address (PCI Base Address for the Device Configuration Space)

+ 0x0800 (Offset of the UART register set for serial channel 2)

+ 0x0003 (Offset of the LCR register within a UART register set)

For a detailed description of the serial channel registers please refer to the XR17V354 data sheet which is available on the Exar website (www.exar.com).

4 XR17V354 Target Chip

4.1 PCI Configuration Registers (PCR)

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	91CF 1498
0x04	Status		Command		Y	0080 0000
0x08	Class Code			Revision ID	N	070002 ??
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	N	00 00 00 00
0x10	Memory Base Address Register (BAR0)				Y	FFFFC000
0x14	Base Address Register (Unimplemented)				N	00000000
0x18	Base Address Register (Unimplemented)				N	00000000
0x1C	Base Address Register (Unimplemented)				N	00000000
0x20	Base Address Register (Unimplemented)				N	00000000
0x24	Base Address Register (Unimplemented)				N	00000000
0x28	Reserved				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	s.b. 1498
0x30	Expansion ROM Base Address (Unimplemented)				N	00000000
0x34	Reserved				N	00000000
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00

Table 4-1 : PCI Header

Device-ID:	0x91CF	TXMC463
Vendor-ID:	0x1498	TEWS TECHNOLOGIES
Revision ID:		XR17V354 silicon revision
Subsystem-ID:	0x900A	-10R
	0x900B	-11R
	0x900C	-12R
	0x900F	-15R
Subsystem Vendor-ID:	0x1498	TEWS TECHNOLOGIES

4.2 Configuration EEPROM

After power-on or PCI reset, the XR17V354 loads initial configuration register data from the on board configuration EEPROM.

The configuration EEPROM contains the following configuration data:

- Vendor ID
- Vendor Device ID
- Subsystem Vendor-ID
- Subsystem ID

See the XR17V354 Manual for more information.

Address	Configuration Register	Value
0x00	Address Word	0x0000
0x01	Vendor ID	0x1498
0x02	Address Word	0x8001
0x03	Device ID	0x91CF
0x04	Address Word	0x8004
0x05	Subsystem Vendor-ID	0x1498
0x06	Address Word	0x4005
0x07	Subsystem ID	s.b.

Table 4-2 : Configuration EEPROM TXMC463

Subsystem-ID Value (Offset 0x07): TXMC463-10R 0x900A

TXMC463-11R 0x900B

TXMC463-12R 0x900C

TXMC463-15R 0x900F

The words following the configuration data contain:

- The module version and revision
- The UART clock frequency in Hz
- The physical interface attached to the serial channels
- The maximal baud rate of the transceivers in bps
- The supported control signals of the serial channels

For the physical interfaces and the control signals applies: Bit 7 represents UART channel 7 and bit 0 represents UART channel 0. The appropriate bit is set to ‘1’ for each UART channel attached to the physical interface represented by the word. Bit 15 to bit 8 are always ‘0’.

Address	Configuration Register	-10R/-15R	-11R	-12R
0x08	Module Version	Reflects Module Version (i.e. V1.0)		
0x09	Module Revision	Reflects Module Revision (i.e. Rev.A)		
0x0A	EEPROM Revision	0x0003	0x0003	0x0003
0x0B	Oscillator Frequency (high)	0x0773	0x0773	0x0773
0x0C	Oscillator Frequency (low)	0x5940	0x5940	0x5940
0x0D-0x0E	Reserved	-	-	-
0x0F	Controller Type	0x0001	0x0001	0x0001
0x10	RS232 Channels	0x000F	0x0000	0x0003
0x11	RS422 Channels	0x0000	0x000F	0x000C
0x12	TTL Channels	0x0000	0x0000	0x0000
0x13	RS485 Full Duplex Channels	0x0000	0x0000	0x0000
0x14	RS485 Half Duplex Channels	0x0000	0x0000	0x0000
0x15-0x1E	Reserved	-	-	-
0x1F	Programmable Interfaces	0x0000	0x0000	0x0000
0x20	Max Data Rate RS232 (high)	0x000F	0x000F	0x000F
0x21	Max Data Rate RS232 (low)	0x4240	0x4240	0x4240
0x22	Max Data Rate RS422 (high)	0x00F4	0x00F4	0x00F4
0x23	Max Data Rate RS422 (low)	0x2400	0x2400	0x2400
0x24	Max Data Rate TTL (high)	0x0000	0x0000	0x0000
0x25	Max Data Rate TTL (low)	0x0000	0x0000	0x0000
0x26	Max Data Rate RS485 Full Duplex (high)	0x0000	0x0000	0x0000
0x27	Max Data Rate RS485 Full Duplex (low)	0x0000	0x0000	0x0000
0x28	Max Data Rate RS485 Half Duplex (high)	0x0000	0x0000	0x0000
0x29	Max Data Rate RS485 Half Duplex (low)	0x0000	0x0000	0x0000
0x2A-0x2F	Reserved	-	-	-
0x30	RxD & TxD	0x000F	0x000F	0x000F
0x31	RTS & CTS	0x000F	0x0000	0x0003
0x32	Full modem	0x000F	0x0000	0x0003
0x33-0x37	Reserved	-	-	
0x38	Enhanced RTS & CTS (Front- or Back I/O only)	0x0000	0x000F	0x0000
0x39	Enhanced Full modem (Front- or Back I/O only)	0x0000	0x0000	0x0000
0x3A	Channels with enhanced RTS & CTS Support for RS232 only	0x0000	0x0000	0x0000
0x3B	Channels with RxD support only	0x0000	0x0000	0x0000
0x3B-0x3F	Reserved	-	-	-

Table 4-3 : Physical Configuration EEPROM Data

5 Configuration Hints

The following chart shows the UART interface mapping of the different variants of the TXMC463.

	TXMC463-10R		TXMC463-11R		TXMC463-12R		TXMC463-15R	
	RS232	RS422	RS232	RS422	RS232	RS422	RS232	RS422
UART0	X			X	X		X	
UART1	X			X	X		X	
UART2	X			X		X	X	
UART3	X			X		X	X	

Table 5-1 : UART interface mapping

Other configurations are available as factory build option on a per channel base.

RS422 channels provide on board 120Ω termination resistors. Do not apply additional external termination resistors here.

6 Programming Hints

6.1 UART Baud Rate Programming

Each of the 4 UART channels of the TXMC463 provides a programmable Baud Rate Generator. The clock of the XR17V354 UART can be divided by any divisor from 1 to 2^{16} – 0.0625. The divisor can be programmed by the UART channel DLM (Divisor MSB), DLL (Divisor LSB) and DLD (Divisor Fractional) registers. After a reset bit 7 of the UART channels MCR register defaults to '0' and the divisor value is 0xFFFF.

The sampling rate for a UART channel can be set to 8x (normal operation is 16x) in the 8XMODE register or 4x in the 4XMODE register. Transmit and receive data rates will double by selecting 8x sample rate or quadruple by selecting the 4x sample rate.

The basic formula of baud rate programming is:

$$\text{Baud Rate} = \frac{125MHz}{MODE \cdot Divisor \cdot (1 + 3 \cdot MCR[7])}$$

where MODE is 16 for 16XMODE, 8 for 8XMODE and 4 for 4XMODE.

Examples for standard baud rates are given in following chart (using 16XMODE sampling):

Baud Rate MCR[7] = 0	Baud Rate MCR[7] = 1	Divisor	DLM Value	DLL Value	DLD Value	Error (%)
9600	2400	813 12/16	0x03	0x2D	0xC	0.01
19.2k	4800	406 14/16	0x01	0x96	0xE	0.01
115.2k	28.8k	67 13/16	0x00	0x43	0xD	0.01
230.4k	57.6k	33 14/16	0x00	0x21	0xE	0.10
460.8k	115.2k	16 15/16	0x00	0x10	0xF	0.10
500k	125k	15 10/16	0x00	0x0F	0xA	0
750k	187.5	10 6/16	0x00	0x0A	0x6	0.40
921.6k	230.4k	8 7/16	0x00	0x08	0x7	0.47
1000k	250k	7 13/16	0x00	0x07	0xD	0
1250k	312.5k	6 4/16	0x00	0x06	0x4	0
1500k	375k	5 3/16	0x00	0x05	0x3	0.40

Table 6-1 : UART Baud Rate Programming

The achievable baud rate will not always exactly match the desired baud rate (see the "Error" column in the table above). A small error (up to 1%) will not affect the UART function.

To calculate a divisor value for a given baud rate, use following formula:

$$\text{Divisor} = \frac{125MHz}{MODE \cdot Baud\ Rate \cdot (1 + 3 \cdot MCR[7])}$$

where MODE is 16 for 16XMODE, 8 for 8XMODE and 4 for 4XMODE.

These steps should be used to modify the DLM, DLL and DLD registers of an UART channel:

1. Write 0x80 to the LCR register of the UART channel (enable access to the DLM, DLL and DLD registers).

2. Program the DLM, DLL and DLD registers of the UART channel.

3. Write normal operation byte value to the LCR register of the UART channel.

These steps should be used to modify MCR register bit 7 of an UART channel (set baud rate generator prescaler):

1. Set UART channel EFR register bit 4 to '1' (enable modification of MCR register bits 5-7).

2. Modify UART channel MCR register bit 7.

3. Set UART channel EFR register bit 4 to '0' (latch modified MCR register setting).

Note that the maximum baud rate for RS232 channel is 1 Mbps. Thus the minimum divisor value for RS232 channels is 0x0007D with MCR[7] = 0 and 16XMODE sampling.

7 Pin Assignment – I/O Connector

7.1 Front Panel I/O Connector

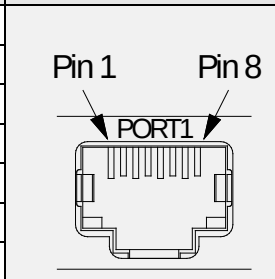
Connector Type		RJ45 modular jack			
Source & Order Info		AMP# 406732-2			
Pin Assignment					
Description RS232		**Pin**	**Connector View**	**Pin**	**Description RS422**
-10R/-12R[1]	**-15R[2]**				**-11R/-12R**
DSR/RI[3]	CD	**1**		**1**	-
CD	RTS	**2**		**2**	-
DTR	GND	**3**		**3**	TxD+
GND	TxD	**4**		**4**	GND
RxD	RxD	**5**		**5**	-
TxD	GND	**6**		**6**	TxD-
CTS	CTS	**7**		**7**	RxD+
RTS	DTR	**8**		**8**	RxD-

Table 7-1 : Pin Assignment Front Panel I/O Connector

7.2 Serial Channel to Front Panel Port Mapping

The serial channels 0-3 are mapped onto the 4 front panel connectors labeled Port1 – Port4.

Serial Channel	Front Panel Port
Serial Channel 0	Port 1
Serial Channel 1	Port 2
Serial Channel 2	Port 3
Serial Channel 3	Port 4

Table 7-2 : Serial Channel to Front Panel Port Mapping

[1] The RS232 pinout is compliant to TIA/EIA-561 (EIA-232D).

[2] The RS232 pinout is compliant to TIP866-TM-20 or to the “Motorola Standard”.

[3] The DSR/RI signal is connected with the DSR and RI transceiver inputs, making both DSR and RI available at the UART. This leaves the choice which signal to use in an application.