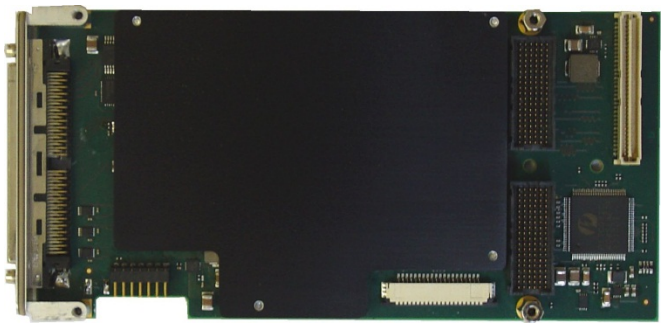
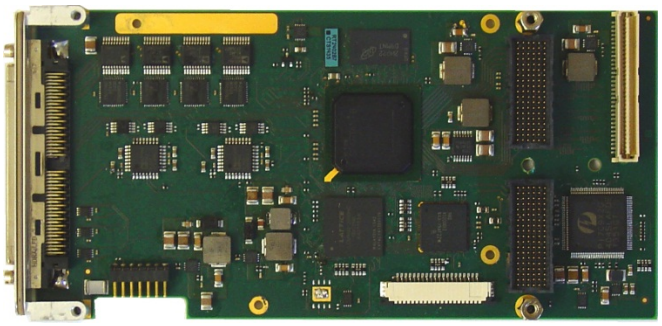
TXMC635 Reconfigurable FPGA with 48 x TTL IO 32 x 16 bit Analog In / 8 x 16 bit Analog Out



TXMC635-10R



TXMC635-10R without heat sink

Application Information

The TXMC635 is a standard single-width Switched Mezzanine Card (XMC) compatible module providing a user configurable XC6SLX45T-2 or XC6SLX100T-2 Xilinx Spartan-6 FPGA.

48 ESD-protected TTL lines provide a flexible digital interface. All I/O lines are individually programmable as input or output. Setting as input sets the I/O line to tri-state and could be used with on-board pull up also as open drain output. Each TTL I/O line has a pull resistor. The pull voltage level is selectable to be either +3.3V, +5V and additionally GND.

8 channels of 16 bit analog outputs allow software selectable output voltage ranges of ±10V, ±10.2564V or ±10.5263V. The output voltage range can be individually set per channel. The conversion time is at most 10 µs and the DAC outputs are routed via operational amplifier in order to protect DAC from damage.

32 ADC input channels can be software configured to operate in single-ended or differential mode with 16 input channels. Each of the 32 channels has a resolution of 16 bit and can work with up to 1 MSPS. The programmable gain amplifier is software configurable and allows a full-scale input voltage range of up to ±24.576V.

For customer specific I/O extension or inter-board communication, the TXMC635-xxR provides 64 FPGA I/Os lines on P14 and 3 FPGA Multi-Gigabit-Transceiver on P16. P14 I/O lines could be configured as 64 single ended LVCMOS33 or as 32 differential LVDS33 interface.

The User FPGA is connected to a 128 Mbytes, 16 bit wide DDR3 SDRAM. The SDRAM-interface uses a hardwired internal Memory Controller Block of the Spartan-6.

The User FPGA is configured by a platform SPI flash or via PCIe download. The flash device is in-system programmable. An in-circuit debugging option is available via a JTAG header for read back and real-time debugging of the FPGA design (using Xilinx “ChipScope”).

The direct configuration via PCIe of the User FPGA is realized by the Configuration FPGA. Configuration data is programmed via 32 bit transfer register to the User FPGA (Spartan6). Data source are XILINX ISE binary files (.bit file or .bin file) which are generated by XILINX ISE Design Software. These binary files consist of header, preamble and configuration data. Only configuration data must be transferred. See also the XILINX User Guide (ug380) “Spartan6 FPGA Configuration” for more information about configuration details and configuration data file formats.

User applications for the TXMC635 with XC6SLX45T-2 FPGA can be developed using the design software ISE Project Navigator (ISE) and Embedded Development Kit (EDK). IDE versions are 14.7. Licenses for both design tools are required.

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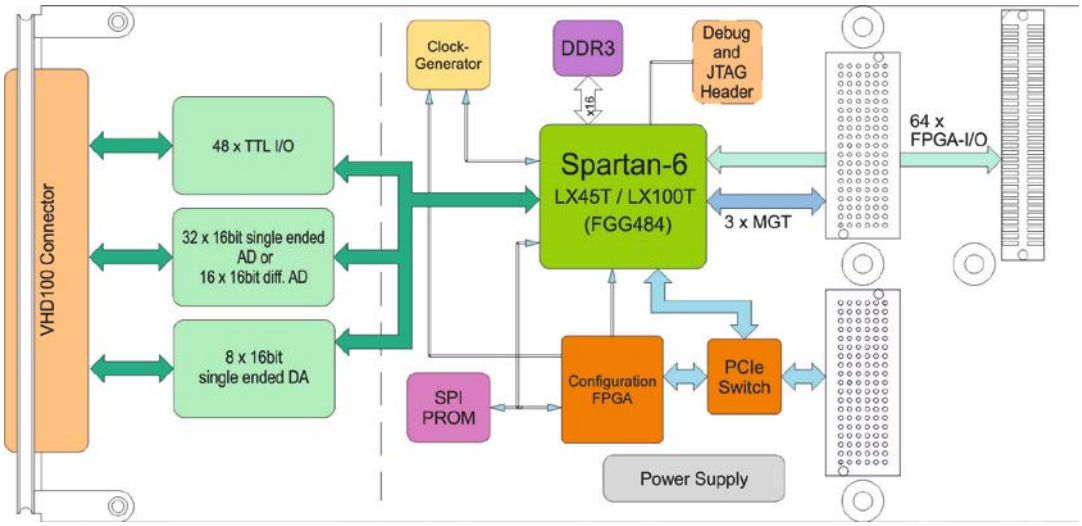
TEWS offers a well-documented basic FPGA Example Application design. It includes an .ucf file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TXMC635.

It implements local bus interface to local bridge device, register mapping, DDR3 memory access and basic I/O. It comes as a Xilinx ISE project with source code and as a ready-to-download bit stream.

Technical Information

- Form Factor: Standard single width XMC
  - Board size: 149 mm x 74 mm
- PCI Express (Base Specification 1.1) compliant interface conforming to ANSI/VITA 42.3-2006
- IPMI resource: FRU hardware definition information stored in on-board EEPROM
- TXMC635-10R Xilinx XC6SLX45T-2 Spartan6 FPGA
- TXMC635-20R Xilinx XC6SLX100T-2 Spartan6 FPGA
- Serial Flash for FPGA Configuration
- FPGA clock options:
  - Local clock generator as source for the FPGA internal PLL
- 1 DDR3 SDRAM bank, 64M x 16 (128 MB)
- Front I/O lines
  - 48 TTL I/O
    TTL signaling voltage (maximum current: +/-32mA) direction individually programmable
  - 8 channels single-ended 16 bit analog output
    - Programmable output voltage: ±10V, ±10.2564V or ±10.5263V
    - Conversion time: typ.10µs
    - Factory calibration
  - 32 single ended or 16 differential analog inputs
    - 16 bit resolution
    - Conversion time: 1.1µs
    - User programmable input voltage range
    - Factory calibration
- Back I/O lines
  - 64 single ended or 32 differential back I/O lines on rear connector P14.
  - 3 FPGA Multi-Gigabit-Transceiver on rear connector P16
- Operating temperature -40°C to +85°C
- MTBF (MIL-HDBK217F/FN2 G_B 20°C): tbd.



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Order Information

RoHS Compliant

TXMC635-10R	Spartan-6 FPGA XC6SLX45T-2,128 MB DDR3	48 TTL Front I/O, 32x 16bit AD, 8 x 16 bit DA 64 direct FPGA I/O on P14, 3 MGTs on P16
TXMC635-20R	Spartan-6 FPGA XC6SLX100T-2,128 MB DDR3	48 TTL Front I/O, 32x 16bit AD, 8 x 16 bit DA 64 direct FPGA I/O on P14, 3 MGTs on P16

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation

TXMC635-DOC User Manual

Software

TDRV018-SW-25	Integrity Software Support
TDRV018-SW-42	VxWorks Software Support (Legacy and VxBus-Enabled Software Support)
TDRV018-SW-65	Windows Software Support
TDRV018-SW-82	Linux Software Support
TDRV018-SW-95	QNX Software Support

For other operating systems please contact TEWS.

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