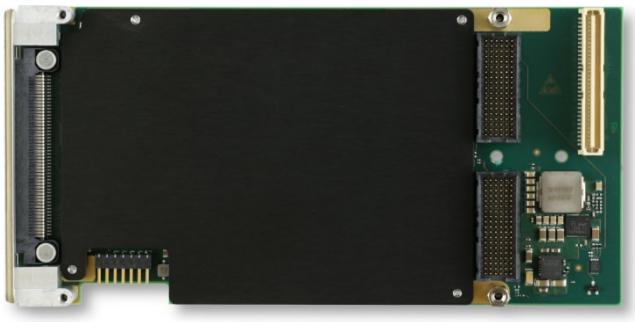
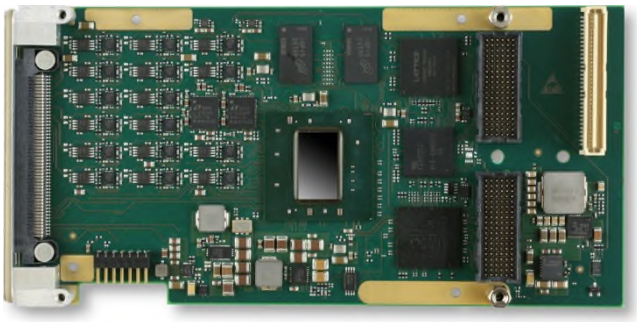
TXMC639 Reconfigurable FPGA with 16 x 16 bit Analog Input 8 x 16 bit Analog Output and 32 digital I/O



TXMC639-11R



TXMC639-11R without heat sink

Application Information

The TXMC639 is a standard single-width Switched Mezzanine Card (XMC) compatible module providing a user configurable FPAG (AMD Kintex™ 7) with up to 16 differential ADC input channels and up to 8 single ended DAC output channels.

The TXMC639 ADC input channels are based on the Octal 16-Bit 1.5Msps Differential LTC2320-16 ADC. The TXMC639-11R provides 16, the TXMC639-10R 8 ADC channels. Each channel has a resolution of 16 bit and can operate at up to 1.5 Msps. The analog input circuit is designed to configurable differential input voltages ranges of ±20.57 V, ±10.28 V or ±5.14 V.

The TXMC639 DAC output channels are based on the Dual 16bit AD5547 DAC. The TXMC639-11R provides 8, the TXMC639-10R 4 DAC channels. Each DAC output is designed as a configurable single-ended bipolar analog output. Output voltage is configurable as ±10.0 V, ±5.0 V or ±2.5 V.

32 ESD-protected TTL lines provide a flexible digital interface. All I/O lines are individually programmable either as input or output. Input I/O lines are tri-stated and could be used with the on-board pull up or as tri-stated output. Each TTL I/O line has a pull resistor sourced by a common pull voltage. The pull voltage level is selectable to be either +3.3 V, +5.0 V or GND.

16 of these ESD-protected TTL lines can be switched between TTL interface and RS422 interface. Switching is done via the Board Configuration Controller (BCC). All 8 RS422 transceivers have individual internal switchable terminations.

For customer specific I/O extension or inter-board communication, the TXMC639 provides 64 FPGA I/Os on P14 and 4 FPGA Multi-Gigabit-Transceiver on P16. P14 I/O lines can be configured as 64 single ended LVCMOS25 or as 32 differential LVDS25 interface in accordance with TEWS CMC modules.

The User FPGA is connected to a 1GB, 32 bit wide DDR3L SDRAM. The SDRAM-interface uses an internal Memory Controller and is routed to a HP bank of User FPGA Kintex™ 7.

The TXMC639 is delivered with an FPGA Board Reference Design (BRD). This is the standard content of the serial configuration SPI flash, and is loaded into the user FPGA by default after power up. The User FPGA can also be configured via the on-board Board Configuration Controller (BCC) or via JTAG interface using a AMD programmer. For full PCIe specification compliance the AMD Tandem Configuration Feature is supported. The SPI flash device is in-system programmable. Also an in-circuit debugging option is available via a JTAG header for real-time debugging of the User FPGA design.

User applications for the TXMC639 with Kintex™ 7 FPGA can be developed using the design software Vivado Design Suite. A full (non-webpack) license for the Vivado Design Suite design tool is required, due to FPGA density.

Technical Information

Issue 1.0.2
2024-02-09

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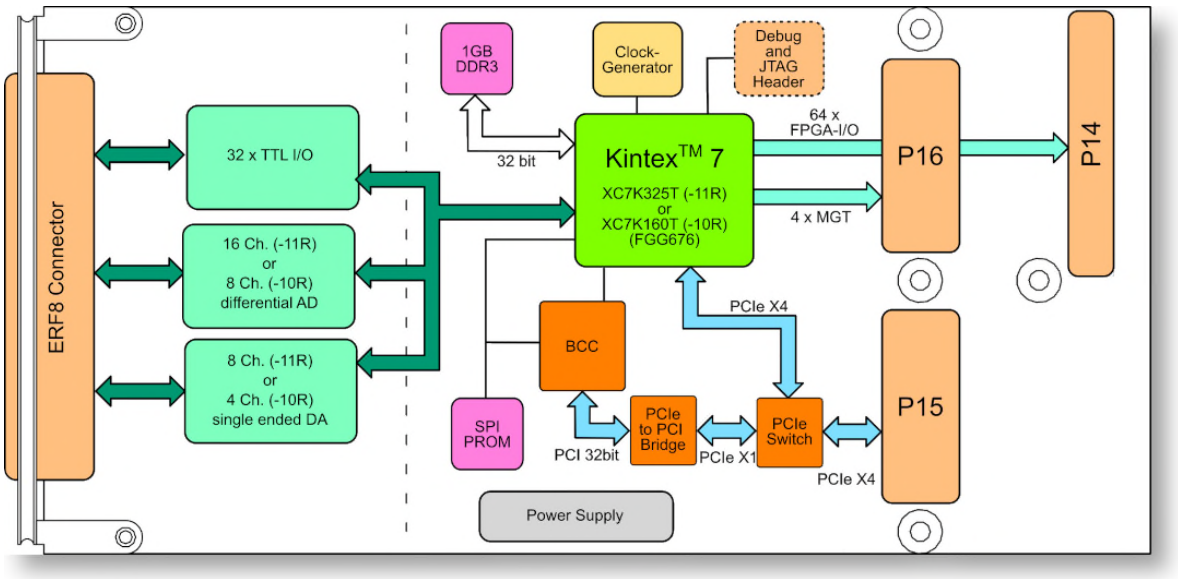
- Form Factor: Standard single width XMC
  - Board size: 149 mm x 74 mm
- PCI Express (Base Specification 2.1) compliant interface conforming to ANSI/VITA 42.3-2006
- IPMI resource: FRU hardware definition information stored in on-board EEPROM
- TXMC639 FPGA options:
  - -10R AMD XC7K160T-2FBG676I Kintex™ 7
  - -11R AMD XC7K325T-2FBG676I Kintex™ 7
- Serial Flash for FPGA Configuration
- FPGA clock options:
  - Local clock generator as source for the FPGA internal PLL
- Analog Front A/D lines
  - Up to 16 Differential 16bit A/D Channels
    - 16 bit resolution
    - Differental :
    - ±20.57 V, ±10.28 V or ±5.14 V
    - Single-Ended:
    - ±10.28 V, ±5.14 V or ±2.57
    - Up to 1.5Msps
    - Correction values for gain / offset error
- Analog Front D/A lines
  - Up to 8 channels single-ended analog output
    - 16 bit resolution
    - Programmable output voltage ranges: ±10V, ±5.0 V or ±2.5 V
    - Full scale settling time: typ.1 µs
    - Correction values for gain / offset error
- Digital Front I/O Lines
  - 32 digital TTL compatible I/O lines
  - 16 lines optional programmable as differential RS422 interface
- DDR3 SDRAM bank, 256M x 32 Bit (1GB)
- P14/P16 Rear I/O lines
  - 64 single ended or 32 differential rear I/O lines on a rear XMC 64pin P14 connector
  - 4 FPGA Multi-Gigabit-Transceiver on a rear XMC P16 connector.
- Operating temperature -40°C to +85°C
- MTBF (MIL-HDBK217F/FN2 GB 20°C): 157000h



Block Diagram TXMC639

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Order Information

RoHS Compliant

TXMC639-10R	XC7K160T-2FBG676 Kintex™ 7 FPGA, 1GB DDR3	8 x Analog In, 4 x Analog Out, 32 digital Front I/O, 64 direct FPGA Rear I/O Lines and 4 MGTs Rear I/O
TXMC639-11R	XC7K325T-2FBG676 Kintex™ 7 FPGA, 1GB DDR3	16 x Analog In, 8 x Analog Out, 32 digital Front I/O, 64 direct FPGA Rear I/O Lines and 4 MGTs Rear I/O

Software

TDRV018-SW-25	Integrity Software Support
TDRV018-SW-42	VxWorks Software Support (Legacy and VxBus-Enabled Software Support)
TDRV018-SW-65	Windows Software Support
TDRV018-SW-82	Linux Software Support
TDRV018-SW-95	QNX Software Support

For other operating systems please contact TEWS.

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