The Embedded I/O Company

TEWS TECHNOLOGIES

TXMC639

Reconfigurable FPGA with 16 x 16 bit Analog Input, 8 x 16 bit Analog Output and 32 digital I/O

Version 1.0

User Manual

Issue 1.0.2

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TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

TXMC639-10R

8 x Analog In, 4 x Analog Out, 32 TTL (with 16 differential-selectable) Front I/O and 64 direct rear FPGA I/O Lines,

XC7K160T-2FBG676 Kintex™ 7 FPGA, 1GB DDR3

TXMC639-11R

16 x Analog In, 8 x Analog Out, 32 TTL (with 16 differential-selectable) Front I/O and 64 direct rear FPGA I/O Lines,

XC7K325T-2FBG676 Kintex™ 7 FPGA, 1GB DDR3

Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

W	Write Only
R	Read Only
R/W	Read/Write
R/C	Read/Clear
R/S	Read/Set

Issue	Description	Date
1.0.0	First Issue	May 2023
1.0.1	Reduction of the ADC digital output coding values to 2 decimal places for better adaptation to the 16 bit correction values.	September 2023
1.0.2	General Revision	January 2024

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1 Product Description

The TXMC639 is a standard single-width Switched Mezzanine Card (XMC) compatible module providing a user configurable Kintex™ 7 with (up to) 16 differential ADC input channels and (up to) 8 single ended DAC output channels.

The TXMC639 ADC input channels are based on the Linear Octal 16 bit 1.5Msps Differential LTC2320-16 ADC. Each ADC channel has a resolution of 16 bit and can operate at up to 1.5 Msps. The analog input circuit is designed to allow configurable differential input voltages ranges of ±20.56 V, ±10.28 V or ±5.14 V.

The TXMC639 DAC output channels are based on the Dual 16bit AD5547 DAC. Each DAC output is designed as a configurable single-ended bipolar analog output. Output voltage is configurable as Single Ended ±10.0 V, ±5.0 V or ±2.5 V.

32 ESD-protected TTL lines provide a flexible digital interface. All I/O lines are individually programmable either as input or output. Input I/O lines are tri-stated and could be used with the on-board pull up or as tri-stated output. Each TTL I/O line has a pull resistor sourced by a common pull voltage. The pull voltage level is selectable to be either +3.3 V, +5 V and additionally GND.

16 of these ESD-protected TTL lines can be switched between TTL interface and RS422 interface. Switching is done via BCC. All 8 RS422 transceivers have individual internal switchable terminations.

For customer specific I/O extension or inter-board communication, the TXMC639 provides 64 FPGA I/Os on P14 and 4 FPGA Multi-Gigabit-Transceiver on P16. P14 I/O lines can be configured as 64 single ended LVCMOS25 or as 32 differential LVDS25 interface in accordance with TEWS CMC modules.

The User FPGA is connected to a 1GB, 32 bit wide DDR3L SDRAM. The SDRAM-interface uses an internal Memory Controller and is routed to HP bank of User FPGA Kintex™ 7.

The User FPGA is configured by a serial SPI flash. For full PCIe specification compliance (irrespective of the actual design complexity), the AMD Tandem Configuration Feature has to be used for FPGA configuration. AMD Tandem Methodologies “Tandem PROM” should be the favored Methodology. The SPI flash device is in-system programmable. An in-circuit debugging option is available via a JTAG header for real-time debugging of the FPGA design.

User applications for the TXMC639 with Kintex™ 7 FPGA can be developed using the design software Vivado Design Suite. A full (non-webpack) license for the Vivado Design Suite design tool is required, due to FPGA density.

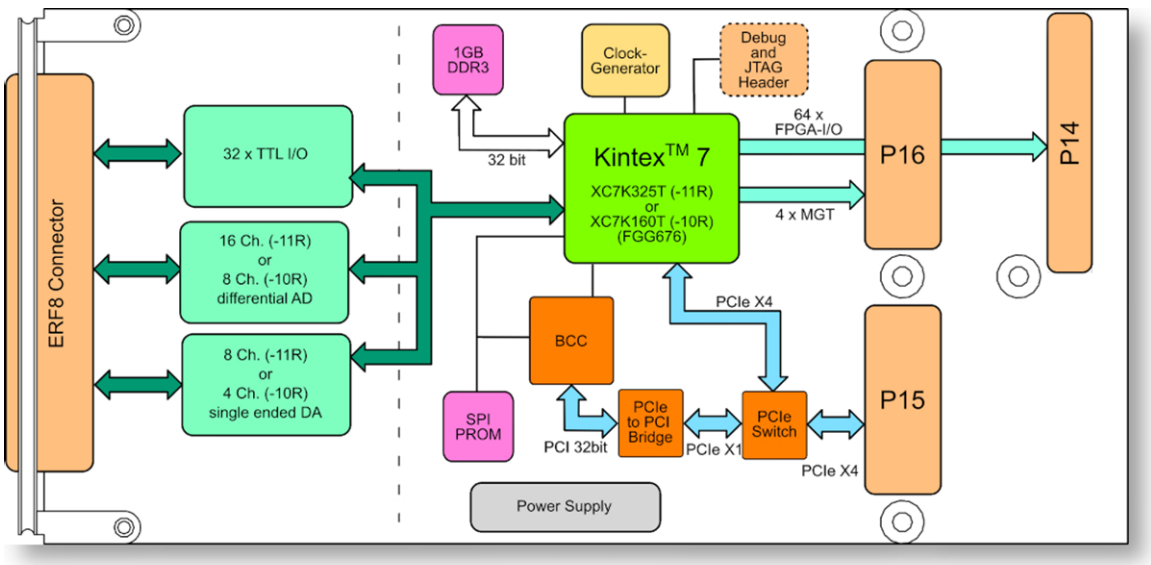


Figure 1 1: Block Diagram TXMC639-11R

2 Technical Specification

PCIe Interface		
Mechanical Interface	Switched Mezzanine Card (XMC) Interface confirming to ANSI/VITA 42.0-2008 (Auxiliary Standard) Standard single-width (149mm x 74mm)	
Electrical Interface	PCI Express x4 Link (Base Specification 2.1) compliant interface conforming to ANSI/VITA 42.3-2006 (PCI Express Protocol Layer Standard)	
On-Board Devices		
PCI Express Switch	PI7C9X2G312GP (Pericom)	
PCI Express to PCI Bridge	XIO2001 (Texas Instruments)	
User configurable FPGA	TXMC639-10R: XC7K160T-2FBG676I (AMD) TXMC639-11R: XC7K325T-2FBG676I (AMD)	
SPI-Flash	MT25QL128 (Micron) 128 Mbit (contains TXMC639 FPGA BRD) or compatible; +3.3 V supply voltage	
DDR3 RAM	MT41K256M16TW-107 (Micron)	
Board Configuration Controller	LCMXO2-7000HC (Lattice)	
ADC	LTC2320-16 (Analog Devices)	
DAC	AD5547BRUZ (Analog Devices)	
I/O Interface		
A/D Channels	TXMC639-10: 8 Differential 16 bit A/D Channels TXMC639-11: 16 Differential 16 bit A/D Channels Input Configuration per BCC Device: Input Voltage Ranges: Differental : ±20.56 V, ±10.28 V or ±5.14 V (Single-Ended: ±10.28 V, ±5.14 V or ±2.57 V) All analog inputs are connected via an impedance converter and a second operation amplifier for level adjustment and filtering to the differential ADC inputs. The -3 dB limit of this input stage is at approx. 8MHz	
D/A Channels	TXMC639-10: 4 Single-Ended 16 bit D/A Channels TXMC639-11: 8 Single-Ended 16 bit D/A Channels Output Configuration per BCC Device: Single-Ended Output Voltage Ranges: ±10 V, ±5.0 V, ±2.5 V, Output range configurable per D/A channel. Simultaneous Conversion for all D/A Channels.	
	Maximum single-ended Output Voltage – Vout Maximum Output Drive Current for each Output Maximum Capacitive Load for each Output Typical Settling Time for a 10 mA / 1000 pF	±10 V 10 mA 1000 pF < 1 µs
Digital Front I/O Channels	32 digital I/O Lines • Default configured as 32 48 ESD-protected TTL lines • 16 I/O lines are configurable as 8 differential RS422 I/O lines with individual Termination enable.	

<table>
<tr><td>Digital Rear I/O Channels</td><td>64 direct FPGA I/O lines to P14 Rear I/O connector
Can be used as single-ended or differential I/O
FPGA I/O Standard: LVCMOS25, LVTTL25 and LVDS25
4 MGT line to P16 Rear I/O connector
Each line consists of one differential RX and TX pair.
Transmission speeds of up to 3.125 Gb/s are possible.</td></tr>
<tr><td colspan="2">I/O Connector</td></tr>
<tr><td>Front I/O</td><td>Front I/O Samtec - ERF8_050_01_L_D_RA_L_TR</td></tr>
<tr><td>P14 Rear I/O</td><td>64 pin Mezzanine Connector (Molex 71436-2864 or compatible)</td></tr>
<tr><td>P16 Rear I/O</td><td>114 pin Mezzanine Connector (Samtec – ASP-105885-01)</td></tr>
<tr><td colspan="2">Physical Data</td></tr>
<tr><td>Power Requirements</td><td>Depends on FPGA design
With TXMC639 Board Reference Design / without external load<table><tr><td></td><td>typical @ +12 V VPWR</td><td>typical @ +5 V VPWR</td></tr><tr><td>TXMC639-10R</td><td>1.1 A</td><td>2.5 A</td></tr><tr><td>TXMC639-11R</td><td>1.3 A</td><td>3.3 A</td></tr></table></td></tr>
<tr><td>Temperature Range</td><td>Operating -40°C to +85°C
Storage -40°C to +85°C</td></tr>
<tr><td>MTBF</td><td>TXMC639-10R: 161000 h
TXMC639-11R: 157000 h
MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: G_B 20°C.
The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation.</td></tr>
<tr><td>Humidity</td><td>5 – 95 % non-condensing</td></tr>
<tr><td>Weight</td><td>TXMC639-xx: 140 g</td></tr>
</table>

Table 2-1 : Technical Specification

3 Handling and Operation Instruction

3.1 ESD Protection

The TXMC639 is sensitive to static electricity. Packing, unpacking and all other handling of the TXMC639 has to be done in an ESD/EOS protected Area.

3.2 Thermal Considerations

Forced air cooling is required during operation. Without forced air cooling, damage to the device can occur.

Please also note chapter “Thermal Management”.

4 PCI Device Topology

The TXMC639 consists of two FPGAs. Both FPGAs are designed as PCIe / PCI endpoint devices. One FPGA is the User FPGA (Kintex™ 7) which can be programmed with user defined FPGA code. The second FPGA takes control of on-board hardware functions of TXMC639 and also the configuration control of the User FPGA. This second FPGA is the BCC (Board Configuration Controller).

The BCC PCI endpoint is connected via a PCI-to-PCIe Bridge to the second x1 Downstream Port of the PCIe Switch (Pericom PI7C9X2G312GP). The User FPGA (Kintex™ 7 PCIe endpoint) is directly connected to the first x4 Downstream Port.

The x4 Upstream Port of the PCIe Switch is connected to the XMC P15 Connector, communicating with the host system.

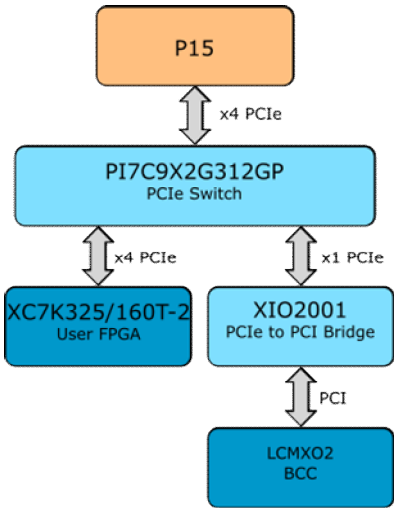


Figure 4-1 : PCIe/PCI Device Topology

Device	Vendor ID	Device ID	Class Code	Description (as shown by lspci)
PI7C9X2G312GP	0x12D8 (Pericom)	0x2312	0x060400	PCIe Switch: 0x04h to indicate device as PCI-to-PCI Bridge 0x06h to indicate device as Bridge device
XIO2001	0x104C (Texas Instruments)	0x8240	0x060400	PCI bridge: Texas Instruments 0x04h to indicate device as PCI-to-PCI Bridge 0x06h to indicate device as Bridge device
XC7A160T-2 / XC7A325T-2	user defined			Device identification for the User programmable FPGA is defined by user. The data will be created with the AMD Vivado “7 Series Integrated Block for PCI Express” IP generator.
BCC LCMXO2	0x1498 (TEWS)	0x927F	0x068000	Bridge Device: TEWS Technologies GmbH Device 927F (TXMC639).

Table 4-1 : On-Board PCIe / PCI Devices

4.1 User FPGA (Kintex™ 7)

The User FPGA address map depends on the user application and is not part of this manual.

4.2 BCC (Board Configuration Controller) FPGA

4.2.1 PCI Configuration Registers (PCR)

PCI CFG Register Address	Write '0' to all unused (Reserved) bits				PCI writeable	Initial Values (Hex Values)
	31 24	23 16	15 8	7 0		
0x00	Device ID		Vendor ID		N	927F 1498
0x04	Status		Command		Y	0480 000B
0x08	Class Code			Revision ID	N	068000 01
0x0C	BIST	Header Type	PCI Latency Timer	Cache Line Size	Y[7:0]	00 00 00 08
0x10	PCI Base Address 0 for Local Address Space 0				Y	FFFFFF00
0x14	PCI Base Address 1 for Local Address Space 1				Y	FFFFFF00
0x18	PCI Base Address 2 for Local Address Space 2				N	00000000
0x1C	PCI Base Address 3 for Local Address Space 3				N	00000000
0x20	PCI Base Address 4 for Local Address Space 4				N	00000000
0x24	PCI Base Address 5 for Local Address Space 5				N	00000000
0x28	PCI CardBus Information Structure Pointer				N	00000000
0x2C	Subsystem ID		Subsystem Vendor ID		N	927F 1498
0x30	PCI Base Address for Local Expansion ROM				Y	00000000
0x34	Reserved			New Cap. Ptr.	N	000000 40
0x38	Reserved				N	00000000
0x3C	Max_Lat	Min_Gnt	Interrupt Pin	Interrupt Line	Y[7:0]	00 00 01 00

Table 4-2 : PCI Configuration Registers

4.2.2 PCI BAR Overview

BAR	Size (Byte)	Space	Prefetch	Port Width (it)	Endian Mode	Description
0	256	MEM	No	32	Little	Local Configuration Register Space
1	256	MEM	No	32	Little	In-System Programming Data Space

Table 4-3 : PCI BAR Overview

4.2.2.1 Local Configuration Register Space

Offset to PCI Base Address	Register Name	Size (bit)
0x00	DAC Control and Status Register	32
0x04	DAC Output Voltage Range Register	32
0x08	ADC Input Voltage Range Register	32
0x0C – 0x0F	Reserved	-
0x10 – 0x2C	Register for VOFF and VREF of DAC Channel 1 to 8	8 x 32
0x30 – 0x5F	Reserved	-
0x60	Digital I/O Interface Configuration /Status Register	32
0x64	TXMC639 I/O Area Temperature	32
0x68 – 0x7F	Reserved	-
0x80	Kintex™ 7 JTAG Control Register	32
0x84	Kintex™ 7 JTAG Interface Register	32
0x88	Kintex™ 7 JTAG Signal TMS Data Register	32
0x8C	Kintex™ 7 JTAG Signal TDI Data Register	32
0x90	Kintex™ 7 JTAG Signal TDO Data Register	32
0x94 – 0x9F	Reserved	-
0xA0	I2C Bridge Register	32
0xA4 – 0xBF	Reserved	
0xC0	Interrupt Enable Register	32
0xC4	Interrupt Status Register	32
0xC8	Reserved	-
0xCC	Reserved	-
0xD0	User FPGA Configuration Control/Status Register	32
0xD4	User FPGA Configuration Data Register (Slave SelectMAP)	32
0xD8	Reserved	-
0xDC	Reserved	-
0xE0	ISP Control Register (SPI)	32
0xE4	ISP Configuration Register (SPI)	32
0xE8	ISP Command Register (SPI)	32
0xEC	ISP Status Register (SPI)	32
0xF0	Reserved	-
0xF4	TXMC639 Board Temperature	32
0xF8	TXMC639 Serial Number	32
0xFC	Firmware Version Register	32

Table 4-4 : Local Configuration Register Space

4.2.2.2 In-System Programming Data Space

The In-System Programming (ISP) Data Space is used for passing user FPGA configuration data for in-system programming of the User FPGA SPI Flash.

For ISP write/program instructions, the data must be written (zero-based) to the ISP Data Space before the instruction is started. The data must cover a complete SPI Flash memory page.

For ISP read instructions, the data can be read (zero-based) from the ISP Data Space after the instruction is done. The data is passed for a complete SPI Flash memory page.

The ISP Data Space size is 256byte, covering an SPI Flash Memory Page. All supported SPI Flash read and write instructions are page-based.

Control and status register for ISP are located in the Local Configuration Register Space. The data register for direct FPGA ISP is also located in the Local Configuration Register Space.

5 Register Description

5.1 User FPGA (Kintex™ 7)

The FPGA register description depends on the user application and is not part of this manual.

5.2 BCC (Board Configuration Controller) FPGA

5.2.1 DAC and ADC Control / Status Register – 0x00

The output voltage and input voltage ranges of the TXMC639 DAC outputs are set via *DAC and ADC Control / Status Register, DAC Output Voltage Range Register and ADC Input Voltage Range Register*.

For the three predefined DAC voltage ranges, the *DAC Output Voltage Range Register* is set first and then the values are transferred via the *DAC and ADC Control / Status Register*.

For the individual range selection the *Reference DAC Voltage Control Register* must also be set before updating the data via *DAC and ADC Control / Status Register*.

For the three ADC voltage ranges the *ADC Input Voltage Range Register* is set first and then the values are transferred via the *DAC and ADC Control / Status Register.*

Bit	Symbol	Description	Access	Reset Value
31:24	-	Reserved	R	0
23:22	-	Reserved	R	0
21	ADC_REF_OUTP_UPD	ADC Reference Output Update Initiate DAC Device Output Update with currently adjusted output voltage configuration Self-Clearing	R/S	0
20	ADC_REF_CLR	ADC Reference Clear Performs an asynchronous clear on the DAC device, including post-reset/power-on setup with currently adjusted output voltage configuration *Fundamental Device Reset* ***Shared/Performed with DAC Reference Clear (DAC_REF_CLR)***	R	0
19	ADC_REF_OVRTMP	ADC Reference Over Temperature Status information by provided by DAC device. Reset/cleared by an output update operation.	R	0
18	-	Reserved	-	0
17	ADC_REF _OUTPSTTLE	ADC Reference Output Settle Internal generated settling pulse (set to 20.5us)	R	0
16	ADC_REF_IOBSY	ADC Reference I/O Busy Indicates that • Controller is not in idle • Span-Configuration update is pending • Output Value update is pending Internal synchronization is pending	R	0
15:8	-	Reserved	R	0
7:6	-	Reserved	R	0
5	DAC_REF_OUTP_UPD	DAC Reference Output Update	R/S	0

		Initiate DAC Device Output Update with currently adjusted output voltage configuration Self-Clearing		
4	DAC_REF_CLR	DAC Reference Clear Performs an asynchronous clear on the DAC device, including post-reset/power-on setup with currently adjusted output voltage configuration *Fundamental Device Reset* ***Includes ADC Reference Clear*** Self-Clearing	R/S	0
3	DAC_REF_OVRTMP	DAC Reference Over Temperature Status information by provided by DAC device. Reset/cleared by an output update operation.	R	0
2	-	Reserved	-	0
1	DAC_REF_OUTPSTTLE	DAC Reference Output Settle Internal generated settling pulse (set to 20.5us)	R	0
0	DAC_REF_IOBSY	DAC Reference I/O Busy Indicates that • Controller is not in idle • Span-Configuration update is pending • Output Value update is pending • Internal synchronization is pending	R	0

Table 5-1 : DAC Control and Status Register

5.2.2 DAC Output Voltage Range Register – 0x04

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved	-	00
15:14	DAC_REF7	DAC Output Voltage range selection for DAC channel 7 00 : ±10 V range (default value) 01 : ±5 V range 10 : ±2.5 V range 11 : individual range selection	R/W	0b00
…	-	…	…	…
1:0	DAC_REF0	DAC Output Voltage range selection for DAC channel 0 00 : ±10 V range - (default value) 01 : ±5 V range 10 : ±2.5 V range 11 : individual range selection	R/W	0b00

Table 5-2 : DAC Output Voltage Range Register

For individual voltage range selection also see the chapter *5.2.4Reference DAC Voltage Control Register.*

5.2.3 ADC Input Voltage Range Register – 0x08

Bit	Symbol	Description	Access	Reset Value
31:16	-	Reserved	-	00
15:14	ADC_REF7	ADC Input Voltage range selection for ADC channel 14+15 00 : ±20.56 V diff. - (default value) 01 : ±10.28 V diff. 10 : ±5.14 V diff. 11 : not used	R/W	0b00
…	-	…	…	…
1:0	ADC_REF0	ADC Input Voltage range selection for ADC channel 0+1 00 : ±20.56 V diff. - (default value) 01 : ±10.28 V diff. 10 : ±5.14 V diff. 11 : not used	R/W	0b00

Table 5-3 : ADC Input Voltage Range Register

5.2.4 Reference DAC Voltage Control Register – 0x10 to 0x4C

The 8 TXMC639 DAC outputs consist of four dual DAC devices (AD5547). Each of these DACs could be used independently.

For the generation of the DAC reference voltage, an additional serial DAC device is placed on the TXMC639. This Reference DAC has 16 analog outputs. Two reference voltages for each TXMC639 DAC output.

Via these reference voltages (VREF and VOFF), an individual voltage range can be set for each TXMC639 DAC channel. Both reference voltages are each set as 16 bit value via a 32 bit register of the BCC. This results in 8 32 bit registers via which the reference voltage and thus the output voltage range of the TXMC639 can be configured.

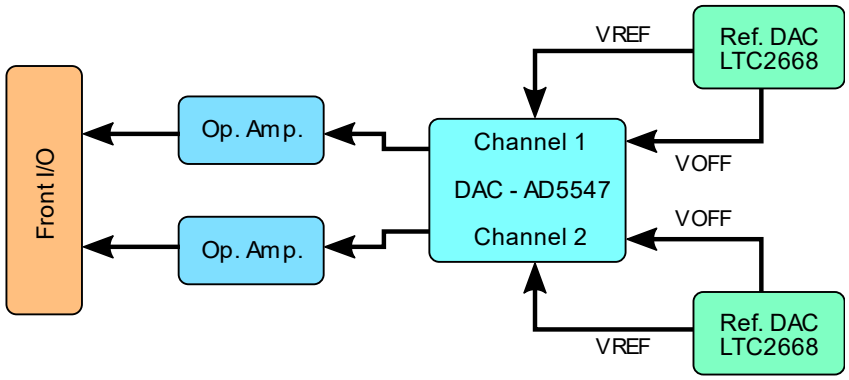


Figure 5-1 : DAC and Ref. DAC Schemata

One 32 bit Register for each of the 8 TXMC639 DAC outputs.

Bit	Symbol	Description	Access	Reset Value
31:16	VREF	16 bit Data Value for VREF which specifies the half voltage swing of the reference voltage for the AD5547 DAC channel.	R/W	0x8000
15:0	VOFF	16 bit Data Value for VOFF which represents the negative reference voltage of the AD5547 DAC channel.	R/W	0x8000

Table 5-4 : Reference DAC Voltage Control Register

Each TXMC639 analog output consists of a half AD5547 output DAC, an operational amplifier driving the output load, and two references DAC outputs each for VREF and VOFF.

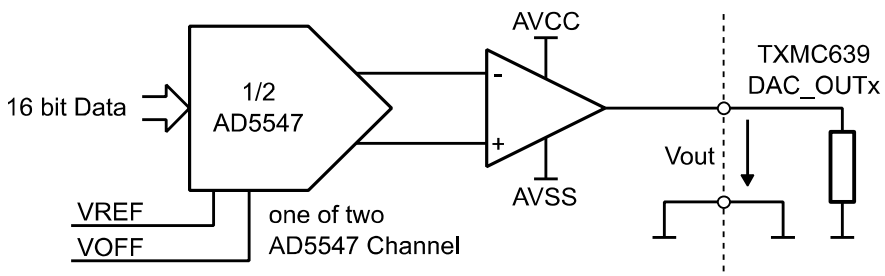


Figure 5-2 : DAC Output Channel

The following table shows the data coding for VREF and VOFF output voltage range.

Description	Digital Code
+9.9997 V	0xFFFF
+5.0 V	0xC000
+2.5 V	0xA000
0 V	0x8000
-2.5 V	0x6000
-5.0 V	0x4000
-10.0 V	0x0000

Table 5-5 : Voltage coding for the Reference DAC

The output voltage range is then calculated with these two reference values (VREF and VOFF) as follows:

Vrange_high = -1 * VOFF

Vrange_low = -1 * VOFF - 2 * VREF

See the following Examples for:

VOFF	VREF	Vrange_low	Vrange_high	Voltage Range	Note
+10 V (0xFFFF)	-10 V (0x0000)	-10 V	+10 V	-10 V … +10 V	typical range
+5 V (0xC000)	-5 V (0x4000)	-5 V	+5 V	-5 V … +5 V	typical range
+1.25 V (0x2000)	-5 V (0x4000)	-1.25 V	+8.75 V	-1.25 V … +8.75 V	asymmetric range
-5 V (0x4000)	+5 V (0xC000)	+5 V	-5 V	+5 V … -5 V	changes sign

Thus, any desired output voltage can be generated. But in any case it is important to ensure that the voltages VOUT and VREF are never set above +10 V or below -10 V. Voltages above these limits cannot be generated and lead to incorrect outputs.

5.2.5 Digital I/O Interface Configuration /Status Register - 0x60

Bit	Symbol	Description	Access	Reset Value
31:18	-	Reserved	-	0
17	IO_MUX_FLT	Multiplexer Fault Indicaton 0: device is operational 1: fault condition signaled *Fault assertion is captured (registered) to ensure detection of short-term events*	R/C	0
16	IO_MUX_OE	Multiplexer Output Enable Controls all multiplexed digital IO Lines in common. It is strongly recommended to enable the Multiplexer Outputs only after correct MUX configuration. 0: disable all multiplexed digital IO Lines 1: enable all multiplexed digital IO Lines	R/W	0
15	IO_MUX_SEL7	Digital Front I/O Line Multiplexer Selection. 1: corresponding I/O lines 16..31 are TTL 0: corresponding I/O lines 16..31 are RS422 SEL0 = I/O lines 16/17 SEL1 = I/O lines 18/19 SEL2 = I/O lines 20/21 SEL3 = I/O lines 22/23 SEL4 = I/O lines 24/25 SEL5 = I/O lines 26/27 SEL6 = I/O lines 28/29 SEL7 = I/O lines 30/31	R/W	0xFF
14	IO_MUX_SEL6			
13	IO_MUX_SEL5			
12	IO_MUX_SEL4			
11	IO_MUX_SEL3			
10	IO_MUX_SEL2			
9	IO_MUX_SEL1			
8	IO_MUX_SEL0			
7:5	-	Reserved	-	0
4	PULL_SRC_SEL	I/O Group Pull Source Selection Defines whether the BCC or the User FPGA controls the I/O Group Pull Selection. 0: BCC 1: User FPGA	R/W	0
3:2	PULL_G1	TTL I/O Group Pull Selection Value is only effective if the register PULL_SRC_SEL is set to BCC controlling. 11 : pull-down 10 : pull-up to 3.3 V 01 : pull-up to 5 V 00 : No pull I/O lines are summarized in the following groups. G0 = I/O_0 … I/O_15 G1 = I/O_16 … I/O_31	R/W	0x0
1:0	PULL_G0			

Table 5-6 : I/O Pull-Resistor Configuration Register

Each TTL I/O Line has a 4k7 Pull-Resistor. The 32 I/O Lines are divided into two groups (G0, G1) which can be configured as 3.3 V pull-up, 5 V pull-up or pull-down. In addition, the Pull-Resistors can float.

If the Pull-Resistors float, the user should keep in mind that the 16 I/O Lines of a group are connected via their Pull-Resistors.

The default adjustment is that the BCC control the I/O Pull Configuration.

5.2.6 TXMC639 I/O Area Temperature Sensor Register - 0x64

Bit	Symbol	Description	Access	Reset Value
31:21	-	Reserved	r	-
20	TMP441_AUTO _TRD_EN	TMP441 Automatic Temperature Read Enable Controls the periodic board temperature read feature. Refresh time = 1 s ‘0’ = disabled ‘1’ = enabled *Automatic mode must be disabled before enabling the I2C bridge mode*	R/W	1
19:16	-	Reserved		0
15:8	TMP441_TEMP	TMP441 Temperature Data Measured data of the I/O area temperature sensor The read value of the temperature sensor is stored sign-extended as a 8 bit two's complement. To actually calculate the temperature from the two's complement data value, use the following formula: Temperature (°C) = TEMP	R	-
7:0	-	Reserved	-	-

Table 5-7 : TXMC639 I/O Area Temperature Sensor Register

5.2.1 User FPGA JTAG Control and Status Register – 0x80

Bit	Symbol	Description		Access	Reset Value
31:10	-	Reserved		-	00
9:8	JTAG_VIO_CTRL_STAT	JTAG Vector-I/O Controller Status Signals the status of the Vector I/O controller. 0b00 = Controller disabled 0b01 = Controller idle (ready-for-request) 0b10 = Ongoing Vector I/O controller operation 0b11 = illegal *Initiate JTAG operations only if the Vector I/O controller is in idle state.*		r	01
7:5	-	Reserved		-	0
4	JTAG_EXT#_INT	JTAG External/Internal Indicates whether a JTAG device is detected/present at the Debug Connector or not. 0b0 = Device detected/present 0b1 = No device detected *Detection is based on the Debug Connector Present signal*		r	-
3	-	Reserved		-	0
2:0	JTAG_MUX	BCC controlled JTAG Multiplexer to USER FPGA		r/w	0b000
		0b000	Fix priority. Which JTAG connection is active depends on the inserted cable. *The priority is as follows:* *1) Debug Connector* *2) USB JTAG* *3) BCC JTAG (V-I/O or B-I/O)*		
		0b001	Hardwired JTAG interface from Debug Connector to Kintex™ 7 is active.		
		0b010	reserved		
		0b100	BCC internal JTAG Controller is connected to Kintex™ 7.		

Table 5-8 : User FPGA JTAG Control and Status Register

5.2.2 User FPGA JTAG Signal Line Register – 0x84

Refer to the chapter JTAG Controller to K7 JTAG Interface for a functional description.

Bit	Symbol	Description	Access	Reset Value
31:24	JTAG_VIO_TCK _CLK_DIV	JTAG Vector-I/O TCK Clock Divider Divider applied onto the internal processing clock to obtain/generate the JTAG TCK I/O clock JTAG_TCK = 53.2MHz / (divider +1) *Default value results in an 1.6625 MHz TCK frequency*	r/w	0x1F
23:16	JTAG_VIO_XFER_ LEN	JTAG Vector-I/O Transfer Length Sets the number of transfer cycles (TCK clocks) performed during a Vector-I/O operation *Default value causes 256 full clock cycles (rising and falling edges) to be emitted on TCK*	r/w	0xFF
15:14	-	Reserved	-	0
13	JTAG_VIO_SHIFT_ REQ	JTAG Vector-I/O Shift Request Initiates a TMS/TDI shift-out operation (incl. TDO read-in) operation *TMS/TDI are coupled. Both vectors are shifted out at the same time.* *The TMS/TDI data interface registers limit the transfer length*	r/s	0
12	JTAG_VIO_GET_ REQ	JTAG Vector-I/O Get Request Initiates a TDO read-in only operation *The TDO data interface register limits the transfer length if all read-in data is required*	r/s	0
11:9	-	Reserved	-	0
8	JTAG_VIO_EN-	JTAG Vector-I/O Enable Controls the state of the BCC JTAG Vector-I/O Interface. 0b0 = Vector-I/O disabled 0b1 = Vector-I/O enabled *Functionality is held in reset until enabled is set*	r/w	0

7	JTAG_BIO_TDO	JTAG bit-I/O - TDO TDO line output state of the User FPGA	r	-
6	JTAG_BIO_TDI	JTAG bit-I/O - TDI Output state for the User FPGA TDI input line	r/w	1
5	JTAG_BIO_TMS	JTAG bit-I/O - TMS Output state for the User FPGA TMS input line	r/w	1
4	JTAG_BIO_TCK	JTAG bit-I/O - TCK Output state for the User FPGA TCK input line	r/w	0
3:1	-	Reserved	-	0
0	JTAG_BIO_EN	JTAG bit-I/O Enable Controls the state of the BCC JTAG bit-I/O Interface. 0b0 = bit-I/O disabled 0b1 = bit-I/O enabled	r/w	0

Table 5-9 : User FPGA JTAG Signal Line Register

5.2.3 User FPGA JTAG TMS Data Register - 0x88

Bit	Symbol	Description	Access	Reset Value
31:0	JTAG_VIO_TMS_DATA	JTAG Vector-I/O TMS Data Sets the JTAG TMS bit data that is shifted-out during TMS/TDI shift operations. *Note: bit 0 is shifted-out first (right-alignment)*	r/w	0

Table 5-10 : User FPGA JTAG TMS Data Register

5.2.4 User FPGA JTAG TDI Data Register - 0x8C

Bit	Symbol	Description	Access	Reset Value
31:0	JTAG_VIO_TDI_DATA	JTAG Vector-I/O TDI Data Sets the JTAG TDI bit data that is shifted-out during TMS/TDI shift operations. *Note: bit 0 is shifted-out first (right-alignment)*	r/w	0

Table 5-11 : User FPGA JTAG TDI Data Register

5.2.5 User FPGA JTAG TDO Data Register - 0x90

Bit	Symbol	Description	Access	Reset Value
31:0	JTAG_VIO_TDO _DATA	JTAG Vector-I/O TDO Data Accumulates TDO bit data read-in during TMS/TDI shift and TDO get request operations *Note: bit 0 is shifted-in last (right-alignment)*	r/w	0

Table 5-12 : User FPGA JTAG TDO Data Register

5.2.6 I2C Bridge Register - 0xA0

Refer to the chapter I2C Bridge for a functional description.

Bit	Symbol	Description	Access	Reset Value
31:1	-	-	-	0
0	I2C_BRDG_MODE_EN	I2C Bridge Mode Enable Controls the USER I2C Bus BCC reach-through onto the management I2C Bus '0' = disabled '1' = enabled	r/w	0

Table 5-13 : I2C Bridge Register

5.2.7 Interrupt Enable Register - 0xC0

Bit	Symbol	Description	Access	Reset Value
31:2		Reserved		0
1	ISP_INS_IE	ISP SPI Instruction Done Event Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled While disabled, the corresponding bit in the Interrupt Status Register is '0'. Disabling interrupts does not affect the interrupt source.	R/W	0
0	ISP_DAT_IE	ISP SPI Page Data Request Event Interrupt Enable 0: Interrupt Disabled 1: Interrupt Enabled While disabled, the corresponding bit in the Interrupt Status Register is '0'. Disabling interrupts does not affect the interrupt source.	R/W	0

Table 5-14 : Interrupt Enable Register

5.2.8 Interrupt Status Register - 0xC4

Bit	Symbol	Description	Access	Reset Value
31:2		Reserved		0
1	ISP_INS_IS	ISP SPI Instruction Done Event Interrupt Status When set, the PCI INTA# interrupt is asserted. The Interrupt is cleared by writing a '1'. 0: Interrupt not active or disabled 1: Interrupt active and enabled	R/C	0
0	ISP_DAT_IS	ISP SPI Page Data Done Event Interrupt Status When set, the PCI INTA# interrupt is asserted. The Interrupt is cleared by writing a '1'. 0: Interrupt not active or disabled 1: Interrupt active and enabled	R/C	0

Table 5-15 : Interrupt Status Register

5.2.9 User FPGA Configuration Control/Status Register - 0xD0

Bit	Symbol	Description	Access	Reset Value
31:5		Reserved		0
4	K7_LINK_ENA	1: Kintex™ 7 to PCIe-Switch LINK is enabled 0: Kintex™ 7 to PCIe-Switch LINK is disabled	R/W	1
3	FP_INIT_STAT	User FPGA INIT_B Pin Status 0: FPGA INIT_B Pin Level is Low (active) 1: FPGA INIT_B Pin Level is High (not active)	R	x
2	FP_DONE_STAT	User FPGA DONE Pin Status The FPGA Done pin is high in case of successful FPGA configuration. 0: FPGA DONE Pin Level is Low (not active) 1: FPGA DONE Pin Level is High (active)	R	x
1	FP_RE_CFG	After power-up the FPGA automatically configures from the on-board SPI Flash in 'Master Serial / SPI' mode. User FPGA Re-Configuration 1: Set all FPGA I/O pins to High-Z and prepare a User FPGA Re-Configuration 1 → 0: Start User FPGA Re-Configuration	R/W	0
0	FP_CFG_MD	Set User FPGA Configuration Mode 0: Master Serial / SPI 1: Slave SelectMap (Parallel) After power-up the User FPGA automatically configures from the on-board SPI Flash in 'Master Serial / SPI' mode.	R/W	0

Table 5-16 : User FPGA Configuration Control/Status Register

5.2.10 User FPGA Configuration Data Register - 0xD4

Bit	Symbol	Description	Access	Reset Value
31:0	ISP_FP_DAT	ISP Select Map Write Data Write Data Register for direct Slave Select Map FPGA programming mode Must be written with 32 bit FPGA programming data until the FPGA Done pin goes high (after the actual programming data, writing some dummy data may be required).	W	-

Table 5-17 : User FPGA Configuration Data Register

The User FPGA Configuration Data Register is used to write data within the User FPGA Slave Select Map Configuration directly to the User FPGA.

5.2.11 ISP Control Register - 0xE0

Bit	Symbol	Description	Access	Reset Value
31:1		Reserved		0
0	ISP_EN	ISP Mode Enable 0: Disable ISP Mode 1: Enable ISP Mode This bit controls the BCC interface between BCC, SPI-Flash and the User FPGA (Kintex™ 7). When set, the BCC is both SPI Flash Master and FPGA Configuration Interface Master. Must be set to 1 for direct Slave Select Map mode or SPI Flash programming. Must be set to 0 when the User FPGA should configure from the SPI Flash (e.g. after SPI Flash programming) in 'Master Serial / SPI' mode. Note, that for ISP Direct FPGA Programming, the FPGA must first be set to Slave Select Map configuration mode.	R/W	0

Table 5-18 : ISP Control Register

5.2.12 ISP Configuration Register - 0xE4

Bit	Symbol	Description	Access	Reset Value
31:24	ISP_SPI_ADD	SPI Flash Address A7-A0	W	0x00
23:16		SPI Flash Address A15-A8	W	0x00
15:8		SPI Flash Address A23-A16	W	0x00
7:0	ISP_SPI_INS	SPI Flash Instruction Code Supported Instructions: 0x02 – Page Program 0x20 – Sector Erase 0xC7 – Chip Erase 0x03 – Read Data	W	0x00

Table 5-19 : ISP Configuration Register

5.2.13 ISP Command Register - 0xE8

Bit	Symbol	Description	Access	Reset Value
31:2		Reserved	-	0
1	ISP_SPI_RST_CMD	ISP SPI Reset Command bit Writing a '1' sets the Instruction Busy bit in the ISP Status Register (if not already set). Breaks any ISP SPI instruction in progress and resets the ISP SPI logic. Check the Instruction Busy bit in the ISP Status Register for reset done status. Always read as '0'.	R/W	0
0	ISP_SPI_INS_CMD	ISP SPI Start Instruction Command bit Writing a '1' sets the SPI Instruction Busy bit in the ISP Status Register and starts the configured SPI instruction. Ignored (lost) while the Instruction Busy bit is set in the ISP Status Register. Always read as '0'.	R/W	0

Table 5-20 : ISP Command Register

5.2.14 ISP Status Register - 0xEC

Bit	Symbol	Description	Access	Reset Value
31:2		Reserved	-	0x00_0000
1	ISP_SPI_ INS_BSY	ISP SPI Instruction Busy Status Set & Cleared automatically by HW. Includes SPI Flash internal program/erase times. When clear again after being set, a new ISP SPI instruction may be started. Capable of generating an event based interrupt. 0: No ISP SPI Instruction in Progress 1: ISP SPI Instruction in Progress	R	0
0	ISP_SPI_ DAT_BSY	ISP SPI Data Transfer Busy Status Set & Cleared automatically by HW. Does not include SPI Flash internal program/erase times. When clear again after being set, new SPI Flash page data may be written to the ISP Data Space (in program mode) or SPI Flash page data is available in the ISP data space (in read mode). Capable of generating an event based interrupt. 0: No ISP SPI Data Transfer in Progress 1: ISP SPI Data Transfer in Progress	R	0

Table 5-21 : ISP Status Register

5.2.15 TXMC639 Board Temperature Sensor Register - 0xF4

Bit	Symbol	Description	Access	Reset Value
31:21	-	Reserved	r	-
20	TMP441_AUTO _TRD_EN	TMP441 Automatic Temperature Read Enable Controls the periodic board temperature read feature. Refresh time = 1s '0' = disabled '1' = enabled *Automatic mode must be disabled before enabling the I2C bridge mode*	r/w	1
19:16	-	Reserved		0
15:8	TMP441_TEMP	TMP441 Temperature Data Measured data of the on-board temperature sensor The read value of the temperature sensor is stored sign-extended as a 8 bit two's complement. To actually calculate the temperature from the two's complement data value, use the following formula: Temperature (°C) = TEMP	r	-
7:0	-	Reserved	-	-

Table 5-22 : TXMC639 Board Temperature Sensor Register

5.2.16 TXMC639 Serial Number Register - 0xF8

Bit	Symbol	Description	Access	Reset Value
31:0	S_NUMBER	The value is the unique serial number of each TXMC639 module	r	-

Table 5-23 : TXMC639 Serial Number Register

Example: 0x0092_AEE6 => SNo.: 9613030

5.2.17 BCC - FPGA Code Version - 0xFC

Bit	Symbol	Description	Access	Reset Value
31:0	CODE_VER	The value shows the BCC Firmware code version of the TXMC639 module.	R	-

Table 5-24: BCC - FPGA Code Version

6 Interrupts

6.1 Interrupt Sources

6.1.1 User FPGA (Kintex™ 7)

The User FPGA interrupt sources depend on the user application and are not part of this target specification.

6.1.2 BCC

The BCC provides two interrupt sources. Both interrupts are used in the context of SPI programming instructions. The Slave Select Map Mode does not provide interrupt support.

- ISP SPI Instruction Done Event Interrupt

  Event-based internal interrupt that becomes active (if enabled), when the ISP SPI Instruction Busy status bit changes from busy to not-busy.

- ISP SPI Page Data Done Event Interrupt

  Event-based internal interrupt that becomes active (if enabled), when the ISP SPI Data Busy status bit changes from busy to not-busy.

These interrupts indicates that an ISP operation is done.

6.2 Interrupt Handling

6.2.1 User FPGA (Kintex™ 7)

The interrupt handling depends on the user application and is not part of this target specification.

6.2.2 BCC

The Local Configuration Register Space located in the BCC provides an interrupt enable register and an interrupt status register.

Interrupt sources are enabled in the interrupt enable register. If enabled, upon an interrupt event, the corresponding bit in the interrupt status register is set. If any interrupt status bit is set in the interrupt status register, an interrupt request is asserted.

Both Interrupts of the BCC must be cleared via write access to the corresponding Interrupt Status Flag in the Interrupt Status Register (active-high write clear).

7 Functional Description

7.1 User FPGA Block Diagram

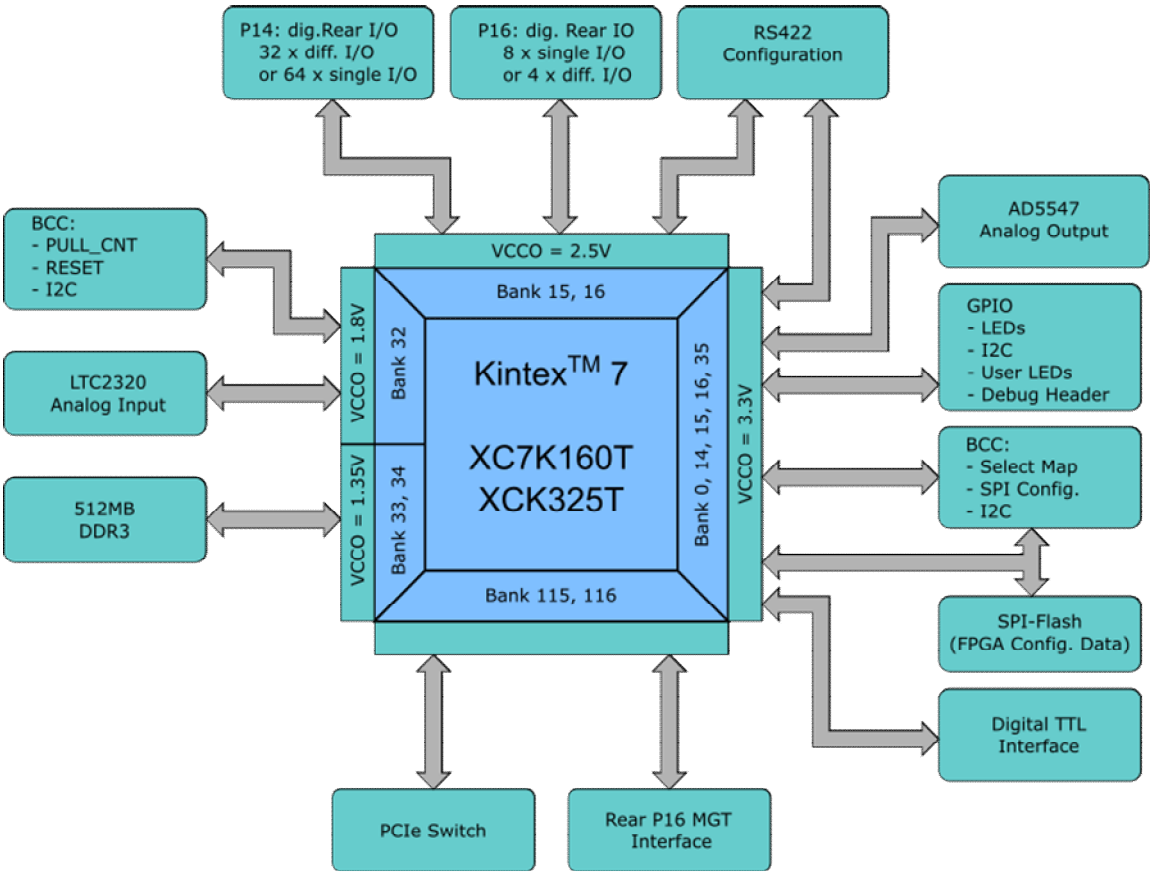


Figure 7-1 : FPGA Block Diagram

For pin assignment, I/O standard, slew rate and driver performance please use the XDC files of the TXMC639 BRD Project.

7.2 User FPGA Highlights

The FPGA is a Kintex™ 7 XCAK160/325T FPGA. The Kintex™ 7 FPGA in a FBG676 package provides eight MGT, four for high speed rear I/O communication and four for the PCI Express interface (x4 Linkage).

Board Option	Kintex™ 7	Logic Cells	Slices	DSP Slices	Block RAM (Kb)			CMTs	GTX	XADC Block
					18 Kb	36 Kb	max(Kb)			
-10R	XC7K160T	162,240	25.350	600	650	325	11,700	8	8	1
-11R	XC7K325T	326,080	50.950	840	890	445	16,020	10	8	1

Table 7-1 : TXMC639 FPGA Feature Overview

PCI Express Highlights:

- Compliant to the PCI Express Base Specification 2.1 with Endpoint and Root Port capability.
- Supports Gen1 (2.5 Gb/s) and Gen2 (5 Gb/s)

XADC Highlights:
XADC (Analog-to-Digital Converter)

On-chip temperature (±4°C max error) and power supply (±1% max error) sensors

- Continuous JTAG access to ADC measurements
- Internal access to all internal sensors of the Kintex™ 7

The board supports JTAG, master serial mode configuration from SPI-Flash or Slave Select MAP configuration for the User FPGA (Kintex™ 7) via the Board Configuration Controller (BCC).

The User FPGA is equipped with 8 I/O banks and 8 GTP (Gigabit Transceiver).

Bank	VCCO	VREF	Signals	Note
Bank 0	3.3 V	none	SPI Configuration Slave Select Map Configuration parallel DAC Interface User LEDs Digital TTL Interface Digital RS422	
Bank 14	3.3 V	none		
Bank 12	3.3 V	none		
Bank 13	3.3 V	none		
Bank 15	2.5 V	none	64 bit Rear I/O Interface to P14 RS422 Enable Interface Additional digital interface to P16	
Bank 16	2.5 V	none		
Bank 32	1.8 V	none	ADC Interface	
Bank 33	1.35 V	0.625 V	32 bit DDR3 Memory Interface 1GB	
Bank 34	1.35 V	0.625 V		
Bank 213	Connected to XMC P16 Rear I/O connector			
Bank 216	PCIe X4 Interface to PCIe Switch Device			

Table 7-2 : FPGA Bank Usage

For a detailed overview of all user FPGA I/O pins and the respective constrains to be set for each pin, TEWS Board Reference Design constrain files "txmc639_xc7k_xxxt_fbg676.xdc" should be used.

7.3 User FPGA Gigabit Transceiver (MGT)

The TXMC639 provides four MGT as Kintex™ 7 PCI Express Endpoint Block and four MGT for a high speed XMC P16 Rear I/O interface.

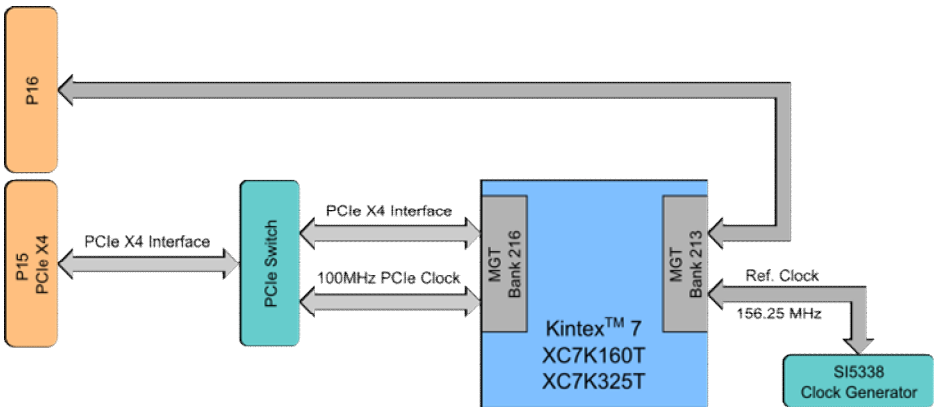


Figure 7-2 : User FPGA MGT Block Diagram

MGT	TXMC639 Signal	FPGA Pins	Connected to
MGTXTXP0_115	MGTTX0	P2 / P1	connected to Rear I/O XMC P16 Interface
	MGTRX0	R4 / R3	
MGTXTXP1_115	MGTTX1	M2 / M1	
	MGTRX1	N4 / N3	
MGTXTXP2_115	MGTTX2	K2 / K1	
	MGTRX2	L4 / L3	
MGTXTXP3_115	MGTTX3	H2 / H1	
	MGTRX3	J4 / J3	
MGTXTXP0_116	PET_07	F2 / F1	used for PCI Express Endpoint Block and connected to XMC P15 Connector
	PER_07	G4 / G3	
MGTXTXP1_116	PET_06	D2 / D1	
	PER_06	E4 / E3	
MGTXTXP2_116	PET_05	B2 / B1	
	PER_05	C4 / C3	
MGTXTXP3_116	PET_04	A4 / A3	
	PER_04	B5 / B5	

Table 7-3 : User FPGA MGT Connections

The MGT clock MGTREFCLK0_116 (PCI Express Endpoint Block clock reference) of 100 MHz is generated by the PI7C9X2G312GP PCIe Switch. The MGTREFCLK0_115 is connected to a 125 MHz clock output of the Si5338 low jitter clock generator. MGTREFCLK1_115 and MGTREFCLK1_116 are not used on the TXMC639.

MGT	TXMC639 Signal	FPGA Pins	Connected to
MGTREFCLK0_115	CLK_MGT±	H6 / H5	125 MHz Si5338 Clock Generator
MGTREFCLK1_115	not used	K6 / K5	not connected
MGTREFCLK0_116	REFCLKO2±	D6 / D5	100 MHz PI7C9X2G312GP PCIe Switch
MGTREFCLK1_116	not used	F6 / F5	not connected

Table 7-4 : User FPGA MGT Reference Clocks

7.4 User FPGA Configuration

The Kintex™ 7 can be configured by the following interfaces:

- Master Serial SPI Flash Configuration Interface
- JTAG Interface via FPGA JTAG Connector
- PCIe Interface via BCC FPGA Slave Select Map Interface Configuration

The change of the configuration mode is done with a configuration register of the BCC FPGA.

At Power-up, the TXMC639 User FPGA (Kintex™ 7) always configures via x4 SPI Interface by "Master Serial / SPI" mode. At factory default the SPI Flash contains the TEWS Board Reference Design application for the TXMC639 User FPGA device.

7.4.1 Master Serial SPI Flash Configuration

It is important for User FPGA Configuration via SPI Master Mode that the ISP Mode Enable (ISP_EN) bit is clear to disable the ISP Mode. This is also the default value after Power Up.
See also Register Description of TXMC639 Configuration Device.

To comply with the PCI-Express specification it is necessary to perform the configuration as quickly as possible. The PCIe specification demands that a PCI device must be accessible after 100ms (120ms). To speed up the SPI Configuration the following points must be taken into account for SPI bitstream generation.

- External Clock Master (53.2MHz) should be used.
- If external Clock Master is used, the SPI Falling Edge Option must be used.
- SPI Configuration Bus Width should be set to X4.
- AMD Tandem Configuration Feature could be used for full PCI-Express specification compliance. Already during PCI-Express IP Core generation this configuration feature must be included. (For more information see: AMD XAPP1179).
- If the Tandem Configuration feature is used, the Persist Option is mandatory.
- For smaller FPGA content, it is sometimes also possible to comply with the PCI-Express specification, when only bitstream Compression is used.

To avoid damage on the BCC or User FPGA (Kintex™ 7) if Tandem configuration or the Persist Option is used, the User FPGA must be set into reconfigure Mode by using the "FP_RE_CFG" bit of the User FPGA Configuration Control/Status Register before Programming or Clearing the SPI Flash.

All required general settings, bitstream setting and additional constraints for a compressed tandem SPI X4 configuration could be found in the TXMC639 Board Reference Design application.

Note: Changing a configuration to tandem configuration results in a change in the timing of the design.

7.4.2 Manually User FPGA SPI Flash Reconfiguration

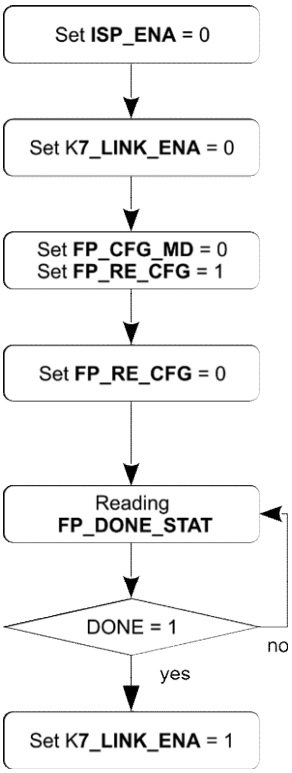
A manually User FPGA Reconfiguration can be performed with the User FPGA Reconfigure Command in the Global Configuration Register.

Set the User FPGA Reconfigure Command to set the User FPGA to configuration state with all FPGA I/O pins are High-Z.

Use the following procedure to perform a User FPGA SPI Reconfiguration

- Assure that ISP Mode Enable is disabled.
- By Reconfiguring the Kintex™ 7 the AMD PCIe endpoint is reloaded and is temporarily not available on the PCI bus. To avoid error messages of the PCIe switch the link between the PCIe Switch and the Kintex™ 7 is disabled.
- Set the User FPGA Configuration Mode (FP_CFG_MD) to Master Serial / SPI and prepare the FPGA Reconfiguration.
- Start the FPGA Reconfiguration by setting the FP_RE_CFG bit of the User FPGA Configuration Control/Status Register to 0.
- Assure that the FPGA DONE Pin status shows a successful FPGA Configuration.

  0: FPGA DONE Pin Level is Low (FPGA is not configured)
  1: FPGA DONE Pin Level is High (FPGA is configured)
- The link between the PCIe Switch and the Kintex™ 7 must be enabled.



A successful User FPGA configuration is indicated with FPGA_DONE status in the Global Status Register and the on-board User FPGA Done LED.

It must be considered in any case, that the Reconfiguration of the User FPGA also reconfigures the PCIe Endpoint of the User FPGA. This leads to the consequence that the PCI Header of the User FPGA PCIe Endpoint no longer exists. For this purpose it is necessary to disable the link between the PCIe switch and the User FPGA PCIe Endpoint before preparing the FPGA Reconfiguration and to enable the link again after reconfiguration.

Additionally, after FPGA Reconfiguration the User FPGA PCIe Endpoint PCI Header must be configured again. If the PCIe interface of the User FPGA PCIe Endpoint does not change. Device ID, Vendor ID, Class Code and PCI Bars do not change, the PCI header could be saved before the FPGA Reconfiguration and written back to configuration space after the Reconfiguration.

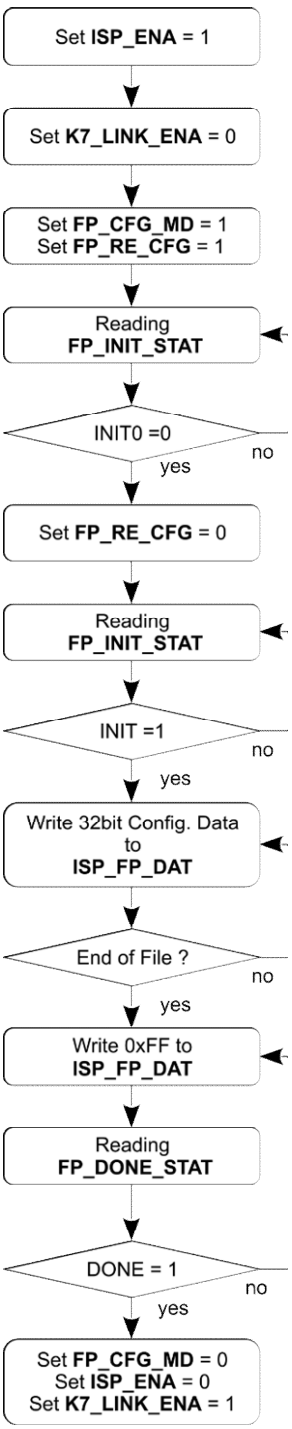
7.4.3 Slave Select Map Configuration

For direct User FPGA configuration via PCIe Interface the **User FPGA Configuration Mode** must be set to **Slave SelectMap** Mode. The on-board logic sets the User FPGA in configuration state with all FPGA I/O pins switches to High-Z. User FPGA is now ready for new configuration data.

The following procedure is required for Select Map Mode User FPGA configuration / reconfiguration.

- First the In System Program (ISP) Mode must be enabled.
- By reconfiguring the Kintex™ 7 the AMD PCIe endpoint is reloaded and is temporarily not available on the PCI bus. To avoid error messages of the PCIe switch the link between the PCIe Switch and the Kintex™ 7 is disabled.
- Check response of the Kintex™ 7 by reading the FPGA INIT_B pin value. If the Level is low the Kintex™ 7 FPGA is in Reset Mode, and then configuration process could be continued.
- Start the FPGA Reconfiguration by setting the FP_RE_CFG bit of the User FPGA Configuration Control/Status Register to 0.
- Check response of the Kintex™ 7 by reading the FPGA INIT_B pin value. While the FPGA INIT_B pin Level is low the Kintex™ 7 isn't ready for configuration.
- If FPGA INIT_B pin high then the configuration data must be continually written to the ISP SelectMap Data Register. Typically 2860903 PCI write accesses are required to configure a Kintex™ 7 325T.
- Dummy Write accesses to create configuration clock cycles while FP_DONE_STAT is low.
- A successful configuration of the User FPGA is indicated with FP_DONE_STAT in the User FPGA Configuration Control/Status Register and the on-board User FPGA Done LED.

  0: FPGA DONE Pin Level is Low (FPGA is not configured)
  1: FPGA DONE Pin Level is High (FPGA is configured)
- After reconfiguration was successful the User FPGA Configuration Mode and the ISP Mode could be disabled. Also the link between the PCIe Switch and the Kintex™ 7 must be enabled.



If not all configuration data bytes are written the User FPGA is not configured correctly.

The number of bytes that must be written corresponds to the size of the AMD configuration files. Typically the .bin or the .bit file could be used as data source.

The .bit file is the standard generated programming file. This is a binary configuration data file which contains header information that does not need to be downloaded to the FPGA. For generating the .bin file the bitGen option must be used. This is also a binary configuration data file but without header information. For configuration of the Kintex™ 7 FPGA on the TXMC639 both files could be used. Both binary configuration data files have additional data to the actual configuration data.

See also the AMD User Guide (ug470) “7 Series FPGAs Configuration” for more information about Configuration Details and Configuration Data File Formats.

The following bitGen options are mandatory for the Slave Select Map Configuration via BBC.

- External Clock Master (53.2MHz) must be used.
- In contrast to SPI Configuration Mode, the Falling Edge Option must be switched off.

Additional important bitGen Options:

- For a faster configuration the bitstream Compression could be used.
- The Persist Option is not needed. But if this option is used, the User FPGA must be set into reconfigure Mode by using the “FP_RE_CFG” bit of the User FPGA Configuration Control/Status Register before Programming or Clearing the SPI Flash.

AMD Tandem Configuration Feature cannot be used for Slave Select Map Configuration. It is therefore necessary to remove the Tandem Configuration Feature from the PCIe IP Core.

A design that is intended for the SPI configuration cannot be used by Slave Select Map configuration and vice versa.

7.4.4 Configuration via JTAG

The TXMC639 provides two JTAG chains which are accessible by the following connector options:

7.4.4.1 User JTAG Chain

For direct FPGA configuration, FPGA read back or in-system diagnostics with Vivado Logic Analyzer, the Molex Debug Connector can be used to access the JTAG-chain. Also an indirect SPI – PROM programming is possible via the User JTAG Chain. This Connector provides a direct connection to a AMD USB Programmer II compatible 2 mm shrouded header.

The second possible source is the BCC internal JTAG TAB controller. See chapter 7.12 JTAG Controller to A7 JTAG Interface.

The Molex JTAG connector has default priority. If a cable is connected here, the BCC switches this interface active. However, each of the sources can be selected via the User FPGA JTAG Control and Status Register - 0x80 in BCC.

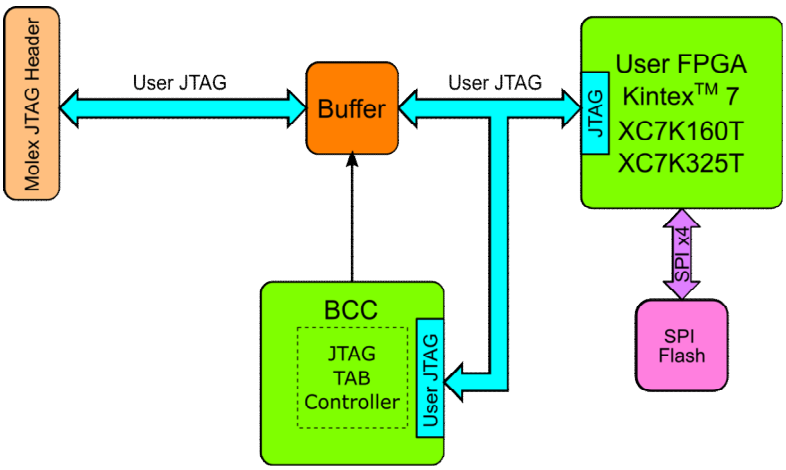


Figure 7-3 : User JTAG-Chain

7.4.4.2 TEWS Factory JTAG Chain

The TEWS Factory JTAG Chain is accessible from the PCIe Edge Connector.

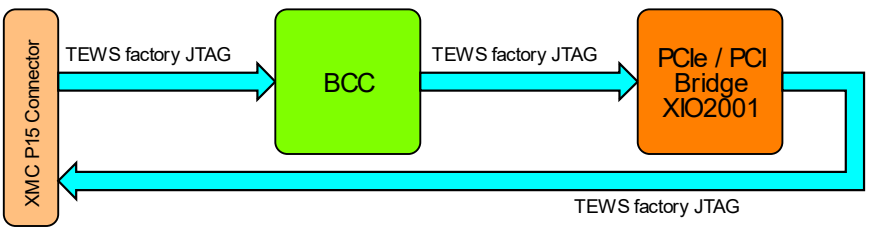


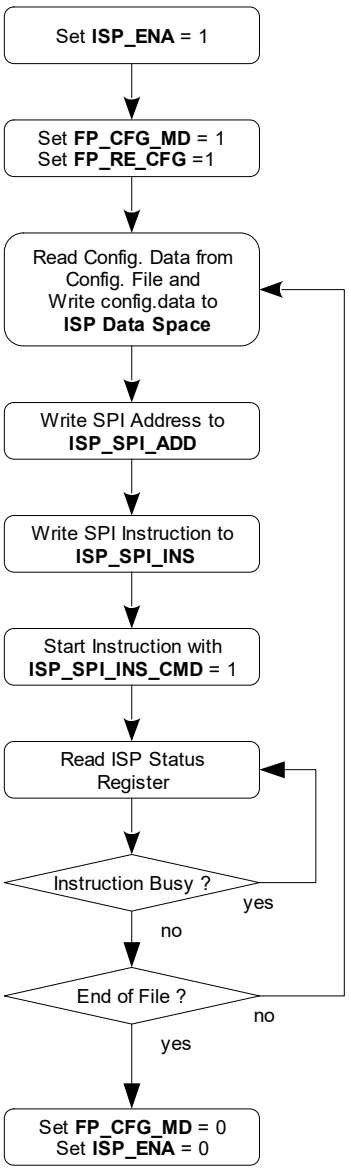
Figure 7-4 : TEWS Factory JTAG-Chain

7.4.5 Programming User FPGA SPI Configuration Flash

To program the User FPGA SPI Configuration Flash the **User FPGA Configuration Mode** must be set to **Master Serial / SPI** and the ISP Mode must be enabled.

The following procedure is required for User FPGA SPI Configuration Flash programming and subsequent reconfiguration of the User FPGA.

- Enable the ISP Mode in the ISP Mode Enable Register.
- Assure that User FPGA Configuration Mode is set to SPI Flash. If the FPGA is not configured or if it is possible that the FPGA accesses the SPI flash during BCC access set FP_RE_CFG = 0b1. Link must be set to disable previously!
- Read Configuration data from Configuration File and write Data to the In Circuit Programming Data Space. 256Byte (1 SPI Flash page) each time can be programmed maximally.
- Set the programming start address and write instruction in the ISP Configuration Register.
- Start the Instruction with ISP Command Register
- Wait on ISP SPI Instruction Done or ISP SPI Page Data Done for next write instruction.
- Process should be repeated until all configuration data is written to the SPI Flash
- After completion of the data programming, the ISP Mode bit must be cleared to set configuration path to User FPGA and a Reconfiguration can be performed.



A successful configuration of the User FPGA is indicated with FP_DONE_STAT in the User FPGA Configuration Control/Status Register and the on-board User FPGA Done LED.

The Programming Instruction always starts at address 0x00 to write data from the ISP Programming Data Space to the SPI flash.

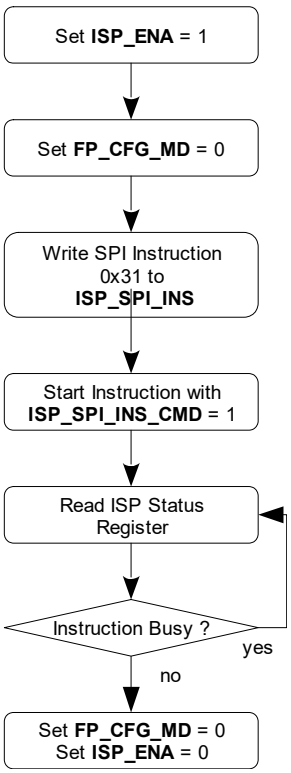
If not all configuration data bytes are written, the User FPGA is not configured correctly.

The source for the User FPGA SPI Configuration Flash data could be the .bin file. This file format can be created from the .bit file by using the AMD Vivado software.

7.4.6 Erasing User FPGA SPI Configuration Flash

For Chip Erase of the User FPGA SPI Configuration Flash the **User FPGA Configuration Mode** must be set to **Master Serial / SPI** and the ISP Mode must be enabled.

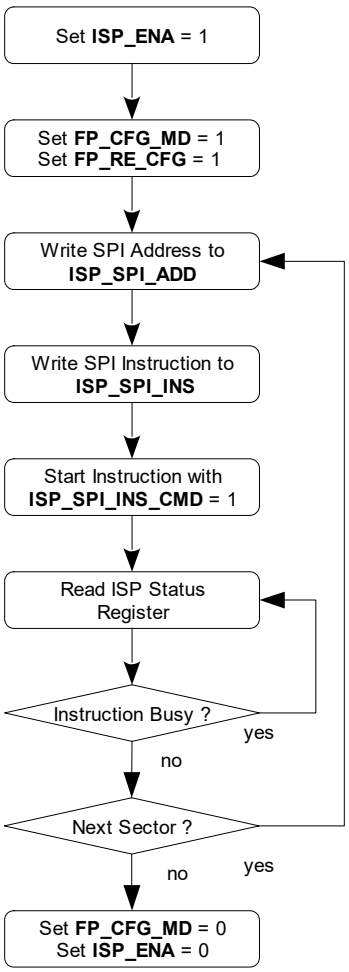
- Enable the ISP Mode in the ISP Mode Enable Register.
- Assure that User FPGA Configuration Mode is set to SPI Flash. If the FPGA is not configured or if it is possible that the FPGA accesses the SPI flash during BCC access set FP_RE_CFG = 0b1. Link must be set to disable previously!
- Set the Chip Erase instruction in the ISP Configuration Register.
- Start the Instruction with ISP Command Register
- Wait on ISP SPI Instruction Done or ISP SPI Page Data Done for erasing process end.
- After completion of the erasing process, the ISP Mode bit should be cleared to set configuration path to User FPGA or a User FPGA SPI Configuration Flash programming process could be done.



7.4.7 Sector Erasing User FPGA SPI Configuration Flash

For Sector Erase of the User FPGA SPI Configuration Flash the **User FPGA Configuration Mode** must be set to **Master Serial / SPI** and the ISP Mode must be enabled.

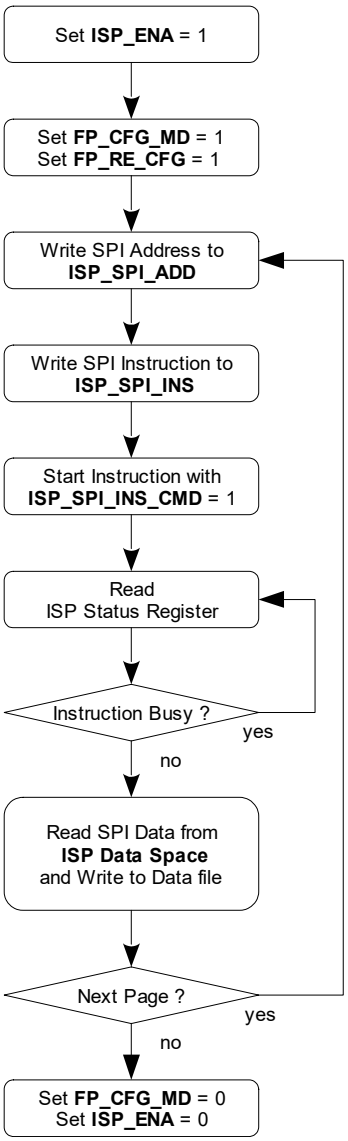
- Enable the ISP Mode in the ISP Mode Enable Register.
- Assure that User FPGA Configuration Mode is set to SPI Flash. If the FPGA is not configured or if it is possible that the FPGA accesses the SPI flash during BCC access set FP_RE_CFG = 0b1. Link must be set to disable previously!
- Write the Sector Address to the ISP Configuration Register
- Set the Chip Erase instruction in the ISP Configuration Register.
- Start the Instruction with ISP Command Register
- Wait on ISP SPI Instruction Done or ISP SPI Page Data Done for erasing process end.
- Process could be repeated for other sectors.
- After completion of the erasing process, the ISP Mode bit should be cleared to set configuration path to User FPGA or a User FPGA SPI Configuration Flash programming process could be done.



7.4.8 Reading User FPGA SPI Configuration Flash

To read the User FPGA SPI Configuration Flash the **User FPGA Configuration Mode** must be set to **Master Serial / SPI** and the ISP Mode must be enabled.

- Enable the ISP Mode in the ISP Mode Enable Register.
- Assure that User FPGA Configuration Mode is set to SPI Flash. If the FPGA is not configured or if it is possible that the FPGA accesses the SPI flash during BCC access set FP_RE_CFG = 0b1. Link must be set to disable previously!
- Set the reading start address and write instruction in the ISP Configuration Register.
- Start the Instruction with ISP Command Register
- Wait on ISP SPI Instruction Done or ISP SPI Page Data Done for next write instruction.
- Read one page of SPI Data from In Circuit Programming Data Space and write to Data file
- Process could be repeated until all needed data is written to the Data file.
- After completion of the reading process, the ISP Mode bit must be cleared to set configuration path back to User FPGA.



7.5 BCC (Board Configuration Controller) FPGA

The Board Configuration FPGA is factory configured, and handles the basic board setup and User FPGA (Kintex™ 7) Configuration.

Changing or erasing the BCF (Board Configuration Firmware) content leads to an inoperable TXMC639 FPGA configuration.

7.5.1 I2C Interface to BCC Register

The TXMC639 BCC provides an I2C Interface to the User FPGA (Kintex™ 7). Via this I2C Interface the TXMC639 Serial Number Register from the BCC Local Configuration Register Space could be read.

For the User FPGA (Kintex™ 7) an I2C Master interface is required to use this interface. For this purpose the BCC provides an I2C slave interface.

Signal	Bank	V_{CCO}	Pin	Description
FPGA_SCL	15	1.8 V	V14	Serial Clock Output A negative edge clock data out.
FPGA_SDA	15	1.8 V	W14	Bisectional Serial Data

Table 7-5: User FPGA I2C Interface to BCC

For pin assignment, I/O standard, slew rate and driver performance please use the XDC files of the TXMC639 BRD Project.

7.6 Clocking

7.6.1 FPGA Clock Sources

As a central clock generator of the TXMC639 the Si5338 clock generator is used. This provides all necessary clocks for the User FPGA and the Configuration FPGA.

The following figure depicts an abstract User FPGA clock flow.

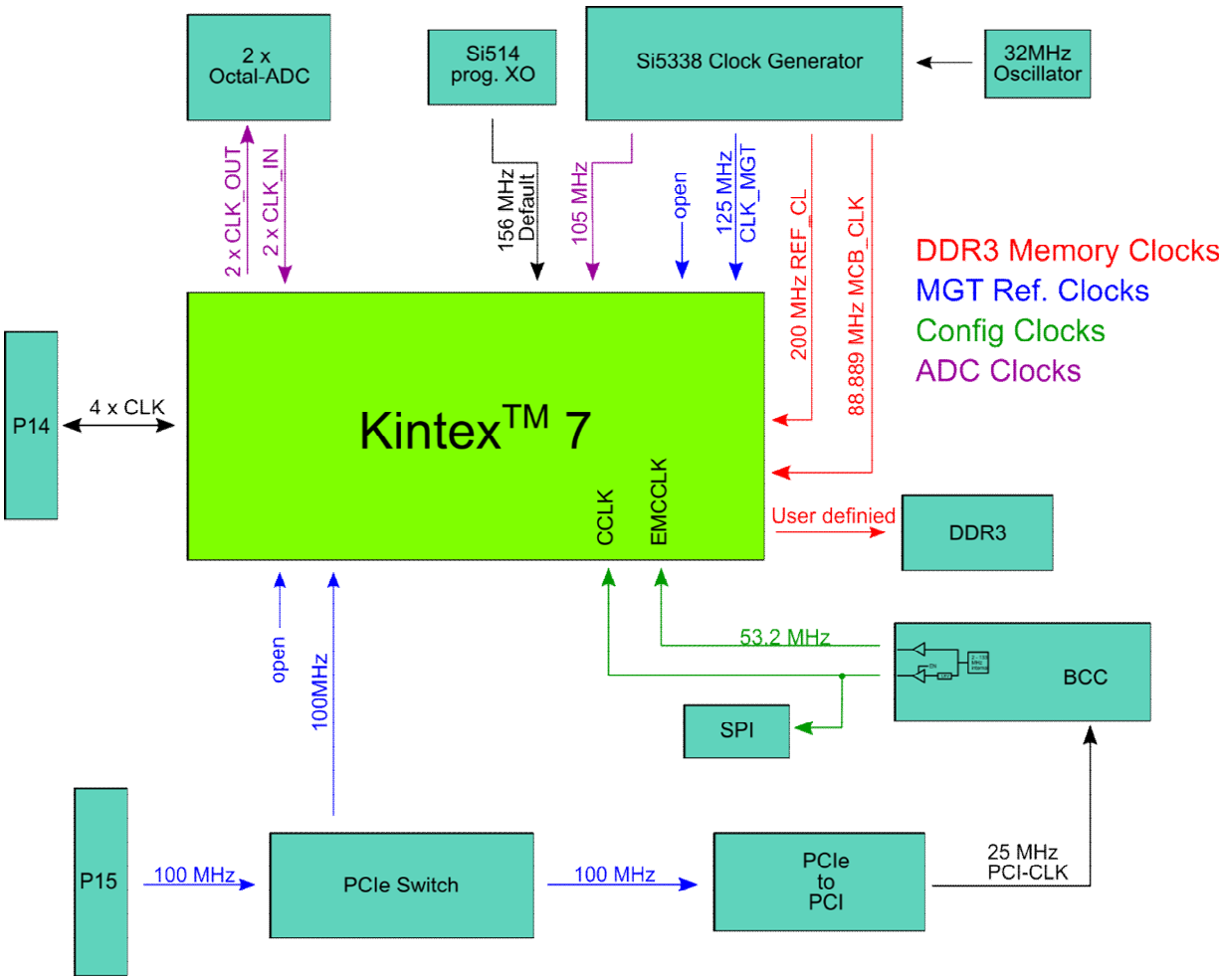


Figure 7-5 : FPGA Clock Sources

The following table lists the available clock sources on the TXMC639:

FPGA Clock Signal Name	FPGA Pin	Source	Description
CLK_MGT±	H6 / H5	SI5338 low-jitter clock generator	125 MHz differential MGT Reference clock for P16 Rear I/O Interface
REFCLKO2±	D6 / D5	PCIe Switch PI7C9X2G312GP	100 MHz differential PCIe Reference clock input
MCB_CLK±	AB11 / AC11	SI5338 low-jitter clock generator	88.889 MHz differential MCB CLK
REF_CLK±	AA10 / AB10	SI5338 low-jitter clock generator	200 MHz differential Reference clock
USER_CLKA	F22	SI5338 low-jitter clock generator	105 MHz Clock Input This clock is designated for ADC/DAC interface clock source.
TTL_IO_0	AB24	Front I/O Line	Single ended TTL based I/O Line
TTL_IO_1	AA23	Front I/O Line	Single ended TTL based I/O Line
TTL_IO_2	Y23	Front I/O Line	Single ended TTL based I/O Line
TTL_IO_3	AA24	Front I/O Line	Single ended TTL based I/O Line
TTL_IO_31	R21	Front I/O Line	Single ended TTL based I/O Line
TTL_IO_30	P21	Front I/O Line	Single ended TTL based I/O Line
TTL_IO_29	R22	Front I/O Line	Single ended TTL based I/O Line
TTL_IO_28	R23	Front I/O Line	Single ended TTL based I/O Line
REAR_IO0±	C12 / C11	Back I/O Connector	Diff. Back I/O Line from P14
REAR_IO1±	E11 / D11	Back I/O Connector	Diff. Back I/O Line from P14
REAR_IO8±	E10 / D10	Back I/O Connector	Diff. Back I/O Line from P14
REAR_IO10±	G11 / F10	Back I/O Connector	Diff. Back I/O Line from P14
DIG_IO_00±	H17 / H18	Back I/O Connector	Diff. Back I/O Line from P14
DIG_IO_01±	G17 / F18	Back I/O Connector	Diff. Back I/O Line from P14
DIG_IO_02±	F17 / E17	Back I/O Connector	Diff. Back I/O Line from P16
DIG_IO_03±	E18 / D18	Back I/O Connector	Diff. Back I/O Line from P16
K7_EMCCLK	B26	BCC	53.2 MHz used for external configuration clock (CCLK)
CCLK	C8	BCC	external Kintex -7 configuration clock

Table 7-6 : Available FPGA clocks

For pin assignment, I/O standard, slew rate and driver performance please use the XDC files of the TXMC639 BRD Project.

7.7 Serial ADC Interface

7.7.1 Overview

The 16 analog inputs of the TXMC639 are realized with 2 LTC2320-16 ADC devices. Each of these SAR-ADCs has eight ADC channels. Thus, a total of 16 ADC channels are available on the TXMC639.

A coarse overview over the analog input section of the TXMC639 is shown by the following figure:

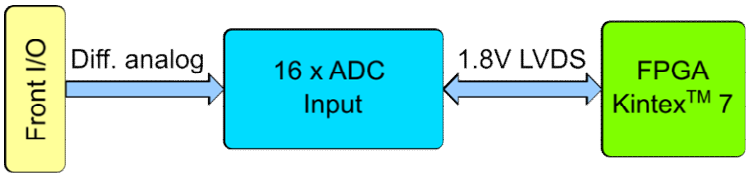


Figure 7-6 : Analog Input Section

The key-features of the LTC2320-16 are:

- Octal Channel - SAR-ADC
- 16 bit resolution
- **1.5Msps Throughput Rate for each Channel**
- LVDS SPI-Compatible Serial Interface to User FPGA (Kintex™ 7)

In order to adapt the LTC2320-16 to a max ±10.28 V input voltage on each input-pin (±20.56 V differential voltage range) two stage input operational amplifiers for input impedance conversion and gain adaption are needed in addition to the ADC.

The following figure shows the structure and principle of eight ADC inputs. All channels are connected via an impedance converter and a level adjustment to the LTC2320-16 octal channel ADC.

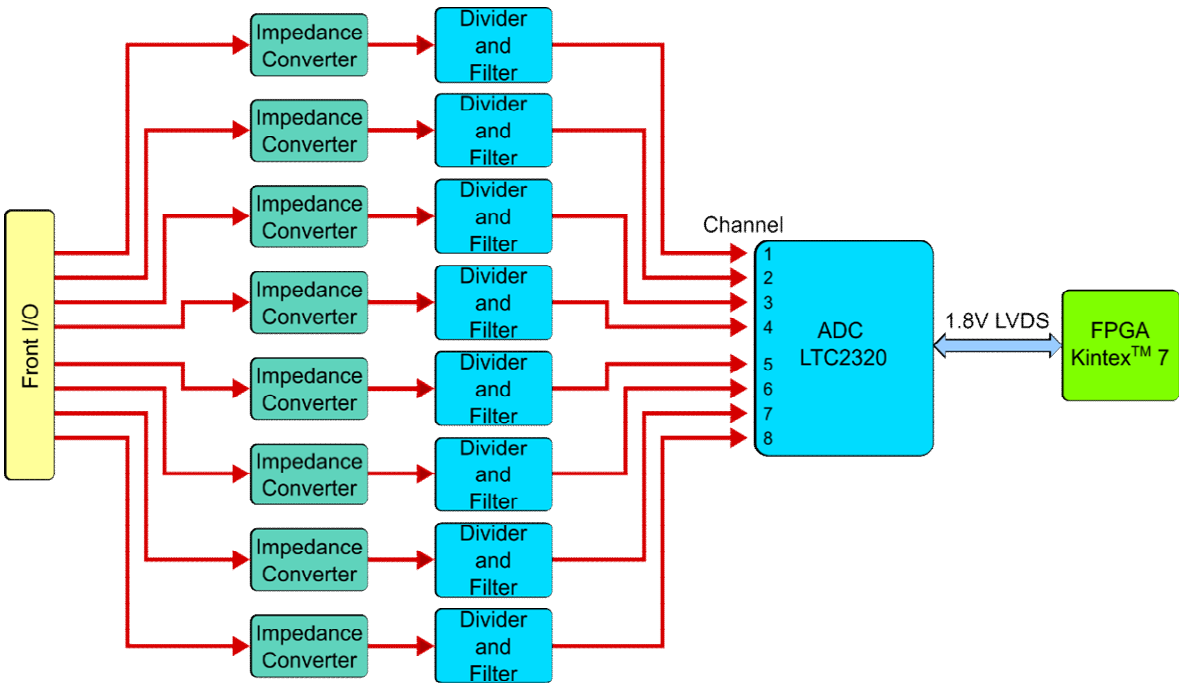


Figure 7-7 : Analog Input Block Diagram

7.7.2 ADC digital Output Coding

Differential common mode voltage is compensated by the analog input stage. In addition, the differential input voltage is reduced by an analogue divider which is built with a differential operational amplifier. The feedback resistors of this operational amplifier determine the divider value. With the ADC LTC2320-16's maximum analogue differential input voltage range of ±5.0 V a theoretical maximum of ±20.56 V differential input voltage range is given for a TXMC639 analog input channel.

Due to the ADC's true differential inputs, the ADC output coding significantly differs compared to a single-ended input.

Analogue to a single-ended input, where the range setting directly describes the ground related input voltage range, the ADC range setting describes the range of ground related voltages that can be tied to the ADC differential inputs. This results in an extended input voltage range, since the ADC measures the voltage between the differential inputs VIN- and VIN+.

An Example: The TXMC639 (differential input) voltage range is ±20.56 V, so the allowed (single-ended, ground related) voltage on each ADC input pin is ±10.28 V. When we examine the two largest differential voltages, we get following results:

VIN-	VIN+	ADC Input
-10.28 V	+10.28 V	+20.56 V
+10.28 V	-10.28 V	-20.56 V

Table 7-7: ADC Max Differential Voltages

The example shows that the range of differential ADC input values is -20.56 V to +20.56 V, which results to a full scale range of 41.12 V for the ±20.56 V ADC Input Range.

The TXMC639 data coding is two's complement.

7.7.2.1 ADC Data Coding ±20.56 V Voltage Range

Description	TXMC639	Digital Code
Full Scale Range	41.12 V	-
Least Significant bit	627 µV	-
Full Scale (pos.)	20.56 V	0x7FFF
Midscale + 1LSB	627 µV	0x0001
Midscale	0.0 V	0x0000
Midscale – 1LSB	-627 µV	0xFFFF
Full Scale (neg.)	-20.56 V	0x8000

Table 7-8: ADC Data Coding

7.7.2.2 ADC Data Coding ±10.28 V Voltage Range

Description	TXMC639	Digital Code
Full Scale Range	20.56 V	-
Least Significant bit	314 µV	-
Full Scale (pos.)	10.28 V	0x7FFF
Midscale + 1LSB	314 µV	0x0001
Midscale	0.0 V	0x0000
-FSR + 1LSB	-10.28 V	0x8001
Full Scale (neg.)	-10.28 V	0x8000

7.7.2.3 ADC Data Coding ±5.14 V Voltage Range

Description	TXMC639	Digital Code
Full Scale Range	10.28 V	-
Least Significant bit	157 µV	-
Full Scale (pos.)	5.14 V	0x7FFF
Midscale + 1LSB	157 µV	0x0001
Midscale	0.0 V	0x0000
Midscale – 1LSB	-157 µV	0xFFFF
Full Scale (neg.)	-5.14 V	0x8000

7.7.3 User FPGA Pinning

Each ADC is connected to the User FPGA (Kintex™ 7) via a dedicated serial clocked Interface. Each ADC device has one input clock, one output clock and one conversion signal. For the eight ADC channel there are four differential double datarate LVDS output lines. In addition, two ADC channels are provided via each data line in multiplex mode.

Signal	Bank	VCCO	Pin	Description
ADC_SCK_00±	32	1.8 V	AA19 / AA20	Differential Clock Output for ADC Channel 0 .. 7
ADC_SCKOUT_00+	32	1.8 V	AB17 / AC17	Differential Clock Input for ADC Channel 0 .. 7
ADC_SDOA_00+	32	1.8 V	V18 / V19	Differential Data from ADC Channel 0 + 1
ADC_SDOB_00+	32	1.8 V	W18 / W19	Differential Data from ADC Channel 2 + 3
ADC_SDOC_00+	32	1.8 V	W15 / W16	Differential Data from ADC Channel 4 + 5
ADC_SDOD_00+	32	1.8 V	Y17 / Y18	Differential Data from ADC Channel 6 +7
ADC_CNV_N_00	15	2.5 V	K15	Convert Signal for ADC Channel 0 .. 7

Signal	Bank	VCCO	Pin	Description
ADC_SCK_01±	32	1.8 V	AF14 / AF15	Differential Clock Output for ADC Channel 8 .. 15
ADC_SCKOUT_01+	32	1.8 V	AC18 / AD18	Differential Clock Input for ADC Channel 8 .. 15
ADC_SDOA_01+	32	1.8 V	AB19 / AB20	Differential Data from ADC Channel 8 + 9
ADC_SDOB_01+	32	1.8 V	AC19 / AD19	Differential Data from ADC Channel 10 + 11
ADC_SDOC_01+	32	1.8 V	AE18 / AF18	Differential Data from ADC Channel 12 + 13
ADC_SDOD_01+	32	1.8 V	AE17 / AF17	Differential Data from ADC Channel 14 + 15
ADC_CNV_N_01	15	2.5 V	M16	Convert Signal for ADC Channel 8 .. 15

To use the clocked serial interface between the User FPGA (Kintex™ 7) and one of the two LTC2320-16 ADC devices please use the LTC2320-16 data sheet which describes the communication process.

7.7.4 Programming Hints LTC2320-16

The LTC2320-16 digital interface is a double datarate X4 clocked SPI based interface.

This differential interface uses differential LVDS signals for serial data transfer. All LVDS signals need a termination on the receiver side of the connection. For the SCK± an external termination resistor is implemented on the TXMC639. The User FPGA inputs ADC_CLKOUT±, SDOA1±, SDOB±, SDOC± and SDOD± of each ADC channel need an FPGA internal termination. The corresponding constrains for the pin assignment, the I/O standard, termination and slew rate is specified in BRD XDC File.

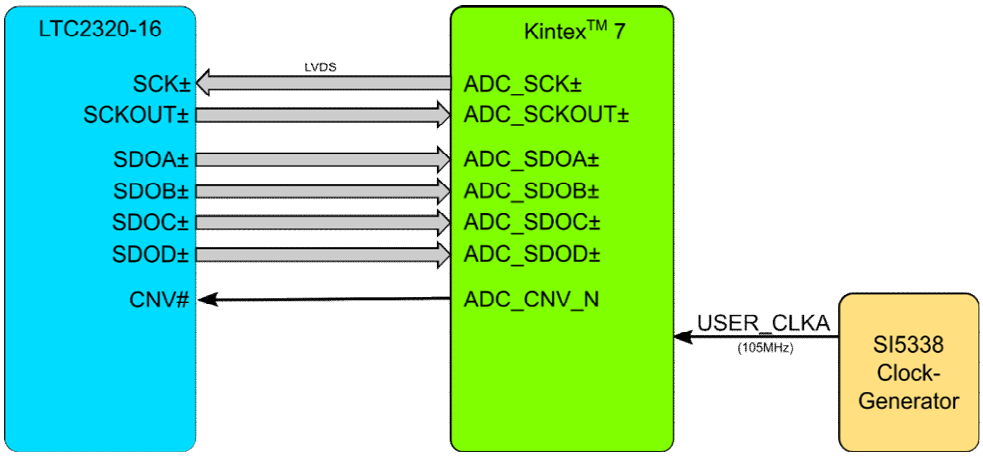


Figure 7-8 : Digital ADC to FPGA Interface

A conversion is triggered by a negative edge on the CNV# line. The acquisition is done during the positive phase of the CNV# signal. The conversion is realised via a D-type flip-flop in order to achieve the lowest possible jitter clock timing.

Following the FPGA drives the ADC_SCK clock, which then initiates the data transfer from the ADC to the FPGA. The ADC then transmits the serial data SDOA, SDOB,SDOC and SDOD synchronous as double data rate (DDR) to CLKOUT. The DDR sequence is MSB first and the LSB at least. The ADC almost always combines two channels in time multiplex on one data line.

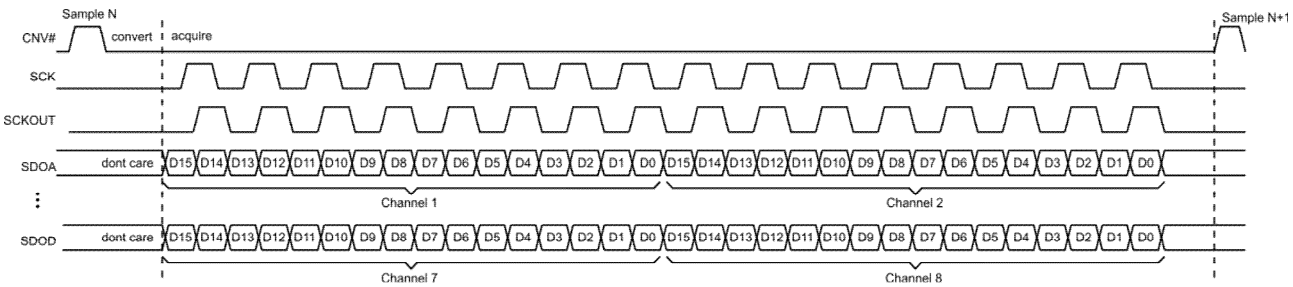


Figure 7-9 : Timing Diagram LTC2320-16 DDR-Mode (2 Channels per SDO Pair)

For a detailed description of the LTC2320-16 interface and the LTC2320-16 function please use the data sheet which describes the whole communication process and all special characteristics of the ADC.

For pin assignment, I/O standard, slew rate and driver performance please use the XDC files of the TXMC639 BRD Project.

7.8 Parallel DAC Interface

7.8.1 Overview

The 8 analog DAC outputs of the TXMC639 are implemented with four AD5547 16 bit Dual-Current DAC devices. Each of these DACs has two DAC channels. Thus, a total of 8 DAC channels are available on the TXMC639. Because of the fact that these DACs have a current output it is necessary to use operational amplifier for each DAC output channel to generate an output voltage range up to ±10 V.

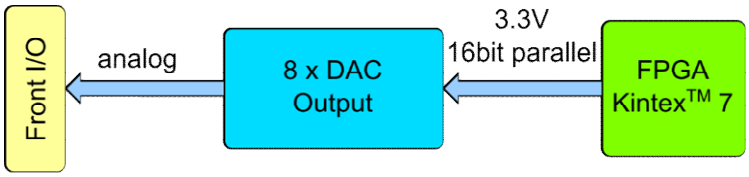


Figure 7-10 : Analog Output Section

As programming interface, a 16 bit parallel Bus is implemented. Respectively all four DAC devices (8 DAC channels) share this Kintex™ 7 16 bit data bus. To set each output individually each DAC device has its control interface.

The following figure shows the structure and principle of two DAC outputs. Both are connected via independent operational amplifiers to the TXMC639 I/O Connector.

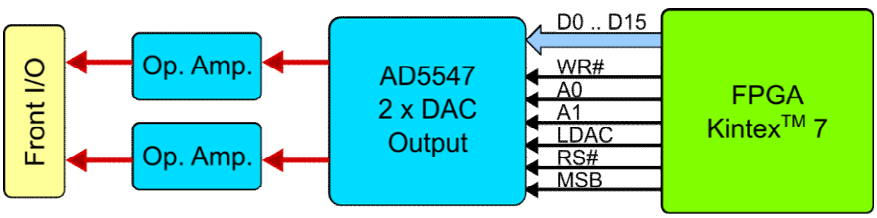


Figure 7-11 : Analog Output Section

The key-features of the TXMC639 DAC Interface are:

- 16 bit Resolution
- Built-in 4-quadrant resistors in combination with an operational amplifier allow ±10 V outputs
- Outputs Drive ±10 mA per channel
- Capacitive Load Driving = 1000 pF

7.8.2 Output Voltage Range

The output voltage ranges of the TXMC639 DAC outputs are set via BCC Register - *DAC Control / Status Register* and *DAC Output Voltage Range Register*.

There are three predefined output voltage ranges ±10 V, ±5 V, ±2,5 V and a fourth mode in which the high and low voltage range can be set individually.

For the first three predefined fixed voltage ranges, the corecture data are determined during the TEWS factory test. Determined correction values are stored in an I2C EEPROM. There are no correction values for the individually adjustable voltage range mode.

Due to tolerances of the reference voltage generation, basic tolerances of the DAC components and temperature dependence, it may happen that the extreme limits for the output voltage cannot be reached.

7.8.3 User FPGA Pinning

First DAC configuration interface is for controlling the DAC channel 0 up to 7.

Signal	Bank	VCCO	Pin	Description
DAC_D0	12	3.3 V	W20	First DAC Data Bus to DAC Device 1 .. 4 with DAC Channel 1 .. 8
DAC_D1	12	3.3 V	Y21	
DAC_D2	12	3.3 V	Y20	
DAC_D3	12	3.3 V	AA22	
DAC_D4	12	3.3 V	Y22	
DAC_D5	12	3.3 V	AB25	
DAC_D6	12	3.3 V	AB22	
DAC_D7	12	3.3 V	AB21	
DAC_D8	12	3.3 V	AC26	
DAC_D9	12	3.3 V	AC24	
DAC_D10	12	3.3 V	AC23	
DAC_D11	12	3.3 V	AD25	
DAC_D12	12	3.3 V	AD24	
DAC_D13	12	3.3 V	AD23	
DAC_D14	12	3.3 V	AC22	
DAC_D15	12	3.3 V	AC21	
DAC_ADR0	12	3.3 V	AE21	DAC Address Line to select the DAC channel A or B from one DAC Device.
DAC_'WR00_01'	12	3.3 V	AF23	A low active WR transfers data to DAC input register. One write signal for each DAC device respectively for two DAC channel.
DAC_'WR02_03'	12	3.3 V	AE23	
DAC_'WR04_05'	12	3.3 V	AF25	
DAC_'WR06_07'	12	3.3 V	AD26	
DAC_LDAC00_01	12	3.3 V	AF22	Load the DAC output register with contents of the input register. One write signal for each DAC device respectively for two DAC channel.
DAC_LDAC02_03	12	3.3 V	AE22	
DAC_LDAC04_05	12	3.3 V	AF24	
DAC_LDAC06_07	12	3.3 V	AE26	
DAC_RS#	12	3.3 V	AE25	Active low resets all 16 input and output DAC registers. Value depends on DAC_MSB line.
DAC_MSB	12	3.3 V	AD21	**MSB Power-On Reset State.** DAC_MSB = 0 corresponds to zero-scale reset; DAC_MSB = 1 corresponds to midscale reset

Table 7-9: TXCM639 parallel DAC Interface

For pin assignment, I/O standard, slew rate and driver performance please use the XDC files of the TXMC639 BRD Project.

7.8.4 Programming Hints for AD5547

TXMC639 DAC Channel write to DAC Input Register Decoding.

ADR0	'WR00_01'	'WR02_03'	'WR04_05'	'WR06_07'	DAC Channel
0	0	1	1	1	Channel 1
1	0	1	1	1	Channel 2
0	1	0	1	1	Channel 3
1	1	0	1	1	Channel 4
0	1	1	0	1	Channel 5
1	1	1	0	1	Channel 6
0	1	1	1	0	Channel 7
1	1	1	1	0	Channel 8

TXMC639 DAC Channel LOAD_DAC Register Decoding.

ADR0	'LDAC00_01'	'LDAC02_03'	'LDAC04_05'	'LDAC06_07'	DAC Channel
0	1	0	0	0	Channel 1
1	1	0	0	0	Channel 2
0	0	1	0	0	Channel 3
1	0	1	0	0	Channel 4
0	0	0	1	0	Channel 5
1	0	0	1	0	Channel 6
0	0	0	0	1	Channel 7
1	0	0	0	1	Channel 8

A detailed description of the AD5547 parallel interface and the AD5547 function please use the data sheet which describes the whole data transfer, data register and output process and all special characteristics of the DAC.

7.9 TTL I/O Interface

Each of the 32 Front I/O TTL lines are designed with a 74LVC2G241 dual buffer as an interface to the User FPGA (Kintex™ 7) pins. The logic levels of the buffers are TTL compatible, meaning that the minimum high level is 2.0 V and the maximum low level is 0.8 V. The nominal output high voltage is 3.3 V.

The buffer outputs are followed by 47 Ω serial resistors for signal integrity and safety reasons and a 4.7kΩ pull resistors. The pull resistors guaranty a TTL compatible logic level when outputs are tristate and not driven externally.

As an option the pull up voltage can be set to 5 V by an analog multiplexer to (weakly) drive a higher voltage than 3.3 V by setting the output to tristate. This means, instead of changing the logical output value (high and low), the output enable is set to logic low for an output high level or logic high to use the pull functionality. The logical output value must be logic low to ensure the low-level at the output while the buffer is active (output enable is active).

For example when connecting to a standard 5 V CMOS logic input (not TTL compatible levels), a high level of minimum 3.5 V is required.

A second option is to set the pull voltage to GND for pull-down functionality. This means, instead of changing the logical output value (high and low), the output enable is set to logical low for an output low level or logical high to drive the output high. The logical output value must be logic high to ensure the high-level at the output while the buffer is active (output enable is active).

Please note that the pull-up or pull-down resistor can only drive high impedance inputs. In low impedance input cases there is a reduced high-level voltage at the I/O pin when the output buffer sources a noticeable current to the external load while driving a high-level. There is also an increased low-level voltage at the I/O pin when the output buffer sinks a noticeable current from the external load while driving a low-level. The maximum current needs to be limited in both cases to ensure proper signal level.

A TVS array protects against ESD shocks.

See the following figure for more information of the TTL I/O circuitry.

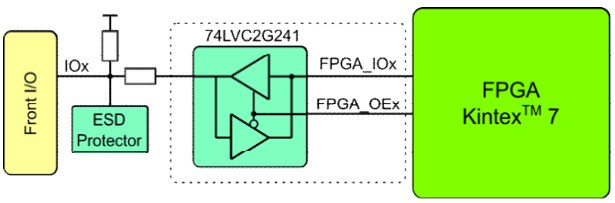


Figure 7-12 : One Channel TTL I/O Interface

Due to on placement restrictions, groups are needed for the pull voltage.

If the Pull-Resistors are set to float (possible selection), the user should keep in mind that the I/O Lines of one group are connected via their Pull-Resistors.

7.9.1 User FPGA Pinning

Signal Name	Pin Number	VCCO	Direction
TTL_IO<0>	AB24	3.3 V	IN/OUT
TTL_IO<1>	AA23	3.3 V	IN/OUT
TTL_IO<2>	Y23	3.3 V	IN/OUT
TTL_IO<3>	AA24	3.3 V	IN/OUT
TTL_IO<4>	U21	3.3 V	IN/OUT
TTL_IO<5>	V23	3.3 V	IN/OUT
TTL_IO<6>	Y26	3.3 V	IN/OUT
TTL_IO<7>	W24	3.3 V	IN/OUT
TTL_IO<8>	U17	3.3 V	IN/OUT
TTL_IO<9>	M22	3.3 V	IN/OUT
TTL_IO<10>	U24	3.3 V	IN/OUT
TTL_IO<11>	W25	3.3 V	IN/OUT
TTL_IO<12>	N18	3.3 V	IN/OUT
TTL_IO<13>	P26	3.3 V	IN/OUT
TTL_IO<14>	N24	3.3 V	IN/OUT
TTL_IO<15>	M24	3.3 V	IN/OUT
TTL_IO<16>	V21	3.3 V	IN/OUT
TTL_IO<17>	N16	3.3 V	IN/OUT
TTL_IO<18>	N26	3.3 V	IN/OUT
TTL_IO<19>	P24	3.3 V	IN/OUT
TTL_IO<20>	M26	3.3 V	IN/OUT
TTL_IO<21>	M21	3.3 V	IN/OUT
TTL_IO<22>	K25	3.3 V	IN/OUT
TTL_IO<23>	P23	3.3 V	IN/OUT
TTL_IO<24>	K26	3.3 V	IN/OUT
TTL_IO<25>	L25	3.3 V	IN/OUT
TTL_IO<26>	T17	3.3 V	IN/OUT
TTL_IO<27>	M25	3.3 V	IN/OUT
TTL_IO<28>	R23	3.3 V	IN/OUT
TTL_IO<29>	R22	3.3 V	IN/OUT
TTL_IO<30>	P21	3.3 V	IN/OUT
TTL_IO<31>	R21	3.3 V	IN/OUT
TTL_OE<0>	AA25	3.3 V	OUTPUT
TTL_OE<1>	W26	3.3 V	OUTPUT
TTL_OE<2>	W21	3.3 V	OUTPUT
TTL_OE<3>	U25	3.3 V	OUTPUT
TTL_OE<4>	U26	3.3 V	OUTPUT
TTL_OE<5>	U22	3.3 V	OUTPUT

TTL_OE<6>	Y25	3.3 V	OUTPUT
TTL_OE<7>	W23	3.3 V	OUTPUT
TTL_OE<8>	P19	3.3 V	OUTPUT
TTL_OE<9>	P25	3.3 V	OUTPUT
TTL_OE<10>	V22	3.3 V	OUTPUT
TTL_OE<11>	V26	3.3 V	OUTPUT
TTL_OE<12>	M19	3.3 V	OUTPUT
TTL_OE<13>	T20	3.3 V	OUTPUT
TTL_OE<14>	R25	3.3 V	OUTPUT
TTL_OE<15>	N21	3.3 V	OUTPUT
TTL_OE<16>	V24	3.3 V	OUTPUT
TTL_OE<17>	N19	3.3 V	OUTPUT
TTL_OE<18>	R26	3.3 V	OUTPUT
TTL_OE<19>	N23	3.3 V	OUTPUT
TTL_OE<20>	N17	3.3 V	OUTPUT
TTL_OE<21>	M20	3.3 V	OUTPUT
TTL_OE<22>	T25	3.3 V	OUTPUT
TTL_OE<23>	N22	3.3 V	OUTPUT
TTL_OE<24>	L24	3.3 V	OUTPUT
TTL_OE<25>	J25	3.3 V	OUTPUT
TTL_OE<26>	J24	3.3 V	OUTPUT
TTL_OE<27>	D24	3.3 V	OUTPUT
TTL_OE<28>	D23	3.3 V	OUTPUT
TTL_OE<29>	E23	3.3 V	OUTPUT
TTL_OE<30>	E22	3.3 V	OUTPUT
TTL_OE<31>	E21	3.3 V	OUTPUT

Table 7-10 : User FPGA TTL IO and OE Pins

For pin assignment, I/O standard, slew rate and driver performance please use the XDC files of the TXMC639 BRD Project.

7.10 RS422 Interface

The TXMC639 provides a multiplex functionality between TTL and RS422 for 16 of the 32 ESD-protected TTL lines so that 16 TTL can alternatively be 8 RS422 channels.

The 16 IO lines IO16 to IO31 become the 8 differential RS422 channels IO16_A/B to IO23_A/B.

The specification for TTL interfaces and RS422 interfaces specifies very different maximum voltage levels or common mode voltages, so this switchover requires some care.

The switching itself is done via 8 Texas Instruments TMUX1072 2-Channel 2:1 Analog Multiplexers with Overvoltage Detection and Protection. These multiplexers make simultaneous use as TTL I/O and RS422 impossible and providing an overvoltage protection to prevent the TTL buffers from being destroyed by RS422 levels.

Every Multiplexer switches two TTL pins to one differential RS422 pair.

Switching is done via the BCC Digital I/O Interface Configuration / Status Register.

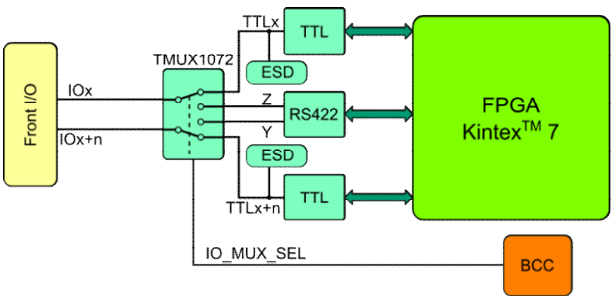


Figure 7-13 : 1 Channel Digital I/O Multiplexer Block Diagram

TTL channels 16 to 31 can be switched.

7.10.1 RS422 FPGA Interface

The Half Duplex RS485/RS422 transceiver LTC2854 from Linear technology is used an the TXMC639 for the differential I/O Interface. The transceiver is controlled via the following pins.

- RO - Receiver Output
- RE# - Receiver Enable
- DE - Driver Enable
- DI - Diver Input
- TE - Termination Enable (internal)

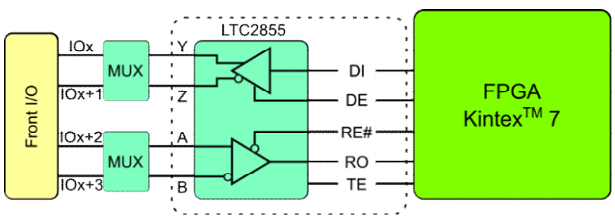


Figure 7-14 : One Channel RS422 I/O Interface

For further information, please use the LTC2854 data sheet.

7.10.2 User FPGA Pinning

Signal Name	Pin Number	VCCO	Direction
Receiver Output			
RS_RO<0>	L23	3.3 V	IN
RS_RO<1>	H24	3.3 V	IN
RS_RO<2>	F25	3.3 V	IN
RS_RO<3>	J26	3.3 V	IN
RS_RO<4>	B20	3.3 V	IN
RS_RO<5>	C21	3.3 V	IN
RS_RO<6>	C22	3.3 V	IN
RS_RO<7>	D25	3.3 V	IN
Receiver Enable			
RS_RE#<0>	L19	2.5 V	OUT
RS_RE#<1>	G20	2.5 V	OUT
RS_RE#<2>	E20	2.5 V	OUT
RS_RE#<3>	J20	2.5 V	OUT
RS_RE#<4>	A19	2.5 V	OUT
RS_RE#<5>	B19	2.5 V	OUT
RS_RE#<6>	C16	2.5 V	OUT
RS_RE#<7>	D20	2.5 V	OUT
Driver Enable			
RS_DE<0>	L20	2.5 V	OUT
RS_DE<1>	F20	2.5 V	OUT
RS_DE<2>	D15	2.5 V	OUT
RS_DE<3>	H19	2.5 V	OUT
RS_DE<4>	A18	2.5 V	OUT
RS_DE<5>	B17	2.5 V	OUT
RS_DE<6>	C17	2.5 V	OUT
RS_DE<7>	D19	2.5 V	OUT
Diver Input			
RS_DI<0>	K20	2.5 V	OUT
RS_DI<1>	F19	2.5 V	OUT
RS_DI<2>	D16	2.5 V	OUT
RS_DI<3>	G19	2.5 V	OUT
RS_DI<4>	A17	2.5 V	OUT
RS_DI<5>	B16	2.5 V	OUT
RS_DI<6>	C18	2.5 V	OUT

RS_DI<7>	C19	2.5 V	OUT

Termination Enable			
RS_TE<0>	K23	3.3 V	OUT
RS_TE<1>	H23	3.3 V	OUT
RS_TE<2>	E26	3.3 V	OUT
RS_TE<3>	H26	3.3 V	OUT
RS_TE<4>	A20	3.3 V	OUT
RS_TE<5>	B21	3.3 V	OUT
RS_TE<6>	C24	3.3 V	OUT
RS_TE<7>	D21	3.3 V	OUT

Table 7-11 : User FPGA RS422 Interface Pins

For pin assignment, I/O standard, slew rate and driver performance please use the XDC files of the TXMC639 BRD Project.

7.11 I/O Pull Configuration

Each TTL I/O Line has a 4k7 Pull-Resistor. The 32 I/O Lines are arranged in two groups which can be configured for 3.3 V pull-up, 5 V pull-up or pull-down. In addition, the Pull-Resistors can float.

If the Pull-Resistors float, the user should keep in mind that the 16 I/O Lines of each group are connected via their Pull-Resistors to the others in the group.

The I/O Pull configuration can be done via the User FPGA or the BCC. The normal behaviour is that the User FPGA firmware controls the I/O Pull Configuration depending on the User FPGA I/O functionality.

The User FPGA IO_PULL Interface configuration signals are connected to two analog multiplexers via the BCC. With these multiplexers, the desired pull resistor reference can be adjusted directly from the User FPGA. There are four I/O lines in total for controlling the two analog multiplexer regarding the I/O Pull Voltage.

CNT **Lines**	**concerns I/O Lines**	**Description**
PULL_1_GRP [1:0]	TTL_IO[16:31]	0b11 : pull-down 0b10 : pull-up to 3.3 V 0b01 : pull-up to 5 V 0b00 : No pull-up or pull-down (default)
PULL_0_GRP[1:0]	TTL_IO[0 :15]	

Table 7-12: I/O Pull Configuration

Signal Name	**Pin Number**	**Direction**	**VCCO**
PULL_0_GRP<0>	D8	OUT	3.3 V
PULL_0_GRP<1>	D7	OUT	3.3 V
PULL_1_GRP<0>	E8	OUT	3.3 V
PULL_1_GRP<1>	C7	OUT	3.3 V

Table 7-13 : User FPGA Pins

For pin assignment, I/O standard, slew rate and driver performance please use the XDC files of the TXMC639 BRD Project.

The BCC offers an additional option for setting the I/O Pull voltage. Through its Digital I/O Interface Configuration / Status Register the User FPGA control can be revoked or rather dominated. (Use this Register to set the desired pull resistor reference.)

7.12 Memory

The TXMC639 is equipped with a 1 GB, 32 bit wide DDR3 SDRAM and a 128 Mbit non-volatile SPI-Flash. The SPI-Flash can also be used as the User FPGA configuration memory.

7.12.1 DDR3 SDRAM

The TXMC639 provides one MT41… (96-ball) DDR3 memory devices. The memory is accessible through a Memory Interface Controller Block IP in bank 33 and 34 of the User FPGA.

Signal	FPGA Pin Number	Termination	Memory Devices	
			Pin	Name
A0	AE12	49.9 Ω VTT	N3	A0
A1	AA7	49.9 Ω VTT	P7	A1
A2	AA8	49.9 Ω VTT	P3	A2
A3	W11	49.9 Ω VTT	N2	A3
A4	AB9	49.9 Ω VTT	P8	A4
A5	W8	49.9 Ω VTT	P2	A5
A6	Y11	49.9 Ω VTT	R8	A6
A7	Y12	49.9 Ω VTT	R2	A7
A8	AF13	49.9 Ω VTT	T8	A8
A9	AA9	49.9 Ω VTT	R3	A9
A10	AB7	49.9 Ω VTT	L7	A10
A11	AD11	49.9 Ω VTT	R7	A11
A12	AB12	49.9 Ω VTT	N7	A12
A13	AA12	49.9 Ω VTT	T3	NC/A13
A14	AC12	49.9 Ω VTT	T7	NC/A14
BA0	AD13	49.9 Ω VTT	M2	BA0
BA1	V9	49.9 Ω VTT	N8	BA1
BA2	AD10	49.9 Ω VTT	M3	BA2
RAS#	AE7	49.9 Ω VTT	J3	RAS#
CAS#	AE13	49.9 Ω VTT	K3	CAS#
WE#	AF7	49.9 Ω VTT	L3	WE#
RESET#	AA2	4.7 kΩ GND	T2	RESET#
CKE	AC7	4.7 kΩ GND	K9	CKE
ODT	V11	4.7 kΩ GND	K1	ODT
CS#	AC13	49.9 Ω VTT	L2	CS#
DM_0	Y3	ODT	E7	LDM
DM_1	V4	ODT	D3	UDM
DM_2	AA4	ODT	E7	LDM
DM_3	AE5	ODT	D3	UDM
DQ0	AA3	ODT	E3	DQ0
DQ1	Y1	ODT	F7	DQ1
DQ2	AB2	ODT	F2	DQ2

Signal	FPGA Pin Number	Termination	Memory Devices	
			Pin	Name
DQ3	V1	ODT	F8	DQ3
DQ4	Y2	ODT	H3	DQ4
DQ5	V2	ODT	H8	DQ5
DQ6	AC2	ODT	G2	DQ6
DQ7	W1	ODT	H7	DQ7
DQ8	W3	ODT	D7	DQ8
DQ9	V6	ODT	C3	DQ9
DQ10	V3	ODT	C8	DQ10
DQ11	U5	ODT	C2	DQ11
DQ12	U1	ODT	A7	DQ12
DQ13	U7	ODT	A2	DQ13
DQ14	U2	ODT	B8	DQ14
DQ15	U6	ODT	A3	DQ15
DQ16	AD6	ODT	E3	DQ0
DQ17	AC4	ODT	F7	DQ1
DQ18	Y6	ODT	F2	DQ2
DQ19	AC3	ODT	F8	DQ3
DQ20	AC6	ODT	H3	DQ4
DQ21	AB4	ODT	H8	DQ5
DQ22	Y5	ODT	G2	DQ6
DQ23	AB6	ODT	H7	DQ7
DQ24	AD4	ODT	D7	DQ8
DQ25	AF2	ODT	C3	DQ9
DQ26	AF3	ODT	C8	DQ10
DQ27	AE6	ODT	C2	DQ11
DQ28	AE2	ODT	A7	DQ12
DQ29	AD1	ODT	A2	DQ13
DQ30	AE3	ODT	B8	DQ14
DQ31	AE1	ODT	A3	DQ15
CK_±	W10 / W9	100 Ω	J7 / K7	CK / CK#
DQS_0±	AB1 / AC1	ODT	F3 / G3	LDQS±
DQS_1±	W6 / W5	ODT	C7 / B7	UDQS±
DQS_2±	AA5 / AB5	ODT	F3 / G3	LDQS±
DQS_3±	AF5 / AF4	ODT	C7 / B7	UDQS±

Table 7-14 : DDR3 SDRAM Interface

DDR3 Memory Device 01
DDR3 Memory Device 02
Both DDR3 Memory Devices 01 & 02

For pin assignment, I/O standard, slew rate and driver performance please use the XDC files of the TXMC639 BRD Project.

For details regarding the DDR3 SDRAM interface, please refer to AMD Memory Interface Generator Documentation. AMD UG586: *Zynq-7000 AP SoC and 7 Series Devices Memory Interface Solutions v4.2*.

7.12.2 SPI-Flash

The TXMC639 provides a Micron MT25QL128ABA 128 Mbit serial Flash memory. This Flash is used as FPGA configuration source (default configuration source).

After configuration, it is always accessible from the FPGA, so it also can be used for code or user data storage.

The SPI-EEPROM is connected via Quad (x4) SPI interface to the User FPGA (Kintex™ 7) configuration interface.

SPI-PROM Signal	Bank	V_{CCO}	Pin	Description / Kintex™ 7
CLK	0	3.3 V	C8	Serial Clock (CCLK_B)
CS#	14	3.3 V	C23	Chip Select (FCS_B)
DI (bit0)	14	3.3 V	B24	Serial Data input (MOSI) / MISO[0]
DO (bit1)	14	3.3 V	A25	Serial Data output (DIN) / MISO[1]
WP# (bit2)	14	3.3 V	B22	MISO[2] – D02
HOLD# (bit3)	14	3.3 V	A22	MISO[3] – D03

Table 7-15 : FPGA SPI-Flash Connections

For pin assignment, I/O standard, slew rate and driver performance please use the XDC files of the TXMC639 BRD Project.

7.12.3 I2C - EEPROM

The TXMC639 provides an STMicroelectronics M24128 (128 Kbit) I2C-Compatible (2-wire) Serial EEPROM.

This EEPROM is used as ADC and DAC correction data memory. In addition, for each correction data set ADC Input and DAC Output the corresponding voltage range of ADC inputs and DAC outputs are also stored.

During factory test the analog input and output channel gain error and offset error are determined. For each device, 16 bit correction values are stored to the I2C EEPROM. These correction values have been determined with TEWS test environment. If system specific correction values are needed, the determination of the correcture values of the entire system can be done by the user and the I2C EEPROM could be used as a possible memory to store the custom correction values.

The I2C EEPROM is connected via 2-wire interface to User FPGA (Kintex™ 7). As usual for the I2C interface the two pins must be realized as open drain buffers.

SPI-PROM Signal	Bank	V_{CCO}	Pin	Description / Kintex™ 7
USER_SCL	13	3.3 V	P16	Serial clock
USER_SDA	13	3.3 V	R16	Serial data

Table 7-16: FPGA I2C EEPROM Connections

For using the serial I2C interface between the USER FPGA (Kintex™ 7) and the I2C EEPROM please see the STMicroelectronics M24128 data sheet which describes the serial communication process.

For pin assignment, I/O standard, slew rate and driver performance please use the XDC files of the TXMC639 BRD Project.

7.12.3.1 ADC and DAC Ccorrectable Errors

There are two errors affecting the accuracy of the ADC and DAC that can be corrected using the factory determined correction values. The correction values are obtained during factory test and are stored in an on-board I2C EEPROM as 2-complement 16 bit values in the range from -32768 to +32767. To achieve a higher accuracy, they are scaled to ¼ LSB.

DAC Offset Error:

For the DAC, this is the data value that is required to produce a zero voltage output signal. This error is corrected by subtracting the offset from the DAC data value.

ADC Offset Error:

The offset error is the data value when converting with the input connected to its own ground in single-ended mode, or with shorted inputs in differential mode. This error is corrected by subtracting the known error from the reading.

DAC Gain Error:

The gain error is the difference between the ideal gain and the actual gain of the DAC. It is corrected by multiplying the DAC data value with a correction factor.

ADC Gain Error:

The gain error is the difference between the ideal gain and the actual gain of the programmable gain amplifier and the ADC. This error is corrected by multiplying the reading with a correction factor.

7.12.3.2 ADC Correction Values

The 16 ADC channels are realized with two octal LTC2320-16 ADC devices.

For each ADC channel and all three input voltage ranges a 16 bit Offset correction and a 16 bit gain correction value is stored.

I2C EEPROM Address	Description	Size (bit)
ADC Range 0		
0x000	ADC Channel 0, $Offset_{Corr}$ High Byte	8
0x001	ADC Channel 0, $Offset_{Corr}$ Low Byte	8
0x002	ADC Corretion 0, $Gain_{Corr}$ High Byte	8
0x003	ADC Corretion 0, $Gain_{Corr}$ Low Byte	8
0x004	ADC Channel 1, $Offset_{Corr}$ High Byte	8
0x005	ADC Channel 1, $Offset_{Corr}$ Low Byte	8
0x006	ADC Corretion 1, $Gain_{Corr}$ High Byte	8
0x007	ADC Corretion 1, $Gain_{Corr}$ Low Byte	8
. . .		
0x03C	ADC Channel 15, $Offset_{Corr}$ High Byte	8
0x03D	ADC Channel 15, $Offset_{Corr}$ Low Byte	8
0x03E	ADC Corretion 15, $Gain_{Corr}$ High Byte	8
0x03F	ADC Corretion 15, $Gain_{Corr}$ Low Byte	8
0x040 .. 0x07E	Reserved	512
ADC Range 1		

0x080	ADC Channel 0, $Offset_{Corr}$ High Byte	8
0x081	ADC Channel 0, $Offset_{Corr}$ Low Byte	8
0x082	ADC Corretion 0, $Gain_{Corr}$ High Byte	8
0x083	ADC Corretion 0, $Gain_{Corr}$ Low Byte	8
0x084	ADC Channel 1, $Offset_{Corr}$ High Byte	8
0x085	ADC Channel 1, $Offset_{Corr}$ Low Byte	8
0x086	ADC Corretion 1, $Gain_{Corr}$ High Byte	8
0x087	ADC Corretion 1, $Gain_{Corr}$ Low Byte	8
…		
0x0BC	ADC Channel 15, $Offset_{Corr}$ High Byte	8
0xBD	ADC Channel 15, $Offset_{Corr}$ Low Byte	8
0x0BE	ADC Corretion 15, $Gain_{Corr}$ High Byte	8
0x0BF	ADC Corretion 15, $Gain_{Corr}$ Low Byte	8
0x0C0 .. 0x0FE	Reserved	512
ADC Range 2		
0x100	ADC Channel 0, $Offset_{Corr}$ High Byte	8
0x101	ADC Channel 0, $Offset_{Corr}$ Low Byte	8
0x102	ADC Corretion 0, $Gain_{Corr}$ High Byte	8
0x103	ADC Corretion 0, $Gain_{Corr}$ Low Byte	8
0x104	ADC Channel 1, $Offset_{Corr}$ High Byte	8
0x105	ADC Channel 1, $Offset_{Corr}$ Low Byte	8
0x106	ADC Corretion 1, $Gain_{Corr}$ High Byte	8
0x107	ADC Corretion 1, $Gain_{Corr}$ Low Byte	8
…		
0x13C	ADC Channel 15, $Offset_{Corr}$ High Byte	8
0x13D	ADC Channel 15, $Offset_{Corr}$ Low Byte	8
0x13E	ADC Corretion 15, $Gain_{Corr}$ High Byte	8
0x13F	ADC Corretion 15, $Gain_{Corr}$ Low Byte	8
0x140 .. 0x67F	Reserved	512

Table 7-17: ADC Correction Values

7.12.3.3 DAC Corretion Values

The 8 DAC channels are realized with eight dual AD5547 DAC devices.

For each DAC channel three correction value sets are stored. One set for each DAC Output Voltage Range Selection (±10V range (default value), ±5V range and ±2.5V range).
Each correction value set consists of a 16 bit value for Offset correction and Gain correction for each channel.

I2C EEPROM Address	Description	Size (bit)
DAC Range 0		
0x680	DAC Range 0 Channel 0 $Offset_{corr}$ High Byte	8
0x681	DAC Range 0 Channel 0 $Offset_{corr}$ Low Byte	8
0x682	DAC Range 0 Channel 0 $Gain_{corr}$ High Byte	8
0x683	DAC Range 0 Channel 0 $Gain_{corr}$ Low Byte	8
0x684	DAC Range 0 Channel 1 $Offset_{corr}$ High Byte	8
0x685	DAC Range 0 Channel 1 $Offset_{co}$ Low Byte	8
0x686	DAC Range 0 Channel 1 $Gain_{corr}$ High Byte	8
0x0687	DAC Range 0 Channel 1 $Gain_{corr}$ Low Byte	8
…		
0x69C	DAC Range 0 Channel 7 $Offset_{corr}$ High Byte	8
0x69E	DAC Range 0 Channel 7 $Offset_{corr}$ Low Byte	8
0x69E	DAC Range 0 Channel 7 $Gain_{corr}$ High Byte	8
0x69F	DAC Range 0 Channel 7 $Gain_{corr}$ Low Byte	8
0x6A0 .. 0x6BE	Reserved	256
DAC Range 1		
0x6C0	DAC Range 1 Channel 0 $Offset_{corr}$ High Byte	8
0x6C1	DAC Range 1 Channel 0 $Offset_{corr}$ Low Byte	8
0x6C2	DAC Range 1 Channel 0 $Gain_{corr}$ High Byte	8
0x6C3	DAC Range 1 Channel 0 $Gain_{corr}$ Low Byte	8
0x6C4	DAC Range 1 Channel 1 $Offset_{corr}$ High Byte	8
0x6C5	DAC Range 1 Channel 1 $Offset_{corr}$ Low Byte	8
0x6C6	DAC Range 1 Channel 1 $Gain_{corr}$ High Byte	8
0x6C7	DAC Range 1 Channel 1 $Gain_{corr}$ Low Byte	8
…		
0x6DC	DAC Range 1 Channel 7 $Offset_{corr}$ High Byte	8
0x6CD	DAC Range 1 Channel 7 $Offset_{corr}$ Low Byte	8
0x6DE	DAC Range 1 Channel 7 $Gain_{corr}$ High Byte	8
0x6CF	DAC Range 1 Channel 7 $Gain_{corr}$ Low Byte	8
0x6E0 .. 0x6FE	Reserved	256
DAC Range 2		
0x700	DAC Range 2 Channel 0 $Offset_{corr}$ High Byte	8
0x701	DAC Range 2 Channel 0 $Offset_{corr}$ Low Byte	8
0x702	DAC Range 2 Channel 0 $Gain_{corr}$ High Byte	8

0x703	DAC Range 2 Channel 0 $Gain_{corr}$ Low Byte	8
0x704	DAC Range 2 Channel 1 $Offset_{corr}$ High Byte	8
0x705	DAC Range 2 Channel 1 $Offset_{corr}$ Low Byte	8
0x706	DAC Range 2 Channel 1 $Gain_{corr}$ High Byte	8
0x707	DAC Range 2 Channel 1 $Gain_{corr}$ Low Byte	8
…		
0x71C	DAC Range 2 Channel 7 $Offset_{corr}$ High Byte	8
0x71D	DAC Range 2 Channel 7 $Offset_{corr}$ Low Byte	8
0x71E	DAC Range 2 Channel 7 $Offset_{corr}$ High Byte	8
0x71F	DAC Range 2 Channel 7 $Offset_{corr}$ Low Byte	8
0x720 .. 0x73E	Reserved	256

Table 7-18: DAC Correction Data Values

7.12.3.4 ADC Data Correction Formula

Please use the total 16 bit data register value for the ADC correction formula.

The basic formula for correcting any ADC reading for the TXMC639 (bipolar input voltage range) is:

$$Value = Reading \cdot \left(1 - \frac{Gain_{corr}}{131072}\right) - \frac{Offset_{corr}}{4}$$

Value is the corrected result.

Reading is the data read from the ADC Data Register.

$Gain_{corr}$ and $Offset_{corr}$ are the ADC correction factors from the Correction Data ROM stored for each programmable gain factor.

The correction values are stored as two's complement 16 bit values in the range -32768 to 32767. For higher accuracy they are scaled to ¼ LSB.

Floating point arithmetic or scaled integer arithmetic is necessary to avoid rounding error while computing above formula.

7.12.3.5 DAC Data Correction Formula

The basic formula for correcting any DAC value is:

$$Data = Value \cdot \left(1 - \frac{Gain_{corr}}{131072}\right) - \frac{Offset_{corr}}{4}$$

Value is the desired DAC value.

Data is the corrected DAC value that must be sending to the DAC.

$Gain_{corr}$ and $Offset_{corr}$ are the DAC correction values from the Correction Data ROM. They are stored separately for each of the 8 DAC channels.

The correction values are stored as two's complement byte wide values in the range from –32768 to +32767. For higher accuracy they are scaled to ¼ LSB.

Floating point arithmetic or scaled integer arithmetic must be used to avoid rounding errors in computing above formula.

7.12.3.6 DAC and ADC voltage ranges

The voltage range for each DAC output and ADC input is composed of two bytes, one high byte and one low byte. Together they provide the 16 bit voltage range in mV.

I2C EEPROM Address	Description	Size (bit)
0x740	DAC Output Range 0, Channel 0 High Byte	8
0x741	DAC Output Range 0, Channel 0 Low Byte	8
0x742	DAC Output Range 0, Channel 1 High Byte	8
0x743	DAC Output Range 0, Channel 1 Low Byte	8
0x744	DAC Output Range 0, Channel 2 High Byte	8
0x745	DAC Output Range 0, Channel 2 Low Byte	8
0x746	DAC Output Range 0, Channel 3 High Byte	8
0x747	DAC Output Range 0, Channel 3 Low Byte	8
0x748	DAC Output Range 0, Channel 4 High Byte	8
0x749	DAC Output Range 0, Channel 4 Low Byte	8
0x74A	DAC Output Range 0, Channel 5 High Byte	8
0x74B	DAC Output Range 0, Channel 5 Low Byte	8
0x74C	DAC Output Range 0, Channel 6 High Byte	8
0x74D	DAC Output Range 0, Channel 6 Low Byte	8
0x74E	DAC Output Range 0, Channel 7 High Byte	8
0x74F	DAC Output Range 0, Channel 7 Low Byte	8
0x750 .. 0x75F	Reserved	128
0x760	DAC Output Range 1, Channel 0 High Byte	8
0x761	DAC Output Range 1, Channel 0 Low Byte	8
0x762	DAC Output Range 1, Channel 1 High Byte	8
0x763	DAC Output Range 1, Channel 1 Low Byte	8
0x764	DAC Output Range 1, Channel 2 High Byte	8
0x765	DAC Output Range 1, Channel 2 Low Byte	8
0x766	DAC Output Range 1, Channel 3 High Byte	8
0x767	DAC Output Range 1, Channel 3 Low Byte	8
0x768	DAC Output Range 1, Channel 4 High Byte	8
0x769	DAC Output Range 1, Channel 4 Low Byte	8
0x76A	DAC Output Range 1, Channel 5 High Byte	8
0x76B	DAC Output Range 1, Channel 5 Low Byte	8
0x76C	DAC Output Range 1, Channel 6 High Byte	8
0x76D	DAC Output Range 1, Channel 6 Low Byte	8
0x76E	DAC Output Range 1, Channel 7 High Byte	8
0x76F	DAC Output Range 1, Channel 7 Low Byte	8
0x770 .. 0x77F	Reserved	128
0x780	DAC Output Range 2, Channel 0 High Byte	8
0x781	DAC Output Range 2, Channel 0 Low Byte	8

0x782	DAC Output Range 2, Channel 1 High Byte	8
0x783	DAC Output Range 2, Channel 1 Low Byte	8
0x784	DAC Output Range 2, Channel 2 High Byte	8
0x785	DAC Output Range 2, Channel 2 Low Byte	8
0x786	DAC Output Range 2, Channel 3 High Byte	8
0x787	DAC Output Range 2, Channel 3 Low Byte	8
0x788	DAC Output Range 2, Channel 4 High Byte	8
0x789	DAC Output Range 2, Channel 4 Low Byte	8
0x78A	DAC Output Range 2, Channel 5 High Byte	8
0x78B	DAC Output Range 2, Channel 5 Low Byte	8
0x78C	DAC Output Range 2, Channel 6 High Byte	8
0x78D	DAC Output Range 2, Channel 6 Low Byte	8
0x78E	DAC Output Range 2, Channel 7 High Byte	8
0x78F	DAC Output Range 2, Channel 7 Low Byte	8
0x790 .. 0x79F	Reserved	128
0x7A0	ACD Input Voltage Range 0, Channel 0 + 1 High Byte	8
0x7A1	ACD Input Voltage Range 0, Channel 0 + 1 Low Byte	8
0x7A2	ACD Input Voltage Range 0, Channel 2 + 3 High Byte	8
0x7A3	ACD Input Voltage Range 0, Channel 2 + 3 Low Byte	8
0x7A4	ACD Input Voltage Range 0, Channel 4 + 5 High Byte	8
0x7A5	ACD Input Voltage Range 0, Channel 4 + 5 Low Byte	8
0x7A6	ACD Input Voltage Range 0, Channel 6 + 7 High Byte	8
0x7A7	ACD Input Voltage Range 0, Channel 6 + 7 Low Byte	8
0x7A8	ACD Input Voltage Range 0, Channel 8 + 9 High Byte	8
0x7A9	ACD Input Voltage Range 0, Channel 8 + 9 Low Byte	8
0x7AA	ACD Input Voltage Range 0, Channel 10 + 11 High Byte	8
0x7AB	ACD Input Voltage Range 0, Channel 10 + 11 Low Byte	8
0x7AC	ACD Input Voltage Range 0, Channel 12 + 13 High Byte	8
0x7AD	ACD Input Voltage Range 0, Channel 12 + 13 Low Byte	8
0x7AE	ACD Input Voltage Range 0, Channel 14 + 15 High Byte	8
0x7AF	ACD Input Voltage Range 0, Channel 14 + 15 Low Byte	8
0x7B0 .. 0x7BF	Reserved	128
0x7C0	ACD Input Voltage Range 1, Channel 0 + 1 High Byte	8
0x7C1	ACD Input Voltage Range 1, Channel 0 + 1 Low Byte	8
0x7C2	ACD Input Voltage Range 1, Channel 2 + 3 High Byte	8
0x7C3	ACD Input Voltage Range 1, Channel 2 + 3 Low Byte	8
0x7C4	ACD Input Voltage Range 1, Channel 4 + 5 High Byte	8
0x7C5	ACD Input Voltage Range 1, Channel 4 + 5 Low Byte	8
0x7C6	ACD Input Voltage Range 1, Channel 6 + 7 High Byte	8
0x7C7	ACD Input Voltage Range 1, Channel 6 + 7 Low Byte	8
0x7C8	ACD Input Voltage Range 1, Channel 8 + 9 High Byte	8

0x7C9	ACD Input Voltage Range 1, Channel 8 + 9 Low Byte	8
0x7CA	ACD Input Voltage Range 1, Channel 10 + 11 High Byte	8
0x7CB	ACD Input Voltage Range 1, Channel 10 + 11 Low Byte	8
0x7CC	ACD Input Voltage Range 1, Channel 12 + 13 High Byte	8
0x7CD	ACD Input Voltage Range 1, Channel 12 + 13 Low Byte	8
0x7CE	ACD Input Voltage Range 1, Channel 14 + 15 High Byte	8
0x7CF	ACD Input Voltage Range 1, Channel 14 + 15 Low Byte	8
0x7D0 .. 0x7DF	Reserved	128
0x7E0	ACD Input Voltage Range 2, Channel 0 + 1 High Byte	8
0x7E1	ACD Input Voltage Range 2, Channel 0 + 1 Low Byte	8
0x7E2	ACD Input Voltage Range 2, Channel 2 + 3 High Byte	8
0x7E3	ACD Input Voltage Range 2, Channel 2 + 3 Low Byte	8
0x7E4	ACD Input Voltage Range 2, Channel 4 + 5 High Byte	8
0x7E5	ACD Input Voltage Range 2, Channel 4 + 5 Low Byte	8
0x7E6	ACD Input Voltage Range 2, Channel 6 + 7 High Byte	8
0x7E7	ACD Input Voltage Range 2, Channel 6 + 7 Low Byte	8
0x7E8	ACD Input Voltage Range 2, Channel 8 + 9 High Byte	8
0x7E9	ACD Input Voltage Range 2, Channel 8 + 9 Low Byte	8
0x7EA	ACD Input Voltage Range 2, Channel 10 + 11 High Byte	8
0x7EB	ACD Input Voltage Range 2, Channel 10 + 11 Low Byte	8
0x7EC	ACD Input Voltage Range 2, Channel 12 + 13 High Byte	8
0x7ED	ACD Input Voltage Range 2, Channel 12 + 13 Low Byte	8
0x7EE	ACD Input Voltage Range 2, Channel 14 + 15 High Byte	8
0x7EF	ACD Input Voltage Range 2, Channel 14 + 15 Low Byte	8
0x790 .. 0x7FE	Reserved	120

Table 7-19: ADC and DAC voltage ranges

7.12.3.7 Version of EEPROM data structure

In the first versions of TXMC639 only the correction data were stored. A version register is used to identify whether the voltage ranges are also present.

I2C EEPROM Address	Description	Size (bit)
0x7FF	EEPROM data structure Version 0x00: Only the ADC and DAC correction data are available. 0x01: ADC and DAC correction data and voltage range data are available.	8

Table 7-20: Version of EEPROM data structure

7.13 Rear I/O Interface

The Rear I/O Pins of the TXMC639 are directly routed to the User FPGA (Kintex™ 7). The I/O functions of these FPGA pins are directly dependent on the configuration of the FPGA.

The Kintex™ 7 VCCO voltage is set to 2.5 V, so only the 2.5 V I/O standards LVCMOS25, LVTTL25 and LVDS_25 are possible when using the TXMC639 rear I/O interface.

Signal Name	Pin Number	Direction	IO Standard for BRD
REAR_IO0-	C11	IN/OUT	LVDS_25
REAR_IO0+	C12	IN/OUT	LVDS_25
REAR_IO1-	D11	IN/OUT	LVDS_25
REAR_IO1+	E11	IN/OUT	LVDS_25
REAR_IO2-	A8	IN/OUT	LVDS_25
REAR_IO2+	A9	IN/OUT	LVDS_25
REAR_IO3-	A10	IN/OUT	LVDS_25
REAR_IO3+	B10	IN/OUT	LVDS_25
REAR_IO4-	A12	IN/OUT	LVDS_25
REAR_IO4+	A13	IN/OUT	LVDS_25
REAR_IO5-	A14	IN/OUT	LVDS_25
REAR_IO5+	B14	IN/OUT	LVDS_25
REAR_IO6-	A15	IN/OUT	LVDS_25
REAR_IO6+	B15	IN/OUT	LVDS_25
REAR_IO7-	B9	IN/OUT	LVDS_25
REAR_IO7+	C9	IN/OUT	LVDS_25
REAR_IO8-	D10	IN/OUT	LVDS_25
REAR_IO8+	E10	IN/OUT	LVDS_25
REAR_IO9-	F12	IN/OUT	LVDS_25
REAR_IO9+	G12	IN/OUT	LVDS_25
REAR_IO10-	F10	IN/OUT	LVDS_25
REAR_IO10+	G11	IN/OUT	LVDS_25
REAR_IO11-	F8	IN/OUT	LVDS_25
REAR_IO11+	F9	IN/OUT	LVDS_25
REAR_IO12-	G9	IN/OUT	LVDS_25
REAR_IO12+	G10	IN/OUT	LVDS_25
REAR_IO13-	E16	IN/OUT	LVDS_25
REAR_IO13+	E15	IN/OUT	LVDS_25
REAR_IO14-	C13	IN/OUT	LVDS_25
REAR_IO14+	C14	IN/OUT	LVDS_25
REAR_IO15-	D13	IN/OUT	LVDS_25
REAR_IO15+	D14	IN/OUT	LVDS_25

REAR_IO16-	B11	IN/OUT	LVDS_25
REAR_IO16+	B12	IN/OUT	LVDS_25
REAR_IO17-	E12	IN/OUT	LVDS_25
REAR_IO17+	E13	IN/OUT	LVDS_25
REAR_IO18-	F13	IN/OUT	LVDS_25
REAR_IO18+	F14	IN/OUT	LVDS_25
REAR_IO19-	D8	IN/OUT	LVDS_25
REAR_IO19+	D9	IN/OUT	LVDS_25
REAR_IO20-	J10	IN/OUT	LVDS_25
REAR_IO20+	J11	IN/OUT	LVDS_25
REAR_IO21-	H8	IN/OUT	LVDS_25
REAR_IO21+	H9	IN/OUT	LVDS_25
REAR_IO22-	H11	IN/OUT	LVDS_25
REAR_IO22+	H12	IN/OUT	LVDS_25
REAR_IO23-	G14	IN/OUT	LVDS_25
REAR_IO23+	H14	IN/OUT	LVDS_25
REAR_IO24-	H13	IN/OUT	LVDS_25
REAR_IO24+	J13	IN/OUT	LVDS_25
REAR_IO25-	F15	IN/OUT	LVDS_25
REAR_IO25+	G15	IN/OUT	LVDS_25
REAR_IO26-	G16	IN/OUT	LVDS_25
REAR_IO26+	H16	IN/OUT	LVDS_25
REAR_IO27-	J16	IN/OUT	LVDS_25
REAR_IO27+	J15	IN/OUT	LVDS_25
REAR_IO28-	K17	IN/OUT	LVDS_25
REAR_IO28+	K16	IN/OUT	LVDS_25
REAR_IO29-	J19	IN/OUT	LVDS_25
REAR_IO29+	J18	IN/OUT	LVDS_25
REAR_IO30-	K18	IN/OUT	LVDS_25
REAR_IO30+	L17	IN/OUT	LVDS_25
REAR_IO31-	L18	IN/OUT	LVDS_25
REAR_IO31+	M17	IN/OUT	LVDS_25

Table 7-21 : Digital Rear I/O Interface

For pin assignment, I/O standard, slew rate and driver performance please use the XDC files of the TXMC639 BRD Project.

7.14 Digital Interface to XMC P16 Connector

Eight additional Pins of the TXMC639 User FPGA (Kintex™ 7) are directly routed to the XMC P16 rear I/O connector. The I/O functions of these FPGA pins are directly dependent on the configuration of the User FPGA.

The Kintex™ 7 VCCO voltage for these pins is set to 2.5 V, so only the 2.5 V I/O standards LVCMOS25, LVTTL25 and LVDS25 are possible when using this TXMC639 XMC P16 Rear I/O interface.

Signal Name	Bank	VCCO	Pin	IO Standard for example
DIG_IO_00-	15	2.5 V	H18	LVDS25
DIG_IO_00+	15		H17	LVDS25
DIG_IO_01-	15		F18	LVDS25
DIG_IO_01+	15		G17	LVDS25
DIG_IO_02-	15		E17	LVDS25
DIG_IO_02+	15		F17	LVDS25
DIG_IO_03-	15		D18	LVDS25
DIG_IO_03+	15		E18	LVDS25

Table 7-22 : XMC P16 digital I/O Interface

For pin assignment, I/O standard, slew rate and driver performance please use the XDC files of the TXMC639 BRD Project.

For the pin assignment at the XMC P16 connector see chapter I/O Description.

7.15 JTAG Controller to User FPGA JTAG Interface

The BCC provides two methods for accessing the User FPGA via JTAG: bit-I/O and Vector-I/O.

7.15.1 Bit-IO

The bit-I/O Interface is a bit-centric interface that allows stimulating the JTAG interface by setting and reading each line (TCK, TMS, TDI and TDO) of the JTAG interface independently.

All bit-I/O register bits (JTAG_BIO_*) are directly linked/connected to the BCC JTAG Interface. If the bit-I/O Interface is enabled (JTAG_BIO_EN = 1), these bits drive the corresponding JTAG lines.

Note that the flexibility comes along with a higher I/O effort since every signal constellation must be set and emitted on the JTAG interface via a TCK high and low sequence with separated register accesses.

7.15.2 Vector-IO

The Vector-I/O Interface focuses on a high abstract level where operations are performed semi-automatically based on vectors and transfer lengths.

Via the register interface TMS (JTAG_VIO_TMS_DATA) and TDI data (JTAG_VIO_TDI_DATA) vectors are defined that shall be shifted-out onto the JTAG interface. These vectors are coupled in a way that the data (bit-information) is shifted-out at the same time.

Note that bit #0 is the first one that appears on the JTAG interface.

Shift operations require the transfer length (JTAG_VIO_XFER_LEN) information. The value has to be set in accordance to the size of the TMS/TDI data vectors or TDO read size and defines the number of transfer cycles or rather the number of TCK cycles (rising and falling edges with 50% duty factor) occurring on the JTAG interface.
The actual TCK I/O clock rate is adjustable (JTAG_VIO_TCK_CLK_DIV).

If the Vector-I/O Interface is enabled (JTAG_VIO_EN = 1) and while the Vector-I/O Controller is idle (JTAG_VIO_CTRL_STAT = 0b01), write (JTAG_VIO_SHIFT_REQ) or read (JTAG_VIO_GET_REQ) operations can be initiated. Requests initiated while the Vector-I/O Controller is not idle are lost.

Note that there is no check regarding the number of bits shifted-out or read-in. Hence illegal data can be shifted-out or read-in if the transfer length is not set appropriately.

bits of the output data vectors are aligned to the beginning of a TCK cycle and are hence updated after a falling edge. If more data is shifted-out than defined, zero bits (‘0’) are transferred, which is useful in JTAG IR- or DR-Shift States.
Data is read-in with every rising edge during shift-out and get-requests. This also allows obtaining the bit-information provided in response of a TMS/TDI operation.

Read-in updates appear immediately on the JTAG Vector-I/O TDO data vector (JTAG_VIO_TDO_DATA).

Note that bit #0 is the last one that has been read-in from the JTAG interface.

7.16 I2C Bridge

The I2C bridge mode allows a unidirectional I2C bus BCC reach-through from the User FPGA I2C Bus onto the BCCs isolated management BCC I2C bus. In consequence of that, the two-independent busses behave like one.

Unidirectional means in this context that only the SDA signal state is bidirectional (transferred to through the BCC) but not the SCL. SCL only traverses from User FPGA to management BCC I2C bus.

Having this feature active, allows accessing the both TMP441 temperature sensor and the SI5338 clock generator device. Both are accessible via their normal (original) I2C addresses.

Note that the Automatic Temperature Read Mode (TMP441_AUTO_TRD_EN) must be disabled before the bridge mode can be enabled.

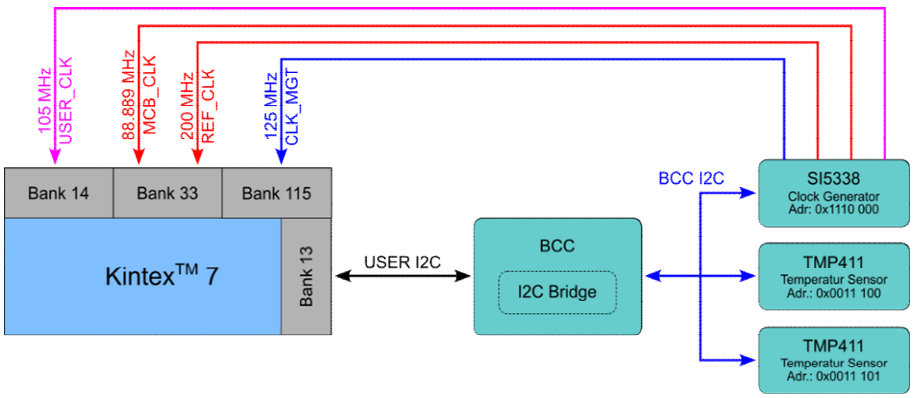


Figure 7-15 : User FPGA I2C to BCC I2C Bridge

For function description and register contents of the clock generator Si5338 and the temperature sensor TMP411 please use the data sheets of the respective device.

Do not change the SI5338 Output driver properties like "Format and Voltage"

Channel 0 must be 3.3 V LVDS

Channel 1 must be 3.3 V SSTL on A and B

Channel 2 must be 3.3 V CMOS on A and B

Channel 4 must be 3.3 V SSTL on A and B

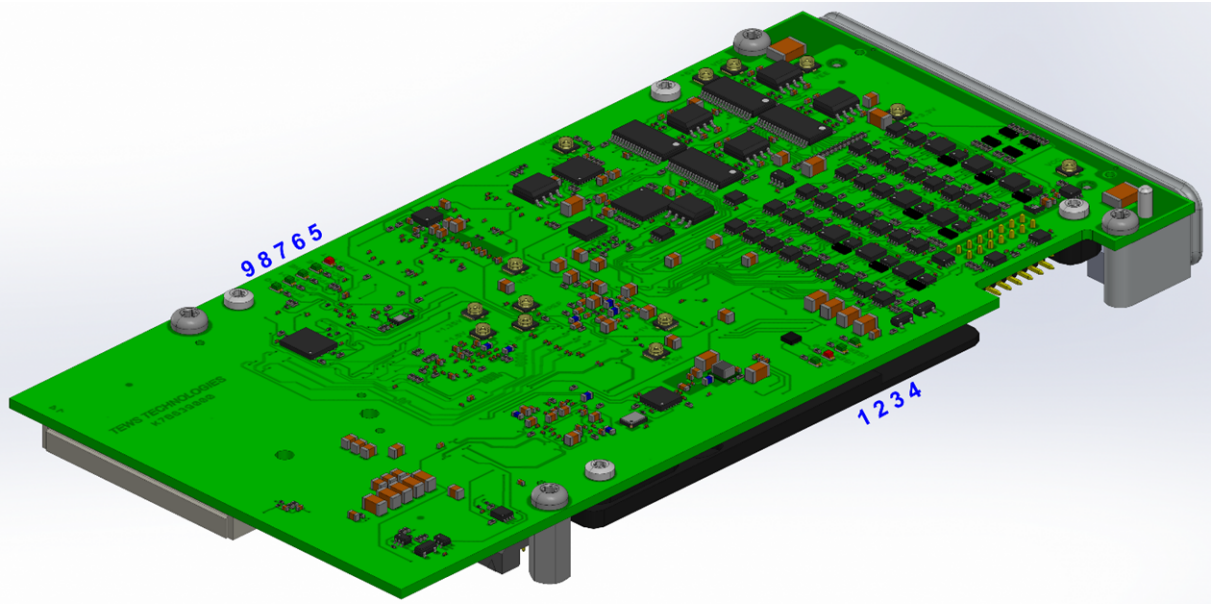
Do not change Si5338 Core VDD or I2C Bus Voltage

Core VDD = 3.3 V

I2C Bus Voltage = 2.5 V or 3.3 V

7.17 On-Board Indicators

The TXMC639 provides a couple of board-status LEDs as shown below. These include Power-Good and FPGA configuration status indications as well as two general purpose LEDs.



No.	LED	Color	State		Description
1	Power Good	Green	on	On-Board Power Supplies are all ok	Power Good Signal for all on-board power supplies.
2		Red	on	On-Board Power Supplies are not ok	
3	USER LED 0	Green	-		Design dependent, can be controlled by the User FPGA. Refer to chapter “User-GPIO”
4	USER LED 1	Green	-		
5	FPGA INIT	Red	on	INIT state is active	User FPGA (Kintex™ 7) INIT# - Pin LED. Indicates FPGA configuration
			off	Device is not configured	
6	BCC DONE	Green	flashing	Board initiation could not be completed	Board Configuration FPGA DONE-Pin LED Indicates successful FPGA configuration and initiation.
			on	Device is completely configured	
			off	Device is not configured	
7	FPGA DONE	Green	on	Device is completely configured	User FPGA (Kintex™ 7) DONE-Pin LED. Indicates successful FPGA configuration
			off	General State is not IDLE	
8	GPIO LED 0	Green	on	General State is IDLE	Configuration FPGA depends.
			off	PCI Reset is active	
9	GPIO LED 1	Green	on	PCI Reset is inactive	

Table 7-23: Board-Status and User LEDs

7.17.1 User FPGA LED Pinning

General purpose I/O connected to the User FPGA Kintex™ 7.

Signal	Bank	VCCO	Pin	Description
USER_LED0	14	3.3 V	H21	2x green on-board LEDs
USER_LED1			G21	

Table 7-24: TXMC639 User On-Board Indicators

For pin assignment, I/O standard, slew rate and driver performance please use the XDC files of the TXMC639 BRD Project.

7.18 User FPGA Reset Inputs

General purpose Reset input connected to the User FPGA Kintex™ 7.

Signal	Bank	VCCO	Pin	Description
DWNRST#	14	3.3 V	K21	Reset from PCIe Switch Based directly on the downstream reset of the PCIe switch on the TXMC639. See the PCIe switch data sheet for more information.
FPGA_RST	32	1.8 V	V16	Reset Input from BCC The reset signal is valid as long as the BCC is in its configuration phase. When all configuration processes on the TXMC639 are completed, this signal is deactivated.

Table 7-25: User FPGA Reset Inputs

For pin assignment, I/O standard, slew rate and driver performance please use the XDC files of the TXMC639 BRD Project.

8 Design Help

8.1 Board Reference Design

User applications for the TXMC639 may be developed by using the TXMC639 FPGA Board Reference Design.

TEWS offers this Board Reference Design as a well-documented basic example. It includes an .xdc constrain file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TXMC639. It implements a PCIe endpoint with interrupt support, register mapping, DDR3 memory access and basic I/O functions. It comes as a AMD Vivado 2020.1 project with source code and as a ready-to-download bit stream. This example design can be used as a starting point for own projects.

The TXMC639 FPGA Application design can be developed using the design software Vivado Design Suite. Licenses for design tools are required.

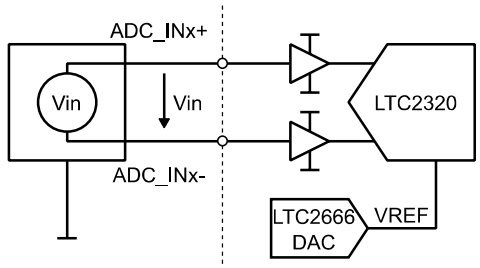
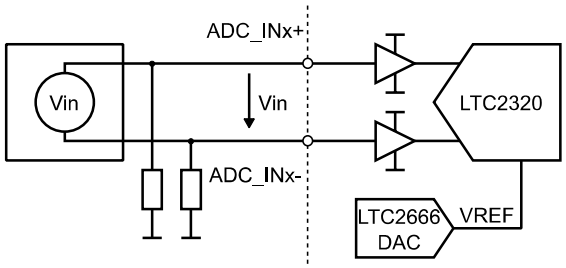
For TXMC639 FPGA Board Reference Design also see the included BRD User Manual.

9 I/O Interfaces

9.1.1 Front I/O - ADC Analog Input Level

All analog inputs are connected via an impedance converter and a second operation amplifier for level adjustment and filtering to the differential ADC inputs. This also serves as a protection of the ADC from excessive analog input levels.

The -3 dB limit of this input stage is at approx. 8MHz

Diff. Source with Ground Reference	Diff. Source without Ground Reference
	
Maximum VIN = ±20.56 V	Maximum VIN = ±20.56 V

The TXMC639 has differential analog inputs. When talking about the input voltage range of a differential input, one has to differentiate between the differential input voltage between the two pins, and the input voltage relative to ground for each pin.

With an maximum input voltage range of ±10.28 V (ground related) for each pin of the differential input, we get the ±20.56 V differential input voltages.

The table below shows the different differential voltages for the three input voltage levels sets.

Programmable Input Voltage Range	diff. VIN_{MAX}[1] (allowed voltage between input pins)	Common Mode Voltage Range	Input Voltage limit for each pin relative to common ground	Full scale differential input range
±20.56 V	±20.56 V	0 V	±10.28 V	41.12 V
±10.28 V	±10.28 V	±5 V	±10.28 V	20.56 V
±5.14 V	±5.14 V	±7.5 V	±10.28 V	10.28 V

Table 9-1 : Differential Input Voltage

[1]For differential, antiphase (180°) inputs with a zero common mode voltage

The maximum range of differential input is -20.56 V to +20.56 V, which results to a full scale range of 41.12 V for the ±10.28 V (per pin, relative to ground) Input voltage range.

The input voltage range of ADC channel can be set via BCC ADC Input Voltage Range Register.

9.1.2 Front I/O – Analog Output Level

All analog outputs of the AD5547 DAC are routed through operational amplifiers to front I/O connector.

Outputs Drive Current	**±10 mA**
Capacitive Load	1000 pF

Table 9-2 : DAC Electrical Interface

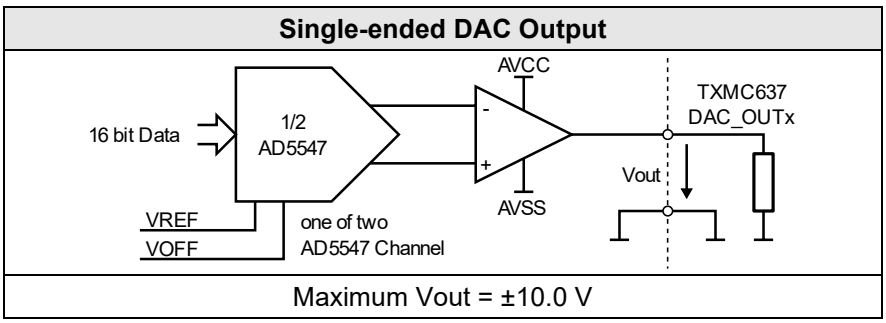


Figure 9-1 : DAC Output Interface

The output voltage range of each DAC channel can be set via VREF and VOFF.

See also the chapter about the configuration of the DAC output voltage in the BCC Register Description.

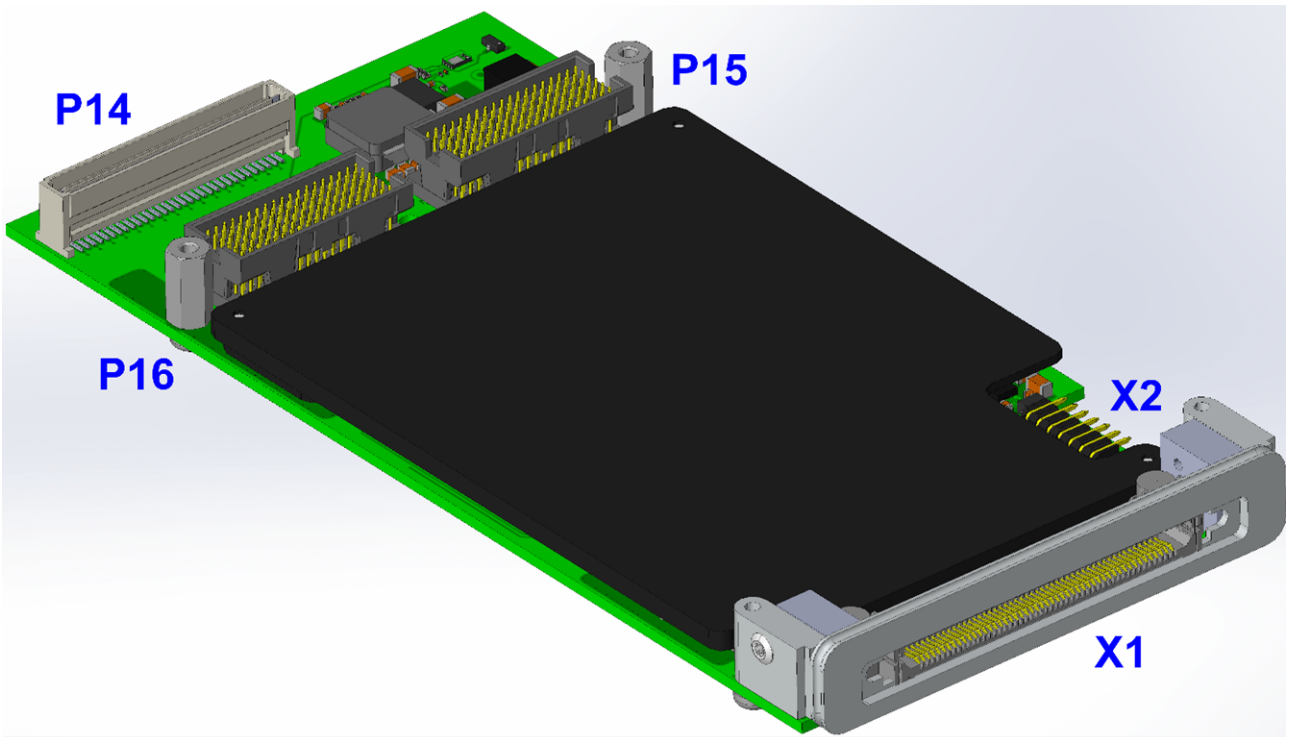
9.1.3 Rear I/O Interface

All 64 single-ended / 32 differential digital rear I/O Pins of the TXMC639 are directly routed from the User FPGA (Kintex™ 7) to the 64 pin P14 XMC rear connector. The I/O functions of these FPGA pins are directly dependent on the configuration of the FPGA.

The Kintex™ 7 VCCO voltage is set to 2.5 V, so only the 2.5 V I/O standards LVCMOS25 and LVDS25 are possible when using the TXMC639 rear I/O interface.

10 I/O Description

10.1 Overview



10.2 Front I/O Connector (X1)

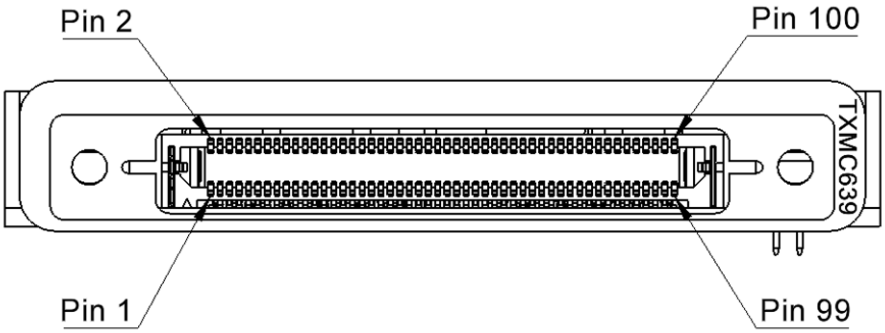


Figure 10-1 : Front Panel I/O Connector Numbering

Pin-Count	100
Connector Type	Rugged Edge Rate Strip, 0.8mm Pitch Connector
Source + Order Info	ERF8_050_01_L_D_RA_L_TR Samtec

Pin	I/O	Connector View	Pin	I/O
1	ADC_IN0+		2	ADC_IN1+
3	ADC_IN0-		4	ADC_IN1-
5	GND		6	GND
7	ADC_IN2+		8	ADC_IN3+
9	ADC_IN2-		10	ADC_IN3-
11	GND	Pin 100 Pi	12	GND
13	ADC_IN4+		14	ADC_IN5+
15	ADC_IN4-		16	ADC_IN5-
17	GND		18	GND
19	ADC_IN6+		20	ADC_IN7+
21	ADC_IN6-		22	ADC_IN7-
23	GND		24	GND
25	ADC_IN8+		26	ADC_IN9+
27	ADC_IN8-		28	ADC_IN9-
29	GND		30	GND
31	ADC_IN10+		32	ADC_IN11+
33	ADC_IN10-	Pin 2 Pi	34	ADC_IN11-
35	GND		36	GND
37	ADC_IN12+		38	ADC_IN13+
39	ADC_IN12-		40	ADC_IN13-
41	GND		42	GND
43	ADC_IN14+		44	ADC_IN15+
45	ADC_IN14-		46	ADC_IN15-

Pin	I/O		Connector View	Pin	I/O	
47	DAC_OUT0			48	DAC_OUT1	
49	GND			50	GND	
51	DAC_OUT2			52	DAC_OUT3	
53	GND			54	GND	
55	DAC_OUT4			56	DAC_OUT5	
57	GND			58	GND	
59	DAC_OUT6			60	DAC_OUT7	
61	GND			62	GND	
63	TTL_IO0			64	TTL_IO2	
65	TTL_IO1			66	TTL_IO3	
67	TTL_IO4			68	TTL_IO6	
69	TTL_IO5			70	TTL_IO7	
71	GND			72	GND	
73	TTL_IO8			74	TTL_IO10	
75	TTL_IO9			76	TTL_IO11	
77	TTL_IO12			78	TTL_IO14	
79	TTL_IO13			80	TTL_IO15	
81	GND			82	GND	
83	TTL_IO16	RS422_0A		84	TTL_IO18	RS422_1A
85	TTL_IO17	RS422_0B		86	TTL_IO19	RS422_1B
87	TTL_IO20	RS422_2A		88	TTL_IO22	RS422_3A
89	TTL_IO21	RS422_2B		90	TTL_IO23	RS422_3A
91	GND			92	GND	
93	TTL_IO24	RS422_4A		94	TTL_IO26	RS422_5A
95	TTL_IO25	RS422_4B		96	TTL_IO27	RS422_5B
97	TTL_IO28	RS422_6A		98	TTL_IO30	RS422_7A
99	TTL_IO29	RS422_6B		100	TTL_IO31	RS422_7B

Table 10-1: Pin Assignment Front Panel I/O Connector

10.3 Rear I/O Connector (P14)

Pin-Count	64
Connector Type	64pol. Mezzanine SMD Connector
Source + Order Info	Molex – 71436-2864

Pin	differential I/O	single ended I/O		Pin	differential I/O	single ended I/O
1	IO_R_0+	IO_R_0		33	IO_R_16+	IO_R_32
2	IO_R_0-	IO_R_1		34	IO_R_16-	IO_R_33
3	IO_R_1+	IO_R_2		35	IO_R_17+	IO_R_34
4	IO_R_1-	IO_R_3		36	IO_R_17-	IO_R_35
5	IO_R_2+	IO_R_4		37	IO_R_18+	IO_R_36
6	IO_R_2-	IO_R_5		38	IO_R_18-	IO_R_37
7	IO_R_3+	IO_R_6		39	IO_R_19+	IO_R_38
8	IO_R_3-	IO_R_7		40	IO_R_19-	IO_R_39
9	IO_R_4+	IO_R_8		41	IO_R_20+	IO_R_40
10	IO_R_4-	IO_R_9		42	IO_R_20-	IO_R_41
11	IO_R_5+	IO_R_10		43	IO_R_21+	IO_R_42
12	IO_R_5-	IO_R_11		44	IO_R_21-	IO_R_43
13	IO_R_6+	IO_R_12		45	IO_R_22+	IO_R_44
14	IO_R_6-	IO_R_13		46	IO_R_22-	IO_R_45
15	IO_R_7+	IO_R_14		47	IO_R_23+	IO_R_46
16	IO_R_7-	IO_R_15		48	IO_R_23-	IO_R_47
17	IO_R_8+	IO_R_16		49	IO_R_24+	IO_R_48
18	IO_R_8-	IO_R_17		50	IO_R_24-	IO_R_49
19	IO_R_9+	IO_R_18		51	IO_R_25+	IO_R_50
20	IO_R_9-	IO_R_19		52	IO_R_25-	IO_R_51
21	IO_R_10+	IO_R_20		53	IO_R_26+	IO_R_52
22	IO_R_10-	IO_R_21		54	IO_R_26-	IO_R_53
23	IO_R_11+	IO_R_22		55	IO_R_27+	IO_R_54
24	IO_R_11-	IO_R_23		56	IO_R_27-	IO_R_55
25	IO_R_12+	IO_R_24		57	IO_R_28+	IO_R_56
26	IO_R_12-	IO_R_25		58	IO_R_28-	IO_R_57
27	IO_R_13+	IO_R_26		59	IO_R_29+	IO_R_58
28	IO_R_13-	IO_R_27		60	IO_R_29-	IO_R_59
29	IO_R_14+	IO_R_28		61	IO_R_30+	IO_R_60
30	IO_R_14-	IO_R_29		62	IO_R_30-	IO_R_61
31	IO_R_15+	IO_R_30		63	IO_R_31+	IO_R_62
32	IO_R_15-	IO_R_31		64	IO_R_31-	IO_R_63

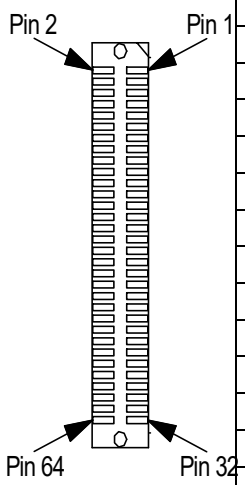


Figure 10-2 : Pin Assignment P14 Rear I/O Connector

10.4 Rear I/O Connector (P16)

Pin-Count	114
Connector Type	XMC Connector 114-pol Male
Source + Order Info	Samtec - ASP-105885-01

	A	B	C	D	E	F
1	Tx 0+	Tx 0-	-	Tx 1+	Tx 1-	-
2	GND	GND	-	GND	GND	-
3	Tx 2+	Tx 2-	-	Tx 3+	Tx 3-	-
4	GND	GND	-	GND	GND	-
5	-	-	-	-	-	-
6	GND	GND	-	GND	GND	-
7	-	-	-	-	-	-
8	GND	GND	-	GND	GND	-
9	Reserved	Reserved	-	Reserved	Reserved	-
10	GND	GND	-	GND	GND	-
11	Rx 0+	Rx 0-	-	Rx 1+	Rx 1-	-
12	GND	GND	-	GND	GND	-
13	Rx 2+	Rx 2-	-	Rx 3+	Rx 3-	-
14	GND	GND	-	GND	GND	-
15	-	-	-	-	-	-
16	GND	GND	DIG_IO_02-	GND	GND	DIG_IO_03-
17	-	-	DIG_IO_02+	-	-	DIG_IO_03+
18	GND	GND	DIG_IO_00-	GND	GND	DIG_IO_01-
19	-	-	DIG_IO_00+	-	-	DIG_IO_01+

Figure 10-3 : Pin Assignment P16 Rear I/O Connector

10.5 FPGA JTAG Header (X2)

This header is connected via multiplexers to the JTAG I/Os of the on-board User FPGA JTAG interface. The BCC can disconnect the header to become the JTAG master. The pinout of this header is designed in accordance with the AMD Platform Cable USB II. This allows the direct usage of AMD software-tools like Vivado Logic Analyzer or the Vivado Hardware Manager.

Pin-Count	14
Connector Type	2.00 mm Pitch Milli-Grid™ Header
Source + Order Info	Molex 877601416 or compatible

Pin	Signal	Description
1	NC	Not Connected
2	V_{REF}	JTAG Reference Voltage (3.3 V)
3	GND	Ground
4	TMS	Test Mode Select Input
5	GND	Ground
6	TCK	Test Clock
7	GND	Ground
8	TDO	Test Data Output (TAP Controller: TDI)
9	GND	Ground
10	TDI	Test Data Input (TAP Controller: TDO)
11	GND	not connected on the TXMC639
12	NC	not connected on the TXMC639
13	PGND	Used on TXMC639 for AMD Header present detection
14	NC	HALT_INIT_WP signal. Optional. Not connected on the TXMC639

Table 10-2: Pin Assignment JTAG Header