*The Embedded I/O Company*

# TXMC888

## Two Channel SFP+ 10Gb Ethernet Adapter

Version 1.0

## User Manual

Issue 1.0.2

December 2017

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## TXMC888-10R

Two channel 10 Gigabit Ethernet interface SFP+ front panel I/O
(RoHS compliant)

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### Style Conventions

Hexadecimal characters are specified with prefix 0x, i.e. 0x029E (that means hexadecimal value 029E).

For signals on hardware products, an ‚Active Low' is represented by the signal name with # following, i.e. IP_RESET#.

Access terms are described as:

| | |
|---|---|
| W | Write Only |
| R | Read Only |
| R/W | Read/Write |
| R/C | Read/Clear |
| R/S | Read/Set |

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| Issue | Description | Date |
|---|---|---|
| 1.0.0 | Initial issue | November 2015 |
| 1.0.1 | Product description updated | March 2016 |
| 1.0.2 | Storage Temperature Range corrected | December 2017 |

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# 1 Product Description

The TXMC888 is a Switched Mezzanine Card (XMC) compatible module providing a two channel 10 Gigabit Ethernet Enhanced Small Form Factor Pluggable (SFP+) interface.

The XMC-Connector P15 provides access to the Intel™ 82599ES dual port 10GbE controller via an x8 PCIe link.

The TXMC888's SFP+ Cages accept various SFP and SFP+ transceiver modules. These two SFP+ hosts are connected to the Ethernet Controller's SFI Interfaces.

The following transceiver modules have been successfully tested with the TXMC888:

- Intel XDACBL1M
  (SFP+ Direct Attach Twinaxial Cable)
- Finisar FCBG110SD1C01
  (SFP+ SFPwire Active Optical Cable)
- Intel E10GSFPSR
  (SFP+ 10GBASE-SR or 1000BASE-SX)
- Finisar FTLX8571D3BCV
  (SFP+ 10GBASE-SR or 1000BASE-SX)
- Intel E10GSFPLR
  (SFP+ 10GBASE-LR or 1000BASE-LX)
- Finisar FTLX1471D3BCV
  (SFP+ 10GBASE-LR or 1000BASE-LX)
- Finisar FCLF8522P2BTL
  (SFP 1000BASE-T)

All compatible transceivers modules and replacements of the tested modules will also work properly with the TXMC888.

The controller is equipped with a 1 Mbit serial flash memory for Boot ROM and a 128 Kbit EEPROM storing configuration data. LEDs in the front panel indicate the different network activities.

For preconfigured variants of the hardware module containing transceiver modules, please contact TEWS.

The TXMC888-10R provides two 10GbE Interfaces via front panel SFP+ connectors.

**Software support:**

- Software support for Intel™ 82599ES at www.intel.com
- For operating systems not supported by Intel™, please contact TEWS.

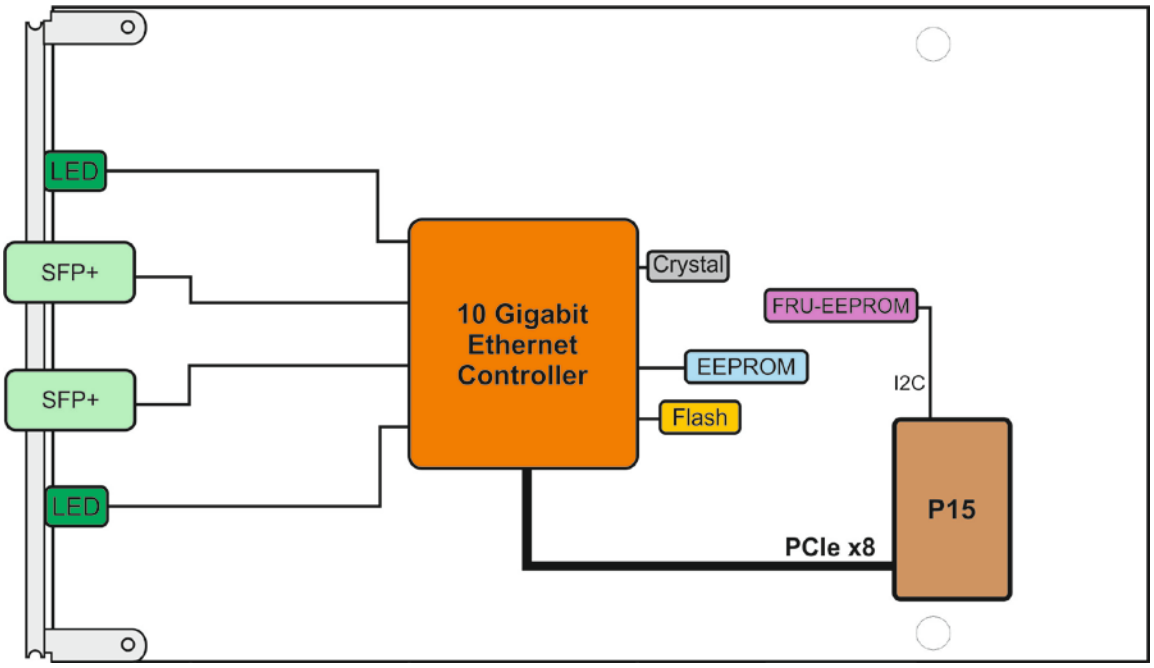


Figure 1-1 : Block Diagram

# 2 Technical Specification

| | | |
|---|---|---|
| **XMC Interface** | | |
| **Mechanical Interface** | Switched Mezzanine Card (XMC) Interface conforming to ANSI/VITA 42.0-2008 (Auxiliary Standard)<br>Standard single-width (149 mm x 74 mm) | |
| **Electrical Interface** | PCI Express (Base Specification 2.0) up to x8 compliant interface conforming to ANSI/VITA 42.3-2006 (XMC PCI Express Protocol Layer Standard) | |
| | | |
| **On Board Devices** | | |
| **10 Gigabit Ethernet Controller** | 82599ES (Intel) | |
| **IPMI resource FRU Data EEPROM** | M24C02 (STMicroelectronics) | |
| | | |
| **Ethernet Interface** | | |
| **Number of Interfaces** | 2 | |
| **Link** | 10GBase-CU (SFP+ Direct Attach, twinax)<br>SFPwire SFP+ Active Optical Cable<br>10GBase-SR/SW / 1000Base-SX<br>10GBase-LR/LW / 1000Base-LX<br>1000Base-T | |
| **I/O Connector** | SFP+ (Molex 74754-0103 and 74441-0001 or compatible) | |
| | | |
| **Physical Data** | | |
| **Power Requirements** | 350mA typical @ VPWR = +12V DC (no link)<br>app. -10mA per 1Gbit/s Link<br>app. additional 50mA per 10Gbit/s Link<br><br>800mA typical @ VPWR = +5V DC (no link)<br>app. -30mA per 1Gbit/s Link<br>app. additional 100mA per 10Gbit/s Link<br><br>1mA typical @ +3.3Vaux DC | |
| **Temperature Range** | Operating<br>Storage | 0°C to +70°C<br>-40°C to +85°C |
| **MTBF** | 555000 h<br>MTBF values shown are based on calculation according to MIL-HDBK-217F and MIL-HDBK-217F Notice 2; Environment: $G_B$ 20°C.<br>The MTBF calculation is based on component FIT rates provided by the component suppliers. If FIT rates are not available, MIL-HDBK-217F and MIL-HDBK-217F Notice 2 formulas are used for FIT rate calculation. | |
| **Humidity** | 5 – 95 % non-condensing | |
| **Weight** | 105 g | |

Table 2-1 : Technical Specification

# 3 10 Gigabit Ethernet Controller

## 3.1 PCI Bus Topology

The Intel 82599ES 10 Gigabit Ethernet Controller is represented by a multifunctional device on the PCI bus. The two different Ethernet Channels can be identified by the corresponding function of the device.

**Multifunctional device (Intel Corporation)**

Bus : Device : **Function 0x00**

| Ethernet Controller | |
|---|---|
| Vendor ID | 0x8086 (Intel Corporation) |
| Device ID | 0x10FB (82599ES 10-Gigabit SFI/SFP+ Network Connection) |

Bus : Device : **Function 0x01**

| Ethernet Controller | |
|---|---|
| Vendor ID | 0x8086 (Intel Corporation) |
| Device ID | 0x10FB (82599ES 10-Gigabit SFI/SFP+ Network Connection) |

## 3.2 Intel 82599ES Function PCI Header

| PCI CFG Register Address | Write '0' to all unused (Reserved) bits | | | | PCI writeable | Initial Values (Hex Values) |
|---|---|---|---|---|---|---|
| | 31 24 | 23 16 | 15 8 | 7 0 | | |
| 0x00 | Device ID | | Vendor ID | | N | 10FB 8086 |
| 0x04 | Status Register | | Command Register | | Y | 0010 0406 |
| 0x08 | Class Code | Subclass | Programming Interface | Revision ID | Y[7:0] | 02 00 00 01 |
| 0x0C | BIST | Header Type | Latency Timer | Cache Line Size | Y[7:0] | 00 80 00 10 |
| 0x10 | Base Address Register 0 | | | | Y | FFFE0004 |
| 0x14 | Base Address Register 1 | | | | Y | FFFFFFFF |
| 0x18 | Base Address Register 2 | | | | Y | FFFFFFE1 |
| 0x1C | Base Address Register 3 | | | | Y | 00000000 |
| 0x20 | Base Address Register 4 | | | | Y | FFFFC004 |
| 0x24 | Base Address Register 5 | | | | Y | FFFFFFFF |
| 0x28 | CardBus CIS | | | | N | 00000000 |
| 0x2C | Subsystem Device ID | | Subsystem Vendor ID | | N | FFFF FFFF |
| 0x30 | Expansion ROM | | | | Y | 00000000 |
| 0x34 | Reserved | | | Capabilities Pointer | N | 000000 40 |
| 0x38 | Reserved | | | | N | 00000000 |
| 0x3C | Max_Lat | Min_Gnt | Interrupt Pin | Interrupt Line | Y[7:0] | 00 00 **01/02** 00 |
| 0x40 | PMC | | Next_Item_Ptr | Cap_ID | N | 4823 50 01 |
| 0x44 | Unknown | Data Register | PMCSR | | Y | 00 00 1E00 |

Table 3-1 : Intel 82559ES PCI Header

# 4 LEDs

The TXMC888 provides four LEDs in the front panel for each of the two channels indicating the corresponding network behavior.

| LED | Colour | Description |
|---|---|---|
| 10G | Yellow | Asserted when a 10 Gbit/s link is established and maintained |
| 1G | Blue | Asserted when a 1 Gbit/s link is established and maintained |
| ACT | Green | Active when link is established and packets are being transmitted or received |
| 100M | Orange | Asserted when a 100 Mbit/s link is established and maintained |

Table 4-1 : LED behavior

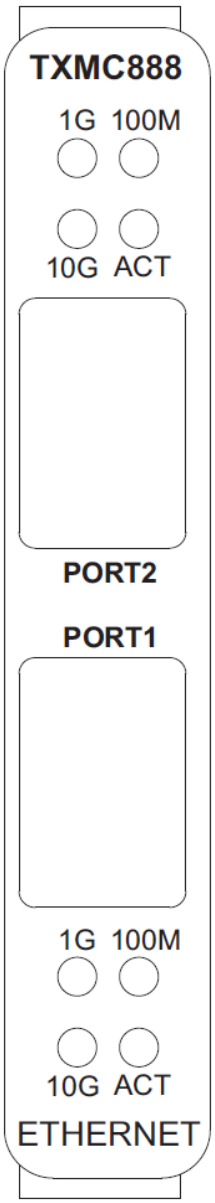


Figure 4-1 : TXMC888 Front Panel

# 5 Pin Assignment – I/O Connector

## 5.1 XMC Connector P15

| | A | B | C | D | E | F |
|---|---|---|---|---|---|---|
| **1** | PET0p0 | PET0n0 | 3.3V | PET0p1 | PET0n1 | VPWR |
| **2** | GND | GND | $\overline{TRST}$ | GND | GND | $\overline{PERST}$ |
| **3** | PET0p2 | PET0n2 | 3.3V | PET0p3 | PET0n3 | VPWR |
| **4** | GND | GND | TCK | GND | GND | $\overline{MRSTO}$ |
| **5** | PET0p4 | PET0n4 | 3.3V | PET0p5 | PET0n5 | VPWR |
| **6** | GND | GND | TMS | GND | GND | +12V |
| **7** | PET0p6 | PET0n6 | 3.3V | PET0p7 | PET0n7 | VPWR |
| **8** | GND | GND | TDI | GND | GND | -12V |
| **9** | Reserved | Reserved | Reserved | Reserved | Reserved | VPWR |
| **10** | GND | GND | TDO | GND | GND | GA0 |
| **11** | PER0p0 | PER0n0 | $\overline{MBIST}$ | PER0p1 | PER0n1 | VPWR |
| **12** | GND | GND | GA1 | GND | GND | $\overline{MPRESENT}$ |
| **13** | PER0p2 | PER0n2 | 3.3V AUX | PER0p3 | PER0n3 | VPWR |
| **14** | GND | GND | GA2 | GND | GND | MSDA |
| **15** | PER0p4 | PER0n4 | Reserved | PER0p5 | PER0n5 | VPWR |
| **16** | GND | GND | MVMRO | GND | GND | MSCL |
| **17** | PER0p6 | PER0n6 | Reserved | PER0p7 | PER0n7 | Reserved |
| **18** | GND | GND | Reserved | GND | GND | Reserved |
| **19** | REFCLK+0 | REFCLK-0 | Reserved | $\overline{WAKE}$ | $\overline{ROOT0}$ | Reserved |

Table 5-1 : XMC Connector P15

## 5.2 SFP+ Connector

| Pin | Signal |
|---|---|
| 1 | VeeT |
| 2 | Tx_Fault |
| 3 | Tx_Disable |
| 4 | SDA |
| 5 | SCL |
| 6 | Mod-ABS |
| 7 | RS0 |
| 8 | Rx_LOS |
| 9 | RS1 |
| 10 | VeeR |
| 11 | VeeR |
| 12 | RD- |
| 13 | RD+ |
| 14 | VeeR |
| 15 | VccR |
| 16 | VccT |
| 17 | VeeT |
| 18 | TD+ |
| 19 | TD- |
| 20 | VeeT |

Table 5-2 : SFP+ Connector